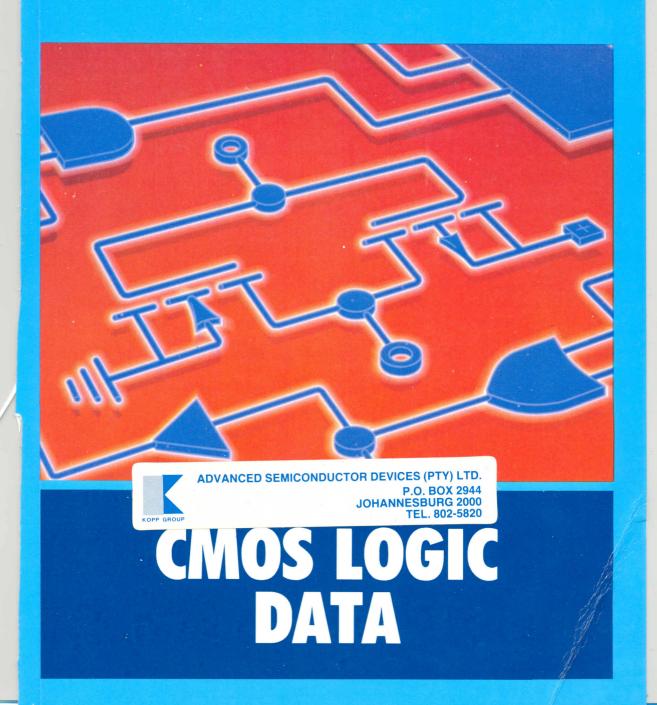


# (M) MOTOROLA Semiconductors



Q quantum electronics

Box 391262

Bramley
2018

**Master Index** 

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- Package Dimensions

# CMOS LOGIC DATA

Prepared by Technical Information Center

This book presents technical data for the broad line of CMOS logic integrated circuits and demonstrates Motorola's continued commitment to Metal-Gate CMOS. Complete specifications are provided in the form of data sheets. In addition, a Product Selector Guide and a Handling and Design Guidelines chapter have been included to familiarize the user with these circuits.

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Master Index 1

# **MASTER INDEX**

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Telecom — See DL136, Telecommunications Data
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14422	Remote Control Transmitter (Product Cancelled)	
14430	Input Address Encoder	
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14435	3½ Digit A/D Logic Subsystem (Product Cancelled)	
14442	Microprocessor-Compatible A/D Converter	
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14460	Automotive Speed Control Processor	
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14466	Low Cost Smoke Detector	
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14468	Interconnectable Smoke Detector	. SF
14469	Addressable Asynchronous Receiver/Transmitter	
14490	Hex Contact Bounce Eliminator	
14495-1	Hexadecimal-to-7 Segment Latch/Decoder ROM/Driver	
14497	PCM Remote Control Transmitter	The state of the s
14499	7-Segment LED Display Decoder/Driver with Serial Interface	
14500B	Industrial Control Unit	
14501UB 14502B	Triple Gate	
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143403	Quad Line Driver	Telecom
144110	Hex D/A Converter with Serial Interface	
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145104	PLL Frequency Synthesizer (Not Recommended for New Designs)	
145106	PLL Frequency Synthesizer	
145107	PLL Frequency Synthesizer (Not Recommended for New Designs)	
145109	PLL Frequency Synthesizer (Not Recommended for New Designs)	
145112	PLL Frequency Synthesizer (Not Recommended for New Designs)	
145143	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
145144	4-Bit Data Bus Input PLL Frequency Synthesizer	CE
145145-1	(Not Recommended for New Designs)	
145146-1	4-Bit Data Bus Input PLL Frequency Synthesizer	
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145159-1	Serial Input PLL Frequency Synthesizer with Analog Phase Detector	SF
145402	13-Bit Linear Codec	
145406	RS-232 Interface	
145409	Pulse Dialer	
145411	Baud Rate Generator	
145412	Pulse/Tone Reperatory Dialer	Telecom
145413	Pulse/Tone Reperatory Dialer	
145414	Dual Tuneable Low-Pass Sampled Data Filters	
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145418	Master Digital Loop Transceiver	

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145422	MDPSK Universal Digital Loop Transceiver (2-Wire Master)	Telecom
145425	160 kbps ISDN Universal Digital Loop Transceiver	Telecom
145426	MDPSK Universal Digital Loop Transceiver (2-Wire Slave)	Telecom
145428	Data Set Interface	Telecom
145429	Telset Audio Interface Circuit	Telecom
145432	2600 Hz Tone Signalling Filter	Telecom
145433	Tuneable Notch/Band-Pass Filter 1911w2 1019922010 A.X.	Telecom
145439	Transcoder	Telecom
145440	Low-Speed Modem Filter 19viiQ 9m.l bsu9	Telecom
145441	Low-Speed Modem Filter shelfd Ishae daw hahavngo Ald xeH	Telecom
145445	Low-Speed Modem Filter 300 Baud FSK Modem	Telecom
145450	1200 Baud FSK Modem	Telecom
145453	33-Segment LCD Driver with Serial Interface	SF
146805	Family of 8-Bit CMOS MCUs/MPUs	MCU,MPU
146818	Real-Time Clock/RAM 1950090 011100 9101199	MCU,MPU
146823	Parallel Interface 1950990 lostno3 etome 8	MCU,MPU
1468705	8-Bit CMOS MCUs with EPROM	MCU,MPU
		145156-1
	Pulse/Tone Reperatory Dialer	

# 2

# CMOS Selection Guide by Function

	BERGNION
Product Selection	n Guide
Equivalent Gat	le Count
8-Input NAND Gate	
Dual 3-Input NOR Gate plus Inverter	
	Complex Gate
	MC14519B

# 2

# **CMOS Selection Guide by Function**

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MC14000UB MC14002B	Dual 3-Input NOR Gate plus Inverter	6-3 6-20
MC14002UB MC14078B	Dual 4-Input NOR Gate	6-20 6-171
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MC14081B MC14073B MC14082B	Quad 2-Input AND Gate Triple 3-Input AND Gate Dual 4-Input AND Gate	6-172 6-164 6-173
OR Gates		
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	4-Bit AND/OR Selector (Quad 2-Channel Data Selector or Quad Exclusive NOR Gate)	6-298
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**Function** 

Device

Flip-Flops/Latches
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MC14027B

MC14042B MC14043B

MC14044B

MC14076B MC14175B

Inverters/Buffers/Level Translator

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MC14015B	Dual 4-Bit Static Shift Register	
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The following is a list of equivalent gate counts for some of Motorola's CMOS devices. In general for CMOS, the number of equivalent gates is equal to the total number of transistors on chip divided by four. This list includes only those devices with equivalent gate counts known at the time of this printing.

DEVICE	EQUIVALENT GATE COUNT	DEVICE	EQUIVALENT GATE COUNT
MC14000UB	3.5	MC14175B	39.5
MC14000B		MC14410	245
MC14001B	Resettable Monost		245
MC140010B		MC14411	
MC14002B	AttuM eld7 sonoM el	MC14433	375
MC140020B	61.5	MC14469	378
MC14006B	1.5	MC14469 MC14490	136.5
MC140070B	40		17
AC14006B	8	MC14503B MC14504B	37.5
MC14011UB	4	MC14504B MC14508B	42 8800
			198 910174 8580
AC14012B	7 (3190.)	MC14510B	14
AC14012UB	4. (algod )		
AC14013B	16	MC14512B	bA 008117 - 8008
AC14016B	8	MC14514B	Igmoo a 59 a raa
AC14017B	62.5	MC14515B	67 858
AC14023B	9	MC14516B	01
AC14023UB	4.5	MC14517B	110
AC14024B	59	MC14518B	43.5
/C14025B	9	MC14520B	43.5
IC14025UB	4.5	MC14522B	86
/C14028B	26	MC14526B	86
/C14029B	65.5		9187 CO 46 8758
/IC14034B	145	MC14528B	119-5 24 gaza
/IC14035B	38.5	MC14532B	38.5
IC14040B	73	MC14536B	103
/IC14042B	17.5	MC14538B	38
/IC14046B	35	MC14539B	20
/IC14049UB	3	MC14541B	93 oxloan
/IC14050B	6	MC14543B	52
/IC14051B	48.5	MC14549B	189 18-5122 8786
/IC14052B	48.5	MC14553B	147.5
/IC14053B	32.5	MC14555B	21
/IC14066B	13	MC14556B	25
/IC14068B	8	MC14557B	232.5
/IC14069UB	3	MC14559B	122 909
/IC14071B	10	MC14568B	137.25
/IC14072B	8	MC14569B	156
/IC14073B	10.5	MC14572UB	4
IC14075B	10.5	MC14573	rtsubni 70sasoo
IC14078B	7.5	MC14574	9
1C14081B	10	MC14575	Soon Industrial
MC14082B	8	MC145106	220.5
/C14093B	16	MC145146-1	1423
IC14094B	79	MC145151-1	2000
1C14099B	70	MC145152-1	2000
AC14161B	72.5	MC145155-1	1626
/C14163B	72.5	MC145156-1	1626
AC14174B	43.5	MC145158-1	1626

Progran	am
High Temperature Tes	

	) towari	

# The "BETTER" Program

Motorola's reliability and quality-enhanced program was developed to provide improved levels of quality and reliability for standard commercial products.

The "BETTER" program is offered on Metal-Gate CMOS in dual-in-line ceramic and plastic packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industry's finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing each tailored to meet different user needs at nominal costs.

The program is designed to:

- Eliminate Incoming Electrical Inspection
- Estimate Need for Independent Test Labs and Associated Extra Time and Costs
- Reduce Field Failures
- Reduce Service Calls
- Reduce Equipment Downtime
- Reduce Board and System Rework
- Reduce Infant Mortality
- Save Time and Money
- Increase End-Customer Satisfaction

# BETTER PROCESSING — STANDARD PRODUCT PLUS:

100% Screen	Level I "S"	Level II "D"	Level III "DS"
Temp Cycle 10 Cycles — 25°C to +150°C	×		×
25°C Functional and Parametric Test	X	X	x
High Temperature Test*	×		×
Burn-In		X	×
25°C Post Burn-In Functional and Parametric Test		X	X

<sup>\*</sup>Thigh = +125°C for AL Device, +85°C for CL/CP Device.

# "BETTER" AQL GUARANTEES

			AQL*	
Test	Condition	Level I	Level II	Level III
High Temperature Functional	T <sub>A</sub> = 100°C or T <sub>A</sub> Max	0.065		0.065
DC Parametric	T <sub>A</sub> = 25°C	0.065	0.065	0.065
DC Parametric	T <sub>A</sub> Max	0.39		0.39
External Visual and Mechanical	Major/Minor	0.065	0.065	0.065
Hermeticity (Not Applicable to Plastic Packages)	Gross/Fine	0.15	0.15	0.15

<sup>\*&</sup>quot;AQL" values shown are for reference only. "LTPD" type sampling plans that are equal to or tighter than values indicated may be used.

Also, the guaranteed electrical and visual/mechanical AQL levels will be progressively tightened. Contact your nearest Motorola sales office for current values.

# PART MARKING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

# **HOW TO ORDER**

MC14001B CP
Part Standard "B Identification Package P Suffix LI

S "BETTER" PROCESSING LEVEL II = SUFFIX S LEVEL III = SUFFIX D LEVEL III = SUFFIX DS

**B** and **UB** Series Family Data

over the remperature range with a 5.0 V aupply. This

The CMOS Devices in this volume which have a B or UB suffix meet the minimum values for the industry-standardized# family specification. These standardized values are shown in the Maximum Ratings and Electrical Characteristics Tables. In addition to a standard minimum specification for characteristics the B/UB devices feature:

- 3-18 volt operational limits
- Capable of driving two low-power TTL loads or one low-power Schottky TTL load over the rated temperature range
- Direct Interface to High-Speed CMOS
- Maximum input current of ± 1 μA at 15 volt power supply over the temperature range
- · Parameters specified at 5.0, 10, and 15 volt supply
- Noise margins: B Series 1.0 V min @ 5.0 V supply 2.0 V min @ 10 V supply 2.5 V min @ 15 V supply

**UB** Series 0.5 V min @ 5.0 V supply

1.0 V min @ 10 V supply 1.0 V min @ 15 V supply

The industry-standardized maximum ratings are shown at the bottom of this page. Limits for the static characteristics are shown in two formats: Table 1 is in the industry format and

Table 2 is in the equivalent Motorola format. The Motorola format is used throughout this data book. Additional specification values are shown on the individual data sheets.

Switching characteristics for the B and UB series devices are

specified under the following conditions:
Load Capacitance, C<sub>L</sub>, of 50 pF
Input Voltage equal to V<sub>SS</sub> – V<sub>DD</sub> (Rail-to-Rail swing)
Input pulse rise and fall times of 20 ns

Propagation Delay times measured from 50% point of input voltage to 50% point of output voltage Three different supply voltages: 5, 10, and 15 V

# Exceptions to the B and UB Series Family Specification

There are a number of devices which have a B or UB suffix whose inputs and/or outputs vary somewhat from the family specification because of functional requirements. Some cate gories of notable exceptions are:

Devices with specialized outputs on the chip, such as NPN emitter-follower drivers or transmission gates, do not meet output specifications.

#Specifications coordinated by EIA/JEDEC Solid-State Products Council.

Devices with specialized inputs, such as oscillator inputs, have unique input specifications.

The input voltage specification is interpreted as the worstcase input voltage to produce an output level of "1" or "0". This "1" or "0" output level is defined as a deviation from the supply (VDD) and ground (VSS) levels. For a 5.0 V supply, this deviation is 0.5 V; for a 10 V supply, 1.0 V; and for 15 V, 1.5 V. As an example, in a device operating at a 5.0 V supply, the device with the input starting at ground is guaranteed to switch on or before 3.5 V and not to switch up to 1.5 V. Switching and not switching are defined as within 0.5 V of the ideal output level for the example with a 5.0 V supply. The actual switching level referred to the input is between 1.5 V and 3.5 V.

# Noise Margin

The values for input voltages and the defined output deviations lead to the calculated noise margins. Noise margin is defined as the difference between VIL or VIH and Vout (output deviation). As an example, for a noninverting buffer at VDD = So volts:  $V_{\rm IL} = 1.5$  volts and  $V_{\rm out} = 0.5$  volts. Therefore, Noise Margin equals  $V_{\rm IL} - V_{\rm out} = 1.0$  volt. This figure is useful while cascading stages (See Figure 1). With the input to the first stage at a worst-case voltage level  $(V_{\rm IL} = 1.5 \text{ V})$ , the outlier ungraphed to be no greater than 0.5 volts with 5.0 volts. put is guaranteed to be no greater than 0.5 volts with a 5.0 volt supply. Since the maximum allowable logic 0 for the second stage is 1.5 volts, this 0.5 volt output provides a 1.0 volt margin for noise to the next stage.

# **Output Drive Current**

Devices in the B Series are capable of sinking a minimum of 0.36 mA over the temperature range with a 5.0 V supply. This value guarantees that these CMOS devices will drive one lowpower Schottky TTL input.

# **B Series vs UB CMOS**

The primary difference between B series and UB series devices is that UB series gates and inverters are constructed with a single inverting stage between input and output. The decreased gain caused by using a single stage results in less noise immunity and a transfer characteristic that is less ideal.

The decreased gain is quite useful when CMOS Gates and inverters are used in a "Linear" mode to form oscillators, monostables, or amplifiers. The decreased gain results in increased stability and a "cleaner" output waveform. In addition to linear operation, the UB gates and inverters offer an increase in speed, since only a single stage is involved.

The B and UB series, and devices with no suffix can be used interchangeably in digital circuits that interface to other CMOS devices, such as High-Speed CMOS Logic.

MAXIMUM RATINGS\* (Voltages Referenced to Voc.)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin. lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

FIGURE 1 50 V  $V_{out} = 0.5 V$  $V_{IL} = 1.5 V$ Vout Second Stage First Stage  $V_{IL} = 1.5 V$ (Noninverting Buffer (Noninverting Buffer)

# TABLE 1 - EIA/JEDEC FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

		*harman T	TEMP	VDD		CVACEBACO.		LIM	A STATE OF THE PARTY OF THE PAR		40000	SARAS.
	PARAN	IETER	RANGE	(Vde)	CONDITIONS	TLO	ow°	+ 20	5°C		GH°	UNITS
1			HANGE	(000)		Min	Mex	Min	Mex	Min	Max	-
100	Quieso	ce Current	Mil	5 10 15	Vin = VSS or VDD	- 10 or 5 VV. - 0 or 5 (5 V.	0.25 0.5 1.0	6 01	0.25 0.5 1.0	16	7.5 15 30	μAdc
	ap.A.kn	GATES	Comm	5 10 15	All velid input combinations	, VS , VS 2 10 0 =	1.0 2.0 4.0	8	1.0 2.0 4.0		7.5 15 30	μAdc
			Mil	5 10 15	VIN = VSS or VDD	10 0 * VEX	1.0 2.0 4.0	01 21	1.0 2.0 4.0		30 60 120	μAdc
	eteloni etsiloni eteloni	BUFFERS, FLIP-FLOPS	Comm	5 10 15	All valid input combinations	VSt to VSt to	4 8 16	15	4.0 8.0 16.0		30 60 120	μAdc
	and a		Mil	5 10 15	VIN = VSS or VDD	MGK so	5 10 20	22	5 10 20	100	150 300 600	μAdc
		MSI	00	5 10 15	All valid input combinations	561 0 <sup>9</sup> 4 1 0 <sup>0</sup> 38	20 40 80	ib sense speck an	20 40 80	ent voca t yours	150 300 600	μAdc
VOL	OL Low-Level Output Voltage		All	5 10 15	VIN = VSS or VDD		0.05 0.05 0.05		0.05 0.05 0.05		0.05 0.05 0.05	Vdc
Vон	High-Level Output Voltage		All	5 10 15	VIN = VSS or VDD	4.95 9.95 14.95	RO3 1	4.95 9.95 14.95	LA FG	4.95 9.95 14.95	OW -	Vdc
VIL	Low \B Typ	/oltage#	All	5 10 15	V <sub>O</sub> = 0.5V or 4.5V V <sub>O</sub> = 1.0V or 9.0V V <sub>O</sub> = 1.5V or 13.5V II <sub>O</sub> I < 1µA	ledrey	1.5 3.0 4.0		1.5 3.0 4.0	EB 1944	1.5 3.0 4.0	Vdc
VIL	Low \UB To	/oltage#	All	5 10 15	VO = 0.5V or 4.5V VO = 1.0V or 9.0V VO = 1.5V or 13.5V IO   < 1µA	70,4	1.0 2.0 2.5	u m	1.0 2.0 2.5		1.0 2.0 2.5	Vdc
VIH	Input High ' B Typ	Voltage#	All	5 10 15	V <sub>O</sub> = 0.5V or 4.5V V <sub>O</sub> = 1.0V or 9.0V V <sub>O</sub> = 1.5V or 13.5V II <sub>O</sub> < 1µA	3.5 7.0 11.0		3.5 7.0 11.0		3.5 7.0 11.0	500	Vdc
VIH	Input High UB To	Voltage#	All	5 10 15	V <sub>O</sub> = 0.5V or 4.5V V <sub>O</sub> = 1.0V or 9.0V V <sub>O</sub> = 1.5V or 13.5V II <sub>O</sub> I < 1µA	4.0 8.0 12.5		4.0 8.0 12.5		4.0 8.0 12.5	N 2 0 4 N 6 F 16 P 6 F 16	Vdc
lor		t Low Current	Mil	5	V <sub>O</sub> = 0.4V, V <sub>IN</sub> = 0 or 5V V <sub>O</sub> = 0.5V,	0.64		0.51		0.36	04 8,8 vi abV 6.8 7 8,81 s	mAdd
			9.1	10	V <sub>IN</sub> = 0 or 10V V <sub>O</sub> = 1.5V, V <sub>IN</sub> = 0 or 15V	1.6	lage.	1.3		0.9	spyr Bi IV 8.0 w IV 0.1 w	apallov a.s.= or a.c.= or
	nov.		Com	5	V <sub>O</sub> = 0.4V, V <sub>IN</sub> = 0 or 5V V <sub>O</sub> = 0.5V,	0.52	tus	0.44		0.36	4.5.V	
				10	V <sub>IN</sub> = 0 or 10V V <sub>O</sub> = 1.5V, V <sub>IN</sub> = 0 or 15V	3.6		3.0		0.9	V 0.6 H	0.1.0

# ELECTRICAL CHARACTERISTICS

-	-		TEAAD				1000	LIM	ITS	THE RESIDENCE	7 251 YU	EDITOR PE
	PARAMETER TEMP VDD CONDITIONS		TLO	TLOW*		5°C	THIGH		UNITS			
			MANGE	(Age)		Min	Max	Min	Max	Min	Max	PARKET
Юн	100000000000000000000000000000000000000	ut High ce) Current	Mil BE:0 8.0	5	V <sub>O</sub> = 4.6V, V <sub>IN</sub> = 0 or 5V V <sub>O</sub> = 9.5V, V <sub>IN</sub> = 0 or 10V V <sub>O</sub> = 13.5V,	-0.25 -0.62	to a <sub>rel</sub> v	-0.2 -0.5	I hak	-0.14	side 2 Corres	mAdo
	6Au			15	VIN = 0 or 15V	-1.8		-1.5		-1.1		
			Com	5	V <sub>O</sub> = 4.6V, V <sub>IN</sub> = 0 or 5V V <sub>O</sub> = 9.5V,	-0.2	enidress peridress	-0.16	- MANG	-0.12		mAdc
	State of	90 90 120	9.1 9.0 9.0	10	V <sub>IN</sub> = 0 or 10V V <sub>O</sub> = 13.5V V <sub>IN</sub> = 0 or 15V	-0.5	1 × 191.50	-0.4	u Mil	-0.3 -1.0		
IN	Input	Current	Mil Comm	15 15	V <sub>IN</sub> = 0 or 15V V <sub>IN</sub> = 0 or 15V	Jugni- iroin	±0.1 ±0.3	01	±0.1 ±0.3	2893 290J	±1.0 ±1.0	μAdc μAdc
loz		e Output ge Current	Mil Comm	15 15	V <sub>IN</sub> = 0 or 15V V <sub>IN</sub> = 0 or 15V		±0.4 ±1.6	1 8	±0.4 ±1.6		±12 ±12	μAdc μAdc
CIN		Capacitance nit load	All	-	Any Input	CR A SC SS	101	ar	7.5			pF

#Applies for Worst Case input combinations.

# TABLE 2 - MOTOROLA FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

	Characteristic		Characteristic (1)		VDD	Tlow*		25	°C	Thigh*		Into J
Characteristic		Symbol	Vdc	Min	Max	Min	Max	Min	Max	Unit		
Output Voltage	"0" Level	VOL	5.0	910 90	0.05	707	0.05	-	0.05	Vdc		
V <sub>in</sub> = V <sub>DD</sub> or 0			10	1 10 1/8	0.05	21	0.05	-	0.05	T BU		
	"1" Level	VOH	5.0	4.95		4.95	-	4.95	-	Vdc		
Vin = 0 or VDD		ox I	10	9.95	* PA	9.95		9.95 14.95	4 egarlo	roit.		
Input Voltage B Types	"0" Level	VIL	13 13	14.33	> intl	14.55		14.95	-	Vdc		
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		60	5.0	2 -TWA	1.5	-	1.5	-	1.5			
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		0.0	10	- Tue	3.0	- Tr	3.0	-	3.0	1000		
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		200	15		4.0	1 =	4.0	-	4.0	1		
	"1" Level	VIH		531						Vdc		
(V <sub>O</sub> = 0.5 or 4.5 Vdc)			5.0	3.5	0 - TOV	3.5	Tesa	3.5	.50	bardo F		
(V <sub>O</sub> 1.0 or 9.0 Vdc)		1 1000	10	7.0	ar¥	7.0		7.0	Current	MARY !		
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		+	15	11.0	10 m 70 M	11.0	-	11.0				
Input Voltage UB Types	"O" Level	VIL	M	1000		101				Vdc		
(V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc)			5.0	-,578	1.0	-	1.0	-	1.0			
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		1 24	10	1000	2.0	1 01	2.0	-	2.0			
2000		-	15	-V6	2.5	-	2.5	-	2.5			
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	"1" Level	VIH		10		1				Vdc		
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		1 61	5.0	8.0	Dept.	8.0	-	4.0 8.0	-			
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		1 61	15	12.5	No.	12.5	_	12.5				

<sup>\*</sup>TLOW = -55°C for Military temperature range device, -40°C for Commercial temperature range device.

THIGH = +125°C for Military temperature range device, +85°C for Commercial temperature range device.

## ELECTRICAL CHARACTERISTICS

tieU				VDD	Tio	w°	25	C	Thi	ph°	
Charact	eristic		Symbol	Vdc	Min	Mex	Min	Max	Min	Max	Unit
Output Drive Current (AL)	B Gates	107	ІОН	12.0 T	001			PROPERTY.	STATE OF THE PARTY	atted or	mAde
(VOH = 2.5 Vdc)	Source			5.0	-3.0	-	-2.4	200	-1.7	2000	1877
(VOH = 4.6 Vdc)				5.0	-0.64	-	-0.51	-	-0.36	-	
(VOH = 9.5 Vdc)			-	10	-1.6	-	-1.3	40-0	-0.9	-	
(VOH = 13.5 Vdc)				15	-4.2	-	-3.4	-	-2.4	-	
(VOL = 0.4 Vdc)	Sink		IOL	5.0	0.64	-	0.51	-	0.36		
(VOL = 0.5 Vdc)			-	10	1.6	-	1.3	100 LA	0.9	WOT ILL	proced? (
(VOL = 1.5 Vdc)			F - 19	15	4.2	-	3.4	-	2.4	-	107 189)
Output Drive Current (CL/	(CP) B Gates		ІОН	97							mAd
(VOH = 2.5 Vdc)	Source		-	5.0	-2.5	-	-2.1	407-10	-1.7	-	
(VOH = 4.6 Vdc)			- 48	5.0	-0.52	-	-0.44	-	-0.36	-	
(VOH = 9.5 Vdc)			1	10	-1.3	-	-1.1	-	-0.9	-	
(VOH = 13.5 Vdc)				15	-3.6	-	-3.0	-	- 2.4	mu <del>d</del> mi	Detried.
(VOL = 0.4 Vdc)	Sink		IOL	5.0	0.52	Divie 1	0.44	79(4	0.36	R 104 DE	18 - W
(VOL = 0.5 Vdc)			-	10	1.3	vsq=(0)	1.1	128-,6	0.9	101 H <sup>C</sup> 81	The History
(VOL = 1.5 Vdc)				15	3.6	-	3.0	-	2.4	-	1
Output Drive Current (AL	) UB Gates		ГОН		1						mAd
(VOH = 2.5 Vdc)	Source		1	5.0	-1.2	_	-1.0	-	-0.7	- 1	111111111111111111111111111111111111111
(VOH = 4.6 Vdc)				5.0	-0.25	_	-0.2	-	-0.14	_	
(VOH = 9.5 Vdc)				10	-0.62	_	-0.5	-	-0.35	_	
(VOH = 13.5 Vdc)				15	-1.8	_	-1.5	_	-1.1	-	
(VOL = 0.4 Vdc)	Sink		IOL	5.0	0.64	_	0.51		0.36		
(VOL = 0.5 Vdc)	Ollik		100	10	1.6	_	1.3	_	0.9	_	
(VOL = 1.5 Vdc)				15	4.2	_	3.4	-	2.4	_	
Output Drive Current (CL)	(CP) LIB Gates		ГОН	-	1		-	-			mAd
(VOH = 2.5 Vdc)	Source		HO	5.0	-1.0	_	-0.8	_	-0.6	_	IIIAU
(VOH = 4.6 Vdc)	Source			5.0	-0.2		-0.16	_	-0.12		
(VOH = 9.5 Vdc)				10	-0.5		-0.4	_	-0.3	_	
(VOH = 13.5 Vdc)				15	-1.4	_	-1.2	_	-1.0	_	
(VOL = 0.4 Vdc)	Sink		la.	5.0	0.52	-	0.44	-	0.36	-	
(VOL = 0.5 Vdc)	SINK		IOL	10	1.3		1.1		0.9		
(VOL = 1.5 Vdc)				15	3.6		3.0	_	2.4	_	
	101 5			13	3.0		3.0		2.4		
Output Drive Current (AL)			ІОН	5.0	-0.64				-0.36	17.7	mAd
(V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc)	Source			10	-1.6		-0.51	_	-0.36		
(V <sub>OH</sub> = 13.5 Vdc)				15	-4.2		-3.4		-2.4		
	C:-1		-	-	-		-	-			1
(VOL = 0.4 Vdc)	Sink		IOL	5.0	0.64	-	0.51	-	0.36		
(VOL = 0.5 Vdc) (VOL = 1.5 Vdc)				15	1.6	-	3.4	-	0.9	-	
Output Drive Current (CL)	CDI Ost - D		1	15	4.2		3.4		2.4	_	-
		ces	ІОН	5.0	-0.52		-0.44		-0.36		mAd
(VOH = 4.6 Vdc)	Source			5.0	-1.3		-1.1	_	-0.9		
(V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)				15	-3.6		-3.0		-2.4	_	
	C:-1-		-	-	-		-				1
$(V_{OL} = 0.4 \text{ Vdc})$	Sink		IOL	5.0	0.52	-	0.44	-	0.36	-	11
(VOL = 0.5 Vdc)				10	1.3	-	1.1	-	0.9	-	
(VOL = 1.5 Vdc)				15	3.6	-	3.0	-	2.4	410	
Input Current (AL Device)			lin	15	-	±0.1	-	±0.1	-	±1.0	μAde
Input Current (CL/CP Dev	ice)		lin	15	-	±0.3	-	±0.3	-	±1.0	μAd
Input Capacitance			Cin	-	-	-	-	7.5	-		pF
(V <sub>in</sub> = 0)											
Gate Quiescent Current	(AL Device)	F177 18	IDD	5.0	-	0.25	-	0.25	-	7.5	μAd
(Per Package)				10	-	0.5	-	0.5	-	15	No solo
				15	-	1.0	-	1.0	-	30	
	(CL/CP Device	e)	IDD	5.0	-	1.0	-	1.0	-	7.5	
				10	-	2.0	-	2.0	-	15	E LE
				15	_	4.0	_	4.0	_	30	

		VDD	Tio	w°	25	o <sub>C</sub>	Thi	gh*	
Characteristic	Symbol	Vdc	Min	Max	Min	Max	Min	Max	Unit
Flip-Flop and Buffer Quiescent Current	 IDD	5.0	1000	1.0	-	1.0	6 E (TR.)	30	μAdo
(Per Package) (AL Device)	0.6-	10	HIST .	2.0	-	2.0	-	60	
1 - 1000-1 - 1000-1	100-1	15	-	4.0	-	4.0	-	120	
(CL/CP Device)	1 <sub>DD</sub>	5.0	-	4.0	-	4.0	-	30	μAdd
	5.4-1	10	-	8.0	-	8.0	-	60	
	1000	15	-	16	-	16	-	120	
MSI Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	5.0	-	150	μAdo
(Per Package)	2.8	8 10	-	10	-	10	-	300	
	-	15	Lar-	20	-	20	905	600	
(CL/CP Device)	1 <sub>DD</sub>	5.0	_	20	-	20	_	150	μAdd
	68.0 1	10	-	40	-	40	-	300	
	8.7-1	15	-	80	-	80	-	600	Mau
LSI Quiescent Current	IDD	31 ]		See	Individu	al Data S	heets.	13.5 V dc	"HOY!

<sup>\*</sup>Tlow = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

# HANDLING AND DESIGN GUIDELINES

## HANDLING PRECAUTIONS

All MOS devices trave insulated gates that are subject to voltage breakdown. The gate oxide for Molorota CAMOB overlose is about 800 Å shot side breaks down at a gate devices in about 800 Å shot side breaks gate and according breakdown from static discharge or other voltage insulationals. The profession entires shown in Figure 1 is

Static compand devices antisen in various server proventy pending on the severity of the demand. The most sproventy destroyed inputs are the eastest to destroyed serit be the structure of the post to vary the best to put the best companies of the vary of the structure of the vary of the structure of the present at the device no long resource respects to structure the deficult will be demanded input will be served on a structure of the vary structure of structure of the demander of the opening the post of the demander of the opening opening of the opening opening of the opening open

great deal of crisestion, CMOB devices are not immune to sarpe share veltage discharges that can be generated during handling actions painting static voltages generated by a particular walking actions a woxed floor have been measured in the 4.15 kV range (depending an humidity, surface conditions, sec.). Therefore, the following processors about

1. Do not exceed the Maximum Ratings specified by the

2. All unused device inputs should be connected to Vop.

3. All four imprehence equipment (pulse generators, etc.) should be connected to CMOS inputs only after lies

intual capacitiance. Note that maximum input rise and fee times should not be exceeded in Figure 2, bod fee possible natworld not be exceeded in Figure 2, to re-concern of the property of the reduce RSD (E) acrostatio (Dispharge) camage for to reduce RSD (E) acrostatio (Dispharge) camage for concernence, an equation for added propagation delay and rise time effects due to series received.

AR CMOS devices should be stored or transported in materials that are entistent. CMOS devices must not be inserted into conventional plastic "snow"; styrotosm or plastic ways, but should be left in their styrotosm, or plastic ways.

All CMOB devices should be placed on a grounded better a compared to the placed on a ground state and operators should ground them selves prior to handling devices, since a worker own selves prior to handling devices, the bench surface, Writt suepe in contact with skin are strongly recommended. See Flaure 3 for an exercise of a voice!

7. Appear or other static generaling materials should not

I. If automatic hearders are being used, high levels of staffic electricity may be generated by the novement of the device, the beha, or the boards. Reduce staffic building by setting federal of blowers or room tennicitiers. All parts of equitatines which come into contact with the top, bottom, or eden of 10 packages must be

 Cold oftenbers using CO<sub>2</sub> for cooling should be equipped with belies, and line CMOS devices must be contained on or in conductive material.

When lead-straightening or hand-soldering is necessary, provide ground shops for the apparatus used

d during wave

**CMOS Handling and Design Guidelines** 

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PIGURE 1 - JUNUT PROTECTION METHODS



# HANDLING AND DESIGN GUIDELINES

# HANDLING PRECAUTIONS

All MOS devices have insulated gates that are subject to voltage breakdown. The gate oxide for Motorola CMOS devices is about 800 Å thick and breaks down at a gate-source potential of about 100 volts. To guard against such a breakdown from static discharge or other voltage transients, the protection network shown in Figure 1 is used on each input to the CMOS device.

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged inputs are the easiest to detect because the input has been completely destroyed and is either shorted to Vpp, shorted to Vss, or open-circuited. The effect is that the device no longer responds to signals present at the damaged input. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Another effect of static damage is that the inputs generally have increased leakage currents.

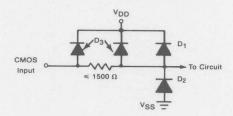
Although the input protection network does provide a great deal of protection, CMOS devices are not immune to large static voltage discharges that can be generated during handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4-15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed:

- Do not exceed the Maximum Ratings specified by the data sheet.
- All unused device inputs should be connected to V<sub>DD</sub> or V<sub>SS</sub>.
- All low-impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
- 4. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board are connected to an input of a CMOS device, a resistor should be used in series with the input. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. This is caused by the time constant formed by the series resistor and

input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 2, two possible networks are shown using a series resistor to reduce ESD (Electrostatic Discharge) damage. For convenience, an equation for added propagation delay and rise time effects due to series resistance size is given.

- 5. All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic "snow", styrofoam, or plastic trays, but should be left in their original container until ready for use.
- 6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 3 for an example of a typical work station.
- Nylon or other static generating materials should not come in contact with CMOS devices.
- 8. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to metal or other conductive material.
- Cold chambers using CO<sub>2</sub> for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
- When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
- 11. The following steps should be observed during wave solder operations:
  - The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
  - The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
  - Operators must comply with precautions previously explained.
  - d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.





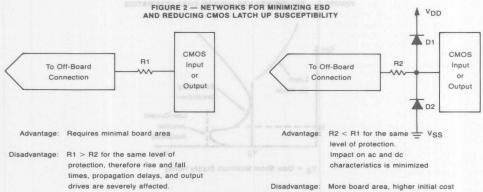
- 12. The following steps should be observed during board-cleaning operations:
  - a. Vapor degreasers and baskets must be grounded to an earth ground.
  - b. Brush or spray cleaning should not be used.
  - c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
- d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
- e. High velocity air movement or application of solvents and coatings should be employed only when assembled printed circuit boards are grounded and a static eliminator is directed at the board.
- 13. The use of static detection meters for production line surveillance is highly recommended.
- 14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules

- 15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
- 16. Double check test equipment setup for proper polarity of VDD and VSS before conducting parametric or functional testing.
- 17. Do not recycle shipping rails or trays. Repeated use causes deterioration of their antistatic coating.

# RECOMMENDED FOR READING:

"Total Control of the Static in Your Business"

Available by writing to: 3M Company Static Control Systems P.O. Box 2963 Austin, Texas 78769-2963 Or by Calling: 1-800-328-1368

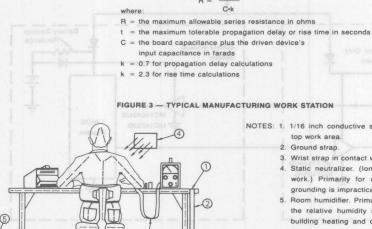


Note: These networks are useful for protecting the following

A digital inputs and outputs C 3-state outputs

B analog inputs and outputs D bidirectional (I/O) ports

# PROPAGATION DELAY AND RISE TIME vs. SERIES RESISTANCE



Resistor = 1 Megohm

- NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area.

  - 3. Wrist strap in contact with skin.
  - Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
  - 5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

# **POWER SUPPLIES**

CMOS devices have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS designs to be implemented using inexpensive, conventional power supplies, instead of switching power supplies and power supplies with cooling fans. In addition, batteries may be used as either a primary power source or for emergency backup.

The absolute maximum power supply voltage for 14000 Series Metal-gate CMOS is 18.0 Vdc. Figure 4 offers some insight as to how this specification was derived. In the figure, VS is the maximum power supply voltage and IS is the sustaining current of the latch-up mode. The value of VS was chosen so that the secondary breakdown effect may be avoided.

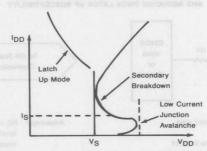
In an ideal system design, a power supply should be designed to deliver only enough current to insure proper operation of all devices. The obvious benefit of this type design is cost savings; an added benefit is protection

against the possibility of latch-up related failures. This system protection can be provided by the power supply filter and/or voltage regulator.

CMOS devices can be used with battery or battery backup systems. A few precautions should be taken when designing battery-operated systems:

- The recommended power supply voltage should be observed. For battery backup systems such as the one in Figure 5, the battery voltage must be at least 3.7 Volts (3 Volts from the minimum power supply voltage and 0.7 Volts to account for the voltage drop across the series diode).
- Inputs that might go above the battery backup voltage should either use a series resistor to limit the input current to less than 10 mA or use the MC14049UB or MC14050B high-to-low voltage translators.
- Outputs that are subject to voltage levels above VDD or below VSS should be protected with a series resistor to limit the current to less than 10 mA or with clamping diodes.





V<sub>S</sub> = Data Sheet Maximum Supply Rating

# FIGURE 5 - BATTERY BACKUP INTERFACE

Power Supply

Battery Backup
Recharge
System

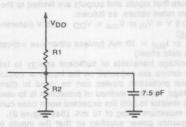
MC14049UB
MC14049UB
MC14050B

MC14050B

MC14050B

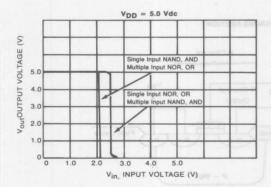
All inputs, while in the recommended operating range (VSS < Vin < VDD) can be modeled as shown in Figure 6. For input voltages in this range, diodes D1 and D2 are modeled as resistors, representing the reverse bias impedance of the diodes. The maximum input current is worst case, 1 $\mu A$ , when the inputs are at VDD or VSS, and VDD = 15.0 V. This model does not apply to inputs with pull-up or pull-down resistors.

FIGURE 6 - INPUT MODEL FOR VSS VIn VDD



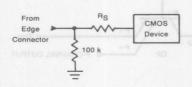
When left open-circuited, the inputs may self-bias at or near the typical switchpoint, where both the P-channel and N-channel transistors are conducting, causing excessive current drain. Due to the high gain of the inverters (see Figure 7), the device may also go into oscillation from any noise in the system. Since CMOS devices dissipate the most power during switching, this oscillation can cause very large current drain and undesired switching.

FIGURE 7 — TYPICAL TRANSFER CHARACTERISTICS FOR BUFFERED DEVICES



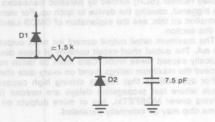
For these reasons, all unused inputs should be connected either to  $V_{DD}$  or  $V_{SS}$ . For applications with inputs going to edge connectors, a 100 kilohm resistor to  $V_{SS}$  should be used, as well as a series resistor for static protection and current limiting (Figure 8). The 100 kilohm resistor will help eliminate any static charges that might develop on the printed circuit board. See Figure 2 for other possible protection arrangements.

FIGURE 8 - EXTERNAL PROTECTION



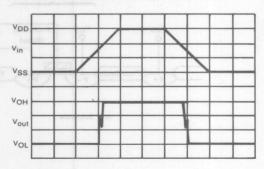
For input voltages outside of the recommended operating range, the CMOS input is modeled as in Figure 9. The resistor-diode protection network allows the user greater freedom when designing a worst case system. The device inputs are guaranteed to withstand voltages from VSS - 0.5 V to VDD + 0.5 V and a maximum current of 10 mA. With the above input ratings, most designs will require no special terminations or design considerations.

FIGURE 9 - INPUT MODEL FOR Vin > VDD or Vin < VSS



Other specifications that should be noted are the maximum input rise and fall times. Figure 10 shows the oscillations that may result from exceeding the 15  $\mu$ s maximum rise and fall time at  $V_{DD}=5.0~V,~5~\mu s$  at 10 V, or 4  $\mu s$  at 15 V. As the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input is amplified, and passed through to the output, causing oscillations. The oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed 15  $\mu$ s at 15 V, 5  $\mu$ s at 10 V, or 4  $\mu$ s at 15 V, Schmitt-trigger devices such as the MC14093B, MC14583B, MC14584B, MC14106B, HC14, or HC132 are recommended for squaring-up these slow transitions.

FIGURE 10 - MAXIMUM RISE AND FALL TIME VIOLATIONS



# **OUTPUTS**

All CMOS B-Series outputs are buffered to insure consistent output voltage and current performance. All buffered outputs have guaranteed output voltages of  $V_{\rm OL}=0.05$  V and  $V_{\rm OH}=V_{\rm DD}-0.05$  V for  $V_{\rm in}=V_{\rm DD}$  or VSS and  $I_{\rm out}=0~\mu{\rm A}.$  The output drives for all buffered CMOS devices are such that 1 LSTTL load can be driven across the full temperature range.

CMOS outputs are limited to externally forced output voltages of  $V_{\rm SS} - 0.5 \ V \le V_{\rm out} \le V_{\rm DD} + 0.5 \ V$ . When voltages are forced outside of this range, a silicon controlled rectifier (SCR) formed by parasitic transistors can be triggered, causing the device to latch up. For more information on this, see the explanation of CMOS Latch Up in this section.

The maximum rated output current for most outputs is 10 mA. The output short-circuit currents of these devices typically exceed these limits. Care must be taken not to exceed the maximum ratings found on every data sheet.

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETs), two or more outputs on the same chip may be externally paralleled.

# **CMOS LATCH UP**

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it

Figure 11 shows the cross-section of a typical CMOS inverter and Figure 12 shows the parasitic bipolar devices. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch up condition, transistors Q1 and Q2 are turned ON, each providing the base current necessary for the other to remain in saturation, thereby latching

the devices in the ON state. Unlike a conventional SCR, where the device is turned ON by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned ON by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than  $V_{\mbox{DD}}+0.5$  V or less than  $V_{\mbox{SS}}-0.5$  V and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below:

- Insure that inputs and outputs are limited to the maximum rated values, as follows:
  - $-0.5 \text{ V} \leq \text{V}_{in} \text{ or } \text{V}_{out} \leq \text{V}_{DD} + 0.5 \text{ V} \text{ (referenced to VSS)}$
  - $|I_{in} \text{ or } I_{out}| \le 10 \text{ mA}$  (unless otherwise indicated on the data sheet)
- If voltage transients of sufficient energy to latch up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the maximum rating of 10 mA. (See Figure 2).
- Sequence power supplies so that the inputs or outputs of CMOS devices are not active before the supply pins are powered up (e.g., recessed edge connectors and/or series resistors may be used in plug-in board applications).
- Voltage regulating or filtering should be used in board design and layout to insure that power-supply lines are free of excessive noise.
- Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

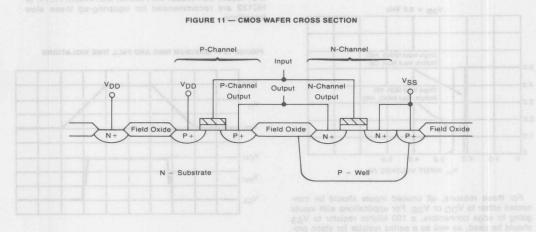
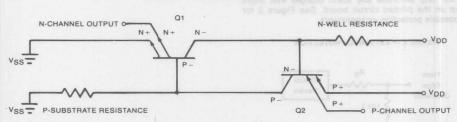


FIGURE 12 - LATCH UP CIRCUIT SCHEMATIC



**Data Sheets** 

Data Sheets 6



# MC14000UB

# **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL 3-INPUT "NOR" GATE PLUS INVERTER

L SUFFIX CERAMIC PACKAGE CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

# ORDERING INFORMATION

A Series: -55°C to +125°C

MC14XXXUBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXUBCP (Plastic Package) MC14XXXUBCL (Ceramic Package)

# **DUAL 3-INPUT "NOR" GATE PLUS INVERTER**

The MC14000UB dual 3-input NOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

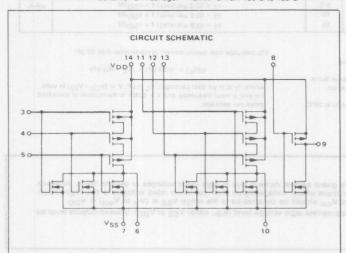
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
  - Pin-for-Pin Replacement for CD4000UB

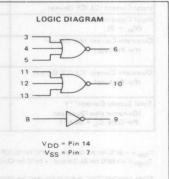
# MAXIMUM RATINGS\* (Voltages Referenced to VSS)

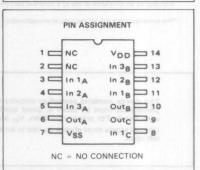
Symbol	Parameter	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/"C from 65°C to 85°C

Ceramic "L" Package: -12mW/"C from 100°C to 125°C







ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tic	w *	100	25°C		Th	igh *	VE
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	50	-	0.05	-	0	0.05	-	0,05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0		10	_	0.05	-	0	0.05	-	0.05	
· III · · DD · · ·		15	-	0.05	-	0	0.05	-	0.05	
Level	VOH	5.0	4.95	_	4.95	5.0	-	4.95	-	Vdc
Vin = 0 or V <sub>DD</sub>	011	10	9.95	-	9 95	10	-	9.95	-	
VIN - OUT VDD	San I	15	14.95	-	14.95	15	-	14.95	-	
Input Voltage "0" Level	VIL									Vdc
(Vo = 45 Vdc)	G.	50	-	1.0	-	2.25	1.0	-	1.0	- 112
(VO = 9.0 Vdc)		10	-	2,0	-	4.50	2.0	-	2.0	
(VO = 13.5 Vdc)		15	RETE	2.5	U 14 3	6 75	2.5	DAMES S	2.5	
"1" Level	VIH	1 -0	DO 21 357	ovini zui	ettes f	Out ruem	£ teub	BUCCON	ON set	
(V <sub>O</sub> = 0.5 Vdc)		5.0	4.0	egny Griffen	4.0	2 75	mail day 0	4.0	in Tues	Vdc
(VO = 1.0 Vdc)	H	10	8.0	_	8.0	5.50	-	8.0	-	
(V <sub>O</sub> = 1.5 Vdc)		15	12.5	smo <u>lo</u> mo	12.5	8.25	MUTTH OUT	12.5	B ULL SED	1950
Output Drive Current (AL Device)	ГОН	10	13/10 (10)	ndcent	marcher al	1 STEELERS	Day Auto	CARG DAY	257112 3	mAdo
(VOH = 2.5 Vdc) Source		50	-1.2	-	-1.0	-1.7	es residence	-0.7	nicezion i	pirt.
(VOH = 4.6 Vdc)		50	-0.25	_	-0.2	-0.36	1000	-0.14	- 0 Total	0
(VOH = 9.5 Vdc)		10	-0,62	-	-0.5	-0.9	213115 186	-0.35	-	
(VOH = 13.5 Vdc)		15	-1.8	-	-1.5	-3.5	E -agai	-1.1	V v <del>io</del> mus	
(VOI = 0.4 Vdc) Sink	IOL	50	0.64	_	0.51	0.88	11-000	0.36	w2 tion	mAdo
(VOL = 0.5 Vdc)	0.	10	1.6	_	1.3	2.25	_	0.9	-	
(VOL = 15 Vdc)		15	42	-	3.4	8.8	et agente	2.4	9-102-113	8
Output Drive Current (CL/CP Device)	ГОН									mAdo
(VOH = 25 Vdc) Source	. A	5.0	-1.0	-	-0.8	-1.7	-	-0.6	_	1
(VOH = 4.6 Vdc)		50	-0.2	-	-0.16	-0.36	-	-0.12	-	
(VOH = 9.5 Vdc)		10	-0.5	-	-0.4	-0.9	-	-0.3	-	
(VOH = 13.5 Vdc)	10	15	-1.4	-	-1.2	-3.5	-	-1.0	-	1
(VOI = 0.4 Vdc) Sink	OL	5.0	0.52	-	0.44	0.88	_	0.36	_	mAdd
(VOL = 0.5 Vdc)		10	1.3	-	1.1	2 25	Hages Hy	09	HTAR N	DAGE NO.
(VOL = 1 5 Vdc)		15	3.6	-	3.0	88	SISSETT SETA	24	-	Toda
Input Current (AL Device)	In	15	0.67	±0.1		± 0.00001	± 0.1	4075000	±1.0	"Add
Input Current (CL/CP Device)	lin	15	-	±0.3		± 0.00001	± 0.3	-	±1.0	μAdo
Input Capacitance	Cin		-	-	1 -	50	7.5	-	_	pF
$(V_{in} = 0)$					uta sed	Resident		muD fland	C to mo	Lino
Quiescent Current (AL Device)	1pp	50	_ 10	0.25	-	0.0005	0.25	0.10089	7.5	иAdd
(Per Package)	00	10	100	0.50	-	0.0010	0.50	1001 <del>-0</del> 007	15.0	
The State of		15	-	1.00	-	0.0015	1.00	-	30.0	1
Quiescent Current (CL/CP Device)	IDD	5.0		1.0	1 -	0 0005	1.0	_	7.5	μAιdo
(Per Package)	00	10	and Auto	2.0	or ogsa	0.0010	2.0	No Beaut	15.0	100
		15	ON	4.0	1000	0.0015	4.0	STRIBLES	30.0	permute
Total Supply Current**†	IT	50			IT =	(0.3 µA/kHz	) f + Ipp	/N		uAd.
(Dynamic plus Quiescent,		10				10.6 µA/kH2				
Per Gate, C <sub>1</sub> = 50 pF)		15	1			(0.8 µA/kH2				1

 $^*T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_{T}$  is in  $\mu$ A (per package),  $C_{L}$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and  $k=0.001\times the$  number of exercised gates per package.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

Characteristic	S	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise Time		tTLH					ns
tTLH = (3.0 ns/pF) CL + 30 ns			5.0	-	180	360	
tTIH = (1.5 ns/pF) CI + 15 ns		4-1	10		90	180	and delivery to
tTLH = (1.1 ns/pF) CL + 10 ns			15	-	65	130	
Output Fall Time	937	THL	iten pa	aran wa	30319.0		ns
t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	644	MEL OF	5.0	NAME NO	100	200	1 3 1 1
t <sub>THI</sub> = (0.75 ns/pF) C <sub>I</sub> + 12.5 ns			10	- 1	50	100	
t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns			15	-	40	80	
Propagation Delay Time	Stor (Stormeller a), profe-	tPLH.	DESCRIPTION OF STREET	May and S	alles alfa	o depued	ns
tpLH tpHL = (1.7 ns/pF) CL + 30 ns	-midwogj Ashtonija	tPHL	5.0	a s_ni s	115	230	hancel
tpLH, tpHL = (0.66 ns/pF) CL + 22 ns	the state of the s	WO 979	10	r yasmin	55	110	Cosm
tpLH, tpHL = (0.50 ns/pF) CL + 15 ns			15	ab = yan	40	80	o\bns

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MOM MIGHE OF FIGURE 1 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

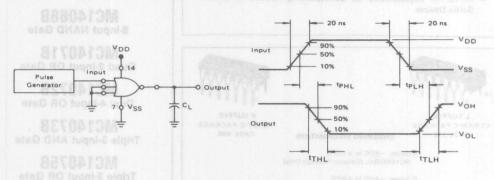


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

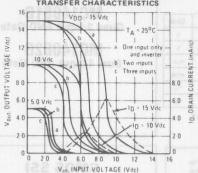
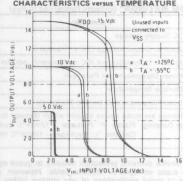


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE



#### **B-SUFFIX SERIES CMOS GATES**

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices



L SUFFIX
CERAMIC PACKAGE
CASE 632



PLASTIC PACKAGE

ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur †Temperature Derating. Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \equiv (V_{in} \text{ or } V_{out}) \equiv V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

MC14001B Quad 2-Input NOR Gate

MC14002B Dual 4-Input Nor Gate

MC14011B Quad 2-Input NAND Gate

MC14012B Dual 4-Input NAND Gate

MC14023B Triple 3-Input NAND Gate

MC14025B Triple 3-Input NOR Gate

> MC14068B 8-Input NAND Gate

MC14071B Quad 2-Input OR Gate

MC14072B Dual 4-Input OR Gate

MC14073B

Triple 3-Input AND Gate

MC14075B Triple 3-Input OR Gate

> MC14078B 8-Input NOR Gate

MC14081B Quad 2-Input AND Gate

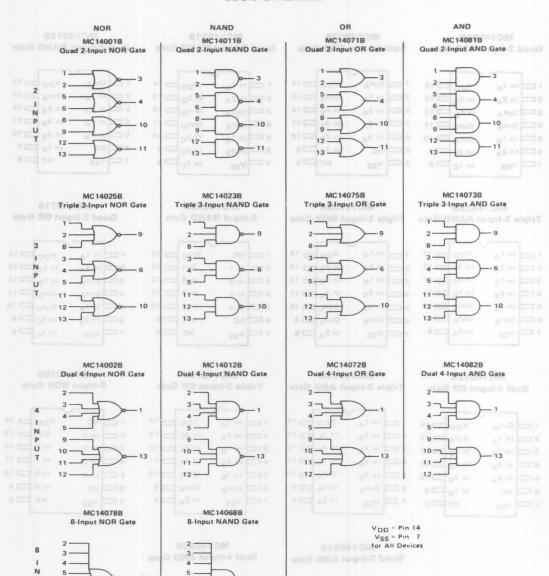
MC14082B Dual 4-Input AND Gate

**CMOS SSI** 

(LOW-POWER COMPLEMENTARY MOS)

**B-SERIES GATES** 

#### LOGIC DIAGRAMS



.

9 -

10 -

11 -

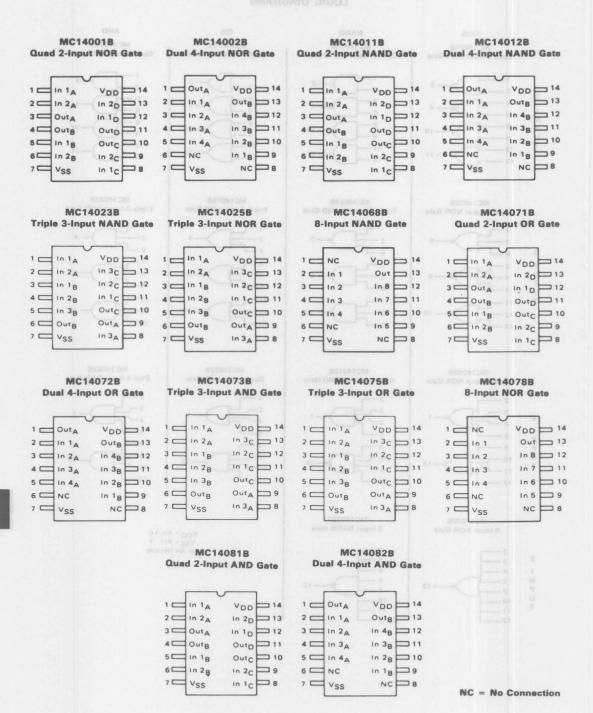
9 -

10.

11.

U

#### PIN ASSIGNMENTS



FLECTRICAL CHARACTERISTICS (Voltages Referenced to Vos)

		VDD	Tic	w °		25°C		Thi	gh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0		0.05	THE PERSON	0	0.05	T. Holling	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	4	0 05		0	0.05		0.05	
THE TOP OF THE PARTY	400	15		0.05		0	0.05	ataexad2s	0.05	LTBCK.
"1" Level	VOH	50	4.95		4.95	5.0		4 95		Vdc
	·OH	10	9.95	NAME OF THE OWNER, OF THE OWNER, OF THE OWNER, OF THE OWNER, OWNER, OWNER, OWNER, OWNER, OWNER, OWNER, OWNER,	9.95	10		9.95		POGRED HST
V <sub>in</sub> = 0 or V <sub>DD</sub>		15	14.95		14.95	15		14.95		1133
nput Voltage "0" Level	VIL	-						1 7 1 1	ekan Ob G	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	1.0	5.0		1.5		2.25	1.5		1.5	
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$		10		3.0		4.50	3.0	42.8 HA	3.0	eugra O
$(V_0 = 13.5 \text{ or } 1.5 \text{ Vdc})$		15		40		6.75	4.0	13-10-19	4.0	1 1147
"1" Level	VIH			10		0.10	am 0	F F 10 14	gian 00 0	- JE13
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	VIH	5.0	3.5		3.5	2.75		3.5	alen 95 01	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	La ciamania de	7.0	5 50		7.0		
$(V_0 = 1.5 \text{ or } 13.5 \text{ Vdc})$		15	11.0	THE SERT	11.0	8 25		11.0	rioti Dainy	PROPER
0		13	11.0		11.0	0.25	- plan	No. of Parties	M. BACKS	mAde
Output Drive Current (AL Device)	ОН		30		2.4	40.08 4		08.01 ×	HERP VILLE	MAGG
(V <sub>OH</sub> = 2.5 Vdc) Source	E - 1	5 0			2.4	-4.2	134 July	-1.7	Hab_HT,	
$(V_{OH} = 4.6 \text{ Vdc})$	-	5.0	0.64		-0.51	-0.88	JOH Rule	0.36	BHFHJ	1
$(V_{OH} = 9.5 \text{ Vdc})$		10	4.2	-	-1.3	-2.25	mus D tu	-0.9	E S 1901	HA
$(V_{OH} = 13.5 \text{ Vdc})$		15	4.2	-	- 3.4	-8.8	J17 Buts	2.4	asant in h	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0 64	-	0.51	0.88	104 3q/a	0.36	349-447	mAde
$(V_{OL} = 0.5 \text{ Vdc})$		10	16	1	13	2.25	304 gala	0.9	584-187	1
$(V_{OL} = 1.5 \text{ Vdc})$		15	4.2	1	3 4	8.8	DATES.	2.4	Select Au	gn1-8
Output Drive Current (CL/CP Device)	ГОН		98			an dell's	JJ Plat	(dSD) =	DHW ART	mAd
(VOH = 2.5 Vdc) Source		5.0	2.5		-2.1	4.2		1.7	JEFF - HJ	
(V <sub>OH</sub> = 4.6 Vdc)		50	0.52		-0.44	-0.88		-0.36	进程, 上了	
(V <sub>OH</sub> = 9.5 Vdc)		10	1.3	-	-1.1	-2.25		-0.9		-
$(V_{OH} = 13.5 \text{ Vdc})$		15	- 3.6		-3.0	8.8		2.4	percip stilun	ned and
(V <sub>OL</sub> = 0.4 Vdc) Sink	10L	5.0	0.52		0.44	0.88	of Second and	0.36	With building	mAd
$(V_{OL} = 0.5 \text{ Vdc})$	.00	10	13		1.1	2 25		0.9	ori ros-se En	internet
(V <sub>OL</sub> = 1.5 Vdc)		15	3 6		3.0	8.8		24		
Input Current (AL Device)	1,0	15	0 DE 10 18	+01	PERSONAL PROPERTY.	±0 00001	.01		110	μAd
Input Current (CL/CP Device)	-	15	+	+03	-	±0 00001	+03		110	μAd
	lin		1	1.03				-	110	-
Input Capacitance	Cin	20 32	-			5.0	7.5			pF
(V <sub>in</sub> = 0)				1						
Quiescent Current (AL Device)	IDD	5 0	1	0.25		0.0005	0 25		7.5	μAd
(Per Package)	00	10		0.50		0.0010	0.50		15.0	1
	all In-	15		1.00		0.0015	1.00		30.0	
Quiescent Current (C1 /CP Device)	'pp	50		1.0		0.0005	1.0		7.5	μAd
(Per Package)		10	1	2.0	1 7 19	0.0010	2.0		15.0	1.1
		15		4.0	10.0	0.0015	4.0	. 2000	30.0	1 18
Total Supply Current**†	IT	50		af-	IT =	(0.3 µA/kH;	z) f + Ipp	/N		μAd
(Dynamic plus Quiescent)	The state of	10			The second second	(0.6 μA/kH:				L'AC
Per Gate, C <sub>1</sub> = 50 pF)	-10-to-y	15				(0.9 μA/kH.	The second second			
		1	A Charles		- 11 -	10.5 μΑ/ΚΠ.		,	JOHN THE PROPERTY OF THE PARTY	

 $<sup>^{*}</sup>T_{low}$  = -55°C for AL Device. -40°C for CL/CP Device.  $T_{high}$  = +125°C for AL Device. +85°C for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 pF) + (C_L - 50) Vfk$$

where IT is in  $\mu$ A (per package),  $C_L$  in pF.  $V=\{V_{DD}-V_{SS}\}$  in volts, fin kHz is input frequency, and  $k=0.001\times$  the number of exercised gates per package

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

#### **B-SERIES GATE SWITCHING TIMES**

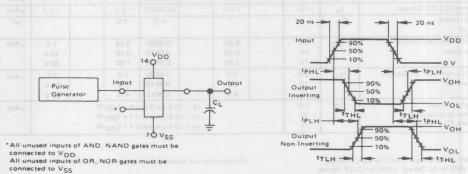
# SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

Characteristic (	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise Time, All B-Series Gates <sup>†</sup> TLH = (1.35 ns/pF) C <sub>L</sub> + 33 ns	E TLH	5.0	1107	100	200	o o ns
tTLH = (0.60 ns/pF) C <sub>L</sub> + 20 ns tTLH = (0.40 ns/pF) C <sub>L</sub> + 20 ns		10	The same	50 40	100	enov man
Output Fall Time, All B-Series Gates	<sup>t</sup> THL	01			9 0 or 1 0 Ve	ns
tTHL = (1.35 ns/pF) CL + 33 ns	0.6	5.0		100	200	- OVI
<sup>†</sup> THL = (0.60 ns/pF) C <sub>L</sub> + 20 ns		10	145V	50	100	
THL = (0.40 ns/pF) C <sub>L</sub> + 20 ns	I as I	15 08	-	40	80	= 6V0
Propagation Delay Time MC14001B, MC14011B only	tPLH, tPHL	0.11 E1		106	7 6 81 10 6 I	ns
tpLH, tpHL = (0.90 ns/pF) CL + 80 ns		5.0	80	125	250	The reality
tpLH, tpHL = (0.36 ns/pF) CL + 32 ns	1 2 1	10	-	50	100	HOT
tpLH, tpHL = (0.26 ns/pF) CL + 27 ns	1 20-1 - 1	15	-	40	80	KO.
All Other 2, 3, and 4 Input Gates		81-1 01			1000 000	HOV
tplH, tpHL = (0.90 ns/pF) C1 + 115 ns		5.0	-	160	300	HOV
tpLH, tpHL = (0.36 ns/pF) CL + 47 ns	1 180	10 0 0	0	65	130	- 30 W
tpLH, tpHL = (0.26 ns/pF) CL + 37 ns		15	1 -	50	100	- 10 A:
8-Input Gates (MC14068B, MC14078B)	N.E.	12 1 62			I S Vaci	E 10/41
tpLH, tpHL = (0.90 ns/pF) CL + 155 ns		5.0	100	200	350	Jugged Dr
tpLH, tpHL = (0.36 ns/pF) CL + 62 ns	100	10 00	-	80	150	HOY)
tpLH, tpHL = (0.26 ns/pF) CL + 47 ns	1 10 0	15	-	60	110	WOY!

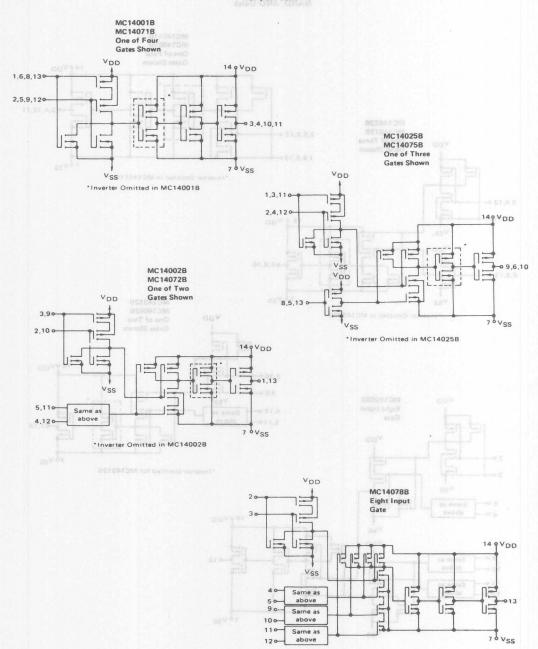
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

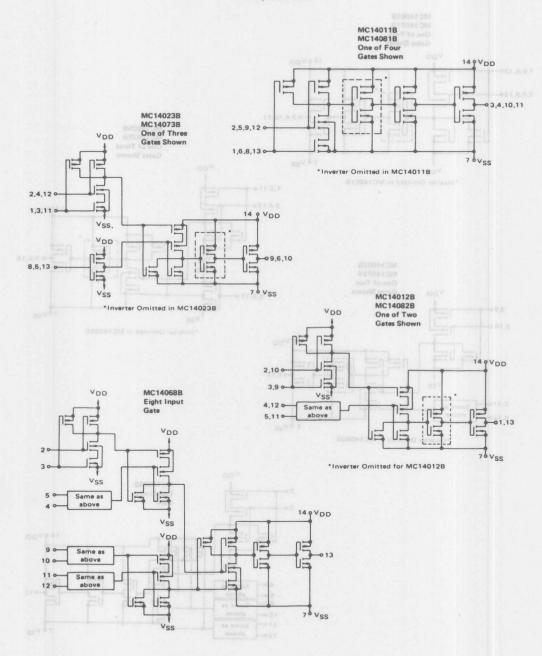
### FIGURE 1 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



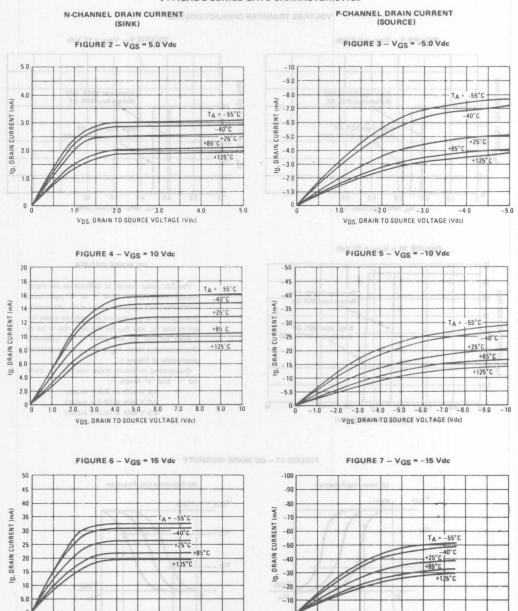
CIRCUIT SCHEMATIC
NOR, OR Gates



#### CIRCUIT SCHEMATICS NAND, AND Gates



#### TYPICAL B-SERIES GATE CHARACTERISTICS



These typical curves are not guarantees, but are design aids.

Caution: The maximum rating for output current is 10 mA per pin.

VDS. DRAIN-TO-SOURCE VOLTAGE (Vdc)

-2.0

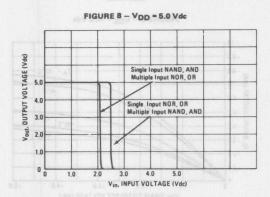
-6.0 -8.0

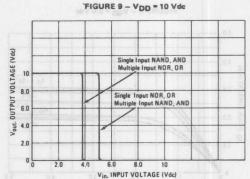
-10 -12 -14 -16

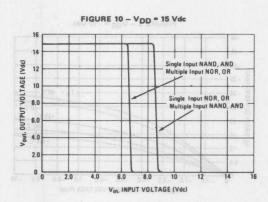
VDS. DRAIN-TO-SOURCE VOLTAGE (Vde)

#### TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

# VOLTAGE TRANSFER CHARACTERISTICS







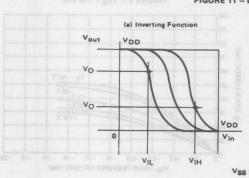
#### DC NOISE MARGIN

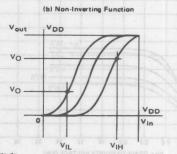
The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values V $_{\rm IL}$  and V $_{\rm IH}$  for the output(s) to be at a fixed voltage V $_{\rm O}$  are given in the Electrical Characteristics table. V $_{\rm IL}$  and V $_{\rm IH}$  are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

1.0 V with a 5.0 V supply 2.0 V with a 10.0 V supply 2.5 V with a 15.0 V supply

#### FIGURE 11 - DC NOISE IMMUNITY





Vss = 0 volts dc



#### **UB-SUFFIX SERIES CMOS GATES**

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000
   Series UB Suffix Devices

MC14001UB Quad 2-Input NOR Gate

MC14002UB
Dual 4-Input NOR Gate

MC14011UB Quad 2-Input NAND Gate

MC14012UB
Dual 4-Input NAND Gate

MC14023UB
Triple 3-Input NAND Gate

MC14025UB Triple3-Input NOR Gate

# CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

UB-SERIES GATES

# MC14011UB MC14002UB MC14001UB Quad 2-Input NAND Gate **Dual 4-Input NOR Gate** Quad 2-Input NOR Gate - 10 10 12 12. 12 -13 -MC14023UB MC14025UB MC14012UB Triple 3-Input NAND Gate Triple 3-Input NOR Gate **Dual 4-Input NAND Gate** 12-

VDD = Pin 14

VSS = Pin 7

for All Devices

LOGIC DIAGRAMS





L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX
PLASTIC PACKAGE
CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXUBAL (Ceramic Package Only)

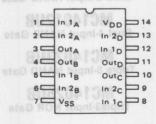
C Series: -40°C to +85°C MC14XXXUBCP (Plastic Package) MC14XXXUBCL (Ceramic Package)

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

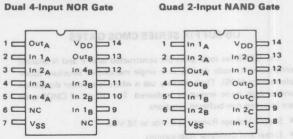
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

### PIN ASSIGNMENTS

#### MC14001UB Quad 2-Input NOR Gate



	MC140	02UB	
Dual	4-Input	NOR	Gate



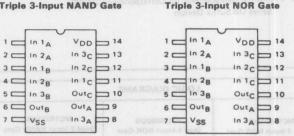
MC14011UB

MC14025UB

MC14012UB **Dual 4-Input NAND Gate** 



MC14023UB **Triple 3-Input NAND Gate** 



NC = No Connection

......

Symbol	EL-LOW.	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Vo	ltage	-0.5 to +18.0	٧
Vin. Vout	Input or Outp	ut Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. lout	Input or Outp	ut Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipa	ation, per Package†	500	mW
T <sub>stg</sub>	Storage Temp	erature	-65 to +150	°C
TL	Lead Temper	ature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C to annuls of goal broke of research and second areas Ceramic "L" Package: -12mW/°C from 100°C to 125°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to Vos)

		VDD	Tic	w°		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Lev	el VOL	5.0		0.05	-	0	0.05	-	0.05	Vdc
	0.	10	1 1	0.05	-	0	0.05	10 F36W	0.05	ni .
V <sub>in</sub> = V <sub>DD</sub> or 0		15		0.05	-	0	0.05	10 FRatis	0.05	177
	el VOH	5.0	4.95	-	4.95	5.0	so 91	4 95	11.12 × H	Vdc
	- VOH	10	9.95	-	9.95	10		9.95	and Tester	venvo
$V_{in} = 0 \text{ or } V_{DD}$		15	14.95	SITI	14.95	15	1= 8S	14.95	18.71 - 1	277
200		13	14.55	-	14.00	13	J. 2 C F 4	10 LTIME	27.01 = 3	Vdo
Input Voltage "0" Lev	el V <sub>IL</sub>			1.0	- 12	2.26	1.0	D (20)se	1.0	Vac
(V <sub>O</sub> = 4.5 Vdc)		50		2.0		2.25	2.0	Commence of the last	2.0	100
$(V_O = 9.0 \text{ Vdc})$		10	286	2.5		4.50	2.5	SMUT S	2.5	SEGOTS
(V <sub>O</sub> = 13.5 Vdc)		15	-	2.5	-	6 75				100
Day "1" Lev	el VIH					\$0.25	+ 13.13	(0.85 ac/	18(97.3	(psp)
$(V_O = 0.5 \text{ Vdc})$	-	5.0	4.0	1	4.0	2.75	9 ,019	4.0	114.51	Vdc
(V <sub>O</sub> = 1.0 Vdc)		10	8.0	-	8.0	5.50		8.0	week as her	The follow
(V <sub>O</sub> = 1.5 Vdc)		15	12.5	-	12.5	8.25	-	12.5	-	1
Output Drive Current (AL Device)	10Н				800 8000	Rig agreeb v	ol bacu ed	in top at 19	palled Ty	mAd
(VOH = 2.5 Vdc) Source		5.0	-1.2	-	-1.0	-1.7	oq.=0) e	-0.7	ed na-en b	obcoppid.
(VOH 4.6 Vdc)		5.0	-0.25	-	-0.2	-0.36		-0.14	-	
(VOH = 9.5 Vdc)		10	-0.62	-	-0.5	-0.9		-0.35	-	
(VOH = 13.5 Vdc)	2005 D T T V G 100 A	15	-1.8	BURT OF	-1.5	-3.5	49-	-1.1	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64		0.51	0.88	-	0.36		mAd
(V <sub>OL</sub> = 0.5 Vdc)	·OL	10	1.6	-	1.3	2.25	_	0.9		
(VOL = 1.5 Vdc)		15	4.2	_	3.4	8.8	_	2.4		
	-\	1.5	7.2	-	-	-		-		mAd
Output Drive Current ICL/CP Devic	e) IOH	50	-1.0		-0.8	-1.7		-0.6		mAd
(VOH = 2.5 Vdc) Source		5.0	-0.2		-0.16	-0.36		-0.12	-	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.5	-	-0.4	-0.9	-	-0.12		
(V <sub>OH</sub> = 9.5 Vdc)	366-2	10	-1.4	-	-1.2	-3.5	1 19	-1.0		
(V <sub>OH</sub> = 13.5 Vdc)		15		-	-		-	-		-
(VOL = 0.4 Vdc) Sink	OL	5.0	0.52	0	0.44	0.88	-0-	0.36	many -	mAde
(VOL = 0.5 Vdc)	Transfer I	10	1.3		1.1	2.25	-	0.9	-	
(VOL = 1.5 Vdc)		15	3.6	- 1	3.0	8.8	0-	24		
Input Current (AL Device)	Lin	15		±01		+0 00001	:01	-	.10	μAdd
Input Current (CL/CP Device)	lin	15		± 0.3		+0.00001	:03		:10	μAdd
Input Capacitance	C <sub>in</sub>	_	-		1	5.0	7.5			pF
(V <sub>in</sub> = 0)	-in					2 158 8 1015		100	N 67 Switz	10000
Quiescent Current (AL Device)	1	5.0		0.25	1	0.0005	0 25	1000	7.5	μAde
(Per Package)	IDD	10		0.25		0.0005	0.50	- 8	15.0	HAU
i ei i ackagei		15		1.00		0.0015	1.00		30.0	
			-	-	-	-		-		-
Quiescent Current (CL/CP Device)	1DD	50	- 1	1.0	-	0.0005	1.0		7.5	μAd
(Per Package)		10	-	2.0		0.0010	2.0	o aŭreo	15.0	
DIT Alestide TIUO	OUT OF TAXABLE STORY	15		4.0		0.0015	4.0		30.0	
Total Supply Current**†	TIME	5 0				(0.3 µA/kH				μAd
(Dynamic plus Quiescent,		10			IT =	10.6 µA/kH	t) f + IDD	/N		
Per Gate, CL = 50 pF)	300	15				(0.8 µA/kH				

\*T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and  $k=0.001\times the$  number of exercised gates per package.

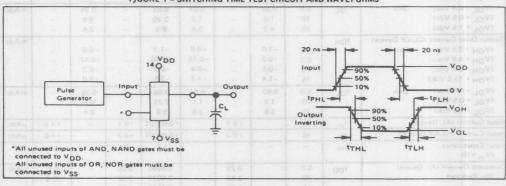
SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

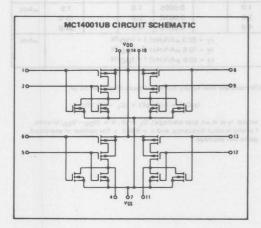
Characteristic			Symbol	V <sub>DD</sub> Vdc	Min	Typ#	Max	Unit
Output Rise Time	9		tTLH	D.C.	100	19992 0	608	ns
tTLH = (3.0 ns/pF) CL + 30 ns			0.00	5.0	-	180	360	CHRY - UKA
tTLH = (1.5 ns/pF) CL + 15 ns			89.0	10		90	180	
tTLH = (1.1 ns/pF) CL + 10 ns			- 20	15	He'V	65	130	
Output Fall Time tTHL = (1.5 ns/pF) C <sub>L</sub> + 25 ns	Q1	8.60 14.95	THL	5.0		100	200	ns
tTHL = (0.75 ns/pF) C1 + 12.5 ns				10	_v	50	100	enteV hum
tTHL = (0.55 ns/pF) CL + 9.5 ns			0.1	15	-	40	80	A OV
Propagation Delay Time	00.4	-01	tPLH, tPHL	100			435X-	ns
tpLH, tpHL = (1.7 ns/pF) CL + 30	ns		0.5	5.0	-	90	180	FI - WAL
tpLH, tpHL = (0.66 ns/pF) CL + 22				10	Lev l	50	100	
tpLH, tpHL = (0.50 ns/pF) CL + 15	ns		- 0	15	_	40	80	0 - 0 A)

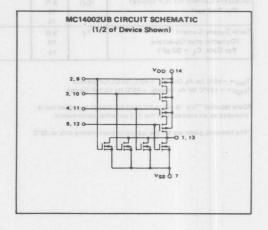
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

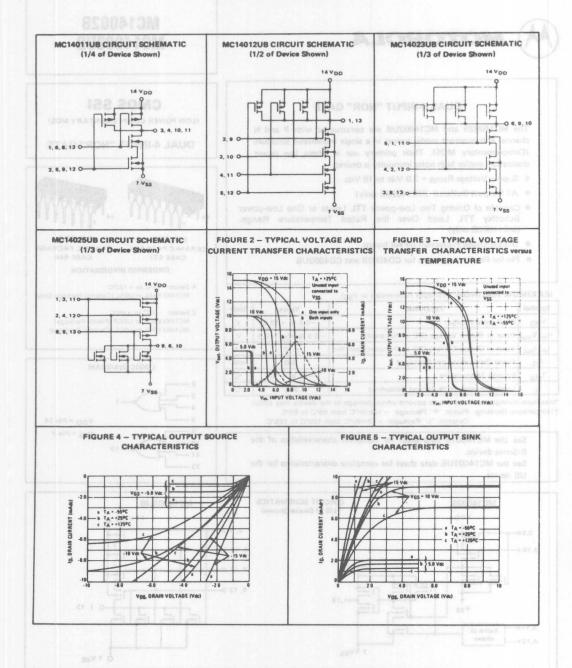
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FJGURE 1 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS









# MC14002B MC14002UB

#### **DUAL 4-INPUT "NOR" GATE**

TOS UB-SERIES GATES

The MC14002B and MC14002UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14002B only)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14002B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4002B and CD4002UB

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

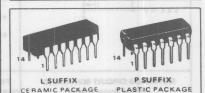
See the MC14001B data sheet for complete characteristics of the B-Series device.

See the MC14001UB data sheet for complete characteristics for the UB device.

### **CMOS SSI**

(LOW POWER COMPLEMENTARY MOS)

**DUAL 4-INPUT "NOR" GATE** 



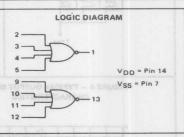
ORDERING INFORMATION

CASE 632

A Series: -55°C to +125°C
MC14XXXBAL or UBAL (Ceramic Package Only)

**CASE 646** 

C Series: -40°C to +85°C MC14XXXBCP or UBCP (Plastic Package) MC14XXXBCL or UBCL (Ceramic Package)



CIRCUIT SCHEMATICS MC14002B MC14002UB (1/2 of Device Shown) VDD 14 VDD Q 2,90 3, 10 0-149VDD 4, 11 0 5. 12 0-Same as above 4,12 7 VSS 0 7 VSS

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For

proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



18-BIT STATIC SHIFT REGISTER

The MC14006B shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in

Output Transitions Occur on the Falling Edge of the Clock Pulse

Capable of Driving Two Low-power TTL Loads or One Low-power

Can be Cascaded to Provide Longer Shift Register Lengths

Schottky TTL Load Over the Rated Temperature Range

# MC14006B

### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

18-BIT STATIC SHIFT REGISTER





L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX PLASTIC PACKAGE CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### MAXIMUM RATINGS\* (Voltages Referenced to Vee)

• Pin-for-Pin Replacement for CD4006B

serial shift registers and time delay circuits.

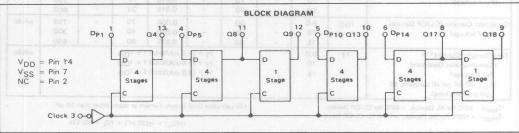
Supply Voltage Range = 3.0 Vdc to 18 Vdc

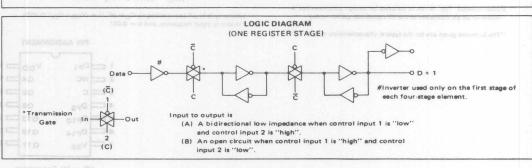
Fully Static Operation

Symbol	- 88.0 - Parameter 88.0 - 45.0 - 1	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	Oly
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C TRUTH TABLE (Single Stage)







to Charles and American and American		VDD	Tio	w*		25°C		Thi	gh*	1
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0		0.05	-	0	0.05	-	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0		10	-	0.05	-	0	0.05	-	0.05	
CONTRACTOR STREET, STR		15	-	0.05	Hoge	0	0.05	Tia-si	0.05	
"1" Level	VOH	5.0	4.95	Your ses	4.95	5.0		4.95		Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	OH	10	9.95	tas anda	9.95	10	espen at	9.95	1 2010 511	
AIU - O OL ADD	or the second	15	14.95	molycae	14.95	15	00 E gn	14.95	Hatte had	1995
nput Voltage "0" Level	VIL		1	- Turpus	100 100 10	1370F 1371	MARK 515	STREET, UK	C 1000 20	Vdc
(VO = 4.5 or 0.5 Vdc)	10	5.0	ME E UIE	1.5	fisson ti	2.25	1.5	MILL br	1.5	SHI
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	gorges y	3.0	101 31	4.50	3.0	S & 9,	3.0	253
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	Duffugliz vi	4:0	12i 250	6.75	4.0	recal to	4.0	955
"1" Level	VIH				181	units Yelf	Demis b	tis eve ciri	sit Platte la	1052
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	-111	5.0	3.5	mile how	3.5	2.75	vienO.	3.5	Turnerol	Vdc
(Vo = 1 0 or 9 0 Vdc)		10	7.0	_	7.0	5.50	Harmer	7.0		
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	_ mai	11.0	udy Sun	0
Output Drive Current (AL Device)	ГОН		0110	RIBLI 124	11.0	0.20	SERVICE TO	11.0	8.J-50 r-6.	mAd
(V <sub>OH</sub> = 2.5 Vdc) Source	тОН	5.0	-3.0	_	-2.4	-4.2	E = sen	-1.7	N same	IIIAU
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	y set site	-0.51	-0.88	d swit	-0.36	17-11-11	
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6		-1.3	-2.25	7002011250702	-0.9	eltaca	7 18
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	tisET and	-3.4	-8.8	ST TOVE	-2.4	Asouth 12	
The first of the comment of the comm	1-	5.0	0.64		0.51	0.88	of mem	0.36	PENDENI	mAd
(VOL = 0.4 Vdc) Sink	IOL	10	1.6	-	1.3	2.25		0.36		mAd
(VOL = 0.5 Vdc)		15	4.2	-	3.4	8.8		2.4	_	
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	0.0	-	2.49		-
Output Drive Current (CL/CP Device)	ІОН		0.5		0.1	10	P associates	*250	COAR NO	mAd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2		-1.7	-	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52		-0.44	-0.88	of the street of the	-0.36	-	foots
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	10-	-1.1	-2.25	_	-0.9	Ingged as	- 00
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8		-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52		0.44	0.88	-	0.36	-	mAd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3	-	1.1	2.25	100	0.9	O volument	100
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8	64KEP 19	2.4	NIG Tales	100
input Current (AL Device)	lin	15	9215 pt	± 0.1	-	±0.00001	±0.1	ator Tourse	± 1.0	μAdo
nput Current (CL/CP Device)	lin	15	- Totals	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdo
Input Capacitance	Cin	_			-	5.0	7.5	-		pF
(Vin = 0)			DI YEAR DE	evely urfl	of ngama	ricertie las	oried assur	W 880-6	na apiral	mumi
Quiescent Current (AL Device)	Ipp	5.0		5.0	0.000	0.005	5.0	-	150	μAde
(Per Package)	.00	10	THE RE	10	-	0.010	10	-	300	
		15	ALT NO	20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20		150	μAde
(Per Package)	יטטי	10	-	40		0.005	40		300	има
		15	-	80	- ans	0.010	80	1972	600	
Total Supply Current**†	1=	5.0	-	00	1 11				600	
(Dynamic plus Quiescent,	IT g	10	1 40			.3 μA/kHz)				μAdd
Per Package)	1 .	15				2.6 µA/kHz)				GOY
(C <sub>1</sub> = 50 pF on all outputs, all	100212	15	PONTS		1T = (3	1.9 µA/kHz)	סטי + ז			SSA
buffers switching)	10/0/15									7391

<sup>\*</sup>Tlow = -55°C for AL Device, -40°C for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ V.f.k}$ 

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD-V\_SS) in volts. If in kHz is input frequency, and k = 0.001

\*\*The formulas given are for the typical characteristics only at 25°C.

1 - DP1 VDD 14 2 - NC 04 13 3 🗆 C 09 12 Q8 11 4 CDP5 5 - DP10 013 10 6 - DP14 0.18 9 7 - VSS 017 8

PIN ASSIGNMENT

NC = No Connection

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#### SWITCHING CHARACTERISTICS\* (C<sub>1</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time  ttlH. ttHL = (1.5 ns/pF) CL + 25 ns  ttlH. ttHL = (0.75 ns/pF) CL + 12.5 ns	tTLH. tTHL	5.0 10		100	200 100	ns
$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		15	- 1	40	80	
Propagation Delay Time  tp_H, tpH_ = (1.7 ns/pF) C_ + 220 ns  tp_H, tpH_ = (0.66 ns/pF) C_ + 77 ns  tp_H, tpH_ = (0.5 ns/pF) C_ + 55 ns	tPLH tPHL	5.0 10 15	40 - <u>5</u> -	300 110 80	600 220 160	ns
Clock Pulse Width	twH 1995	5.0 10 15	200 120 80	100 60 40	-	ns
Clock Pulse Frequency	fcl	5.0 10 15	00L	5.0 8.3 12	2.5 4.2 6.0	МН
Clock Pulse Rise and Fall Time**	tTLH tTHL	5.0 10 15		=	15 5 4	μς
Setup Time	t <sub>su</sub>	5.0 10 15	0	-50 -15 -8.0	-	ns
Hold Time	th	5.0 10 15	180 90 75	75 25 20	=	ns

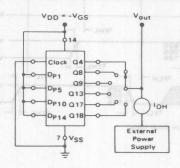
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

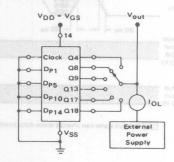
\*\*\*When shift register sections are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the rise and fall times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

# FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



#### FIGURE 2 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT



### MC14006B

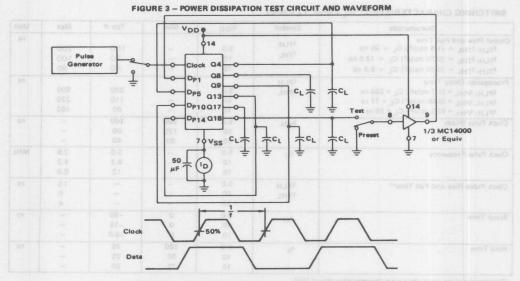
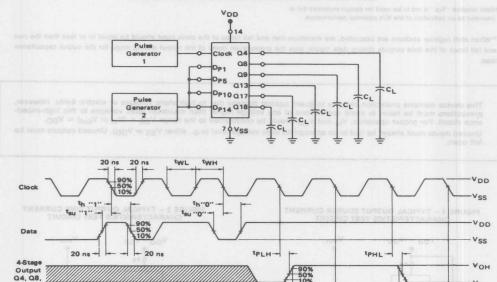


FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



tTLH -

tPLH'

TLH -

-VOL

-VOH

TPHL-

THL -

THL -

Output state can change since data previously clocked in might be in either state.

6

Q13, Q17

5-Stage Output Q9, Q18



# MC14007UB

#### **DUAL COMPLEMENTARY PAIR PLUS INVERTER**

The MC14007UB multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

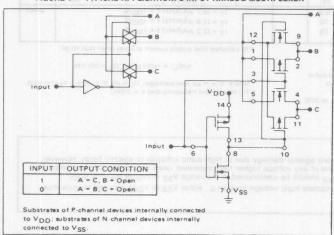
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Anti-static precautions must be taken.

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
Tı	Lead Temperature (8-Second Soldering)	260	00

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

#### FIGURE 1 — TYPICAL APPLICATION: 2-INPUT ANALOG MULTIPLEXER



# **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL COMPLEMENTARY PAIR PLUS INVERTER





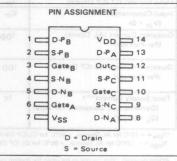
CERAMIC PACKAGE

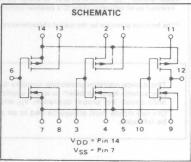
P SUFFIX PLASTIC PACKAGE CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXUBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXUBCP (Plastic Package) MC14XXXUBCL (Ceramic Package)





.

# MC14007UB

ELECTRICAL CHARACTERISTICS (Connected as Inverters) (Voltages Referenced to VSS)

		VDD	Tic	w *		25°C		Thi	igh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin= VDD or 0		10	-	0.05	-	0	0.05	-	0.05	
50		15	-	0.05	_	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95	_	Vdc
Vin = 0 or VDD	- OH	10	9.95	SINGLIFE	9.95	10	ENTAR	9.95	200 F 1 6	120
TOPRE VIOLETINGS INTERIOR DISMON	Library 1	15	14.95	LES A MI	14.95	15	IN INID	14.95	100 TH	1245
Input Voltage "0" Level	VIL									Vdc
(V <sub>O</sub> = 4.5)	112	5.0	lenna/is	1.0	0.230120	2.25	1.0	Jum BU	1.0	anijuc
$(V_0 = 9.0)$	State 1	10	abriane	2.0	160 380	4.50	2.0	dne_lane	2.0	rli bng
$(V_0 = 13.5)$	AUG !	15	TELLERAM	2.5	916 8	6.75	2.5	.834990	2.5	229336
"1" Level	VIH	13	Thousand of	2.5	Jupiger 1	0.73	2.5	1 12 12 12 1	2.5	MARKET IN
(VO = 0.5)	VIH	5.0	4.0	motoni	4.0	2.75	magant .	4.0	blorten	Vdc
(V <sub>O</sub> = 1.0)		10	8.0		8.0	5.50		8.0		100
(V <sub>O</sub> = 1.5)		15	12.5		12.5	8.25		12.5	-11 as	100
		15	12.5		12.5	8.25	2000万 50人	12.5	MOTH 91	DIU 6
Output Drive Current (AL Device)	ІОН		000		HOW OF	DE DESCRIPTION	C = 25	tan app	non And	mAdo
(V <sub>OH</sub> = 2.5 Vdc) Source	SELECTION I	5.0	-3.0	MO 70 8	-2.4	-5.0	wo.j-gw	9-1.7	le eten	(a) (0
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	ognistit o	-0.51	-1.0	art/Trevi	-0.36	TT spiles	928
(VOH = 9.5 Vdc)	HOPPINE !	10	-1.6	NO <u>0</u> ZUE	-1.3	-2.5	nok zone	-0.9	n/PLip1	ora m
(V <sub>OH</sub> = 13.5 Vdc)	R A BAN	15	-4.2	-	-3.4	-10	100 200	-2.4	10 -01	111 4 10
(VOL = 0.4 Vdc) Sink	OL	5.0	0.64	-	0.51	1.0	naker i	0.36	no other	mAdo
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.5		0.9	DE DOUBLES	Polist
(V <sub>OL</sub> = 1.5 Vdc)	MARIAN I	15	4.2	- 1	3.4	10	-	2.4	-	
Output Drive Current (CL/CP Device)	ГОН						TEN MIN			mAdo
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-5.0	-	-1.7	_	
(VOH = 4.6 Vdc)		5.0	-0.52	-	-0.44	-1.0	-	-0.36	-	-
(VOH = 9.5 Vdc)		10	-1.3	-	-1.1	-2.5	State Towns	-0.9	unive in	SE TRACKS
(VOH = 13.5 Vdc)		15	-3.6		-3.0	-10	-	-2.4	_	-
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52		0.44	1.0	100000	0.36		mAdc
(VOL = 0.5 Vdc)	00	10	1.3	-0.50	1.1	2.5	_	0.9	Singply V	bol a
(VOL = 1.5 Vdc)	SK CO.	15	3.6	V 61-10	3.0	10	10.9011	2.4	m.C - 1	
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	± 0.1	-	±1.0	₩Adc
Input Current (CL/CP Device)	lin	15	-	±03	7103 36	±0.00001	±03	ensol ivi	±1.0	μAdc
		13		20.5		5.0	7.5	-	21.0	pF
Input Capacitance	Cin	101	DETY	or 23		5.0	7.5	Shulfrat	mel egg	pr
(V <sub>in</sub> = 0)										1
Quiescent Current (AL Device)	IDD	5.0	-	0.25	1 -	0.0005	0.25	11121111	7.5	μAdc
(Per Package)		10	holde yea	0.50	III STUBS	0.0010	0.50	MINES NEG	15	testi mure
(1) to 470 878 [13]		15	- 3	1.00	meto	0.0015	1.00	offiners.	30	design to
Quiescent Current (CL/CP Device)	IDD	5.0	2,4824	1.0	00070.0	0.0005	1.0	DWESTED	7.5	μAdc
(Per Package)		10	-	2.0	-	0.0010	2.0	-	15	
		15	<b>福田田田田田</b>	4.0	DAILS &	0.0015	4.0	PHOALS	30	PAR
Total Supply Current**†	IT	5.0			IT = (0	7 HA/kHz	f + IDD/	6		μAdc
(Dynamic plus Quiescent, Per Gate)		10	1000			4 HA/kHz				
(C <sub>1</sub> = 50 pF)		15	La design	Sec. 1		2.2 HA/KHZ				
			1 141		,		B #			

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

†To calculate total supply current at loads other than 50 pF

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.003.

\*\*The formulas given are for the typical characteristics only at 25°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

<sup>\*</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise Time	tTLH		ME WENT			ns
<sup>†</sup> TLH = (1.2 ns/pF) C <sub>L</sub> + 30 ns		5.0	-	90	180	
tTLH = (0.5 ns/pF) CL + 20 ns		10		45	90	
tTLH = (0.4 ns/pF) CL + 15 ns		15	- 6	35	70	
Output Fall Time	tTHL		p	northy.		ns
<sup>t</sup> THL = (1.2 ns/pF) C <sub>L</sub> + 15 ns		5.0	00 - 6	75	150	
<sup>†</sup> THL = (0.5 ns/pF) C <sub>L</sub> + 15 ns		10	100 TT - 157	40	80	
tTHL = (0.4 ns/pF) CL + 10 ns		15	T- 1	30	60	
Turn-Off Delay Time	<sup>†</sup> PLH		Ja	n/V	sufur9	ns
tPLH = (1.5 ns/pF) CL + 35 ns		5.0		60	125	
tpLH = (0.2 ns/pF) CL + 20 ns		10	20901	30	75	
tpLH = (0.15 ns/pF) CL + 17.5 ns		15	50.1	25	55	
Turn-On Delay Time	tPHL					ns
tPHL = (1.0 ns/pF) CL + 10 ns		5.0	-	60	125	
tpHL = (0.3 ns/pF) CL + 15 ns		10	-	30	75	
tpHL = (0.2 ns/pF) CL + 15 ns		15	-	25	55	

\* The formulas given are for the typical characteristics only.

Switching specifications are for device connected as an inverter.

#Data labelled "Typ" is not to be used for design purposes but is

### FIGURE 2 - TYPICAL OUTPUT SOURCE CHARACTERISTICS

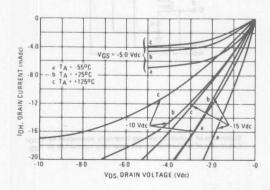
intended as an indication of the IC's potential performance.

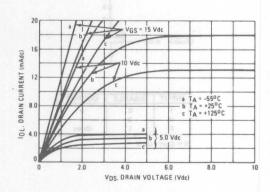
#### FIGURE 3 - TYPICAL OUTPUT SINK CHARACTERISTICS

70 VSS = VOI

VDD = VGS

All unused inputs connected to ground.



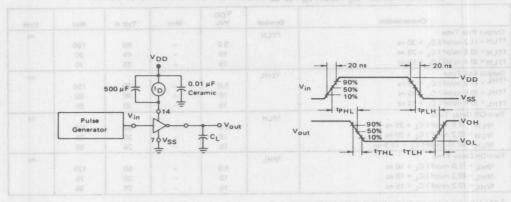


These typical curves are not guarantees, but are design aids.

Caution: The maximum current rating is 10 mA per pin.

# MC14007UB

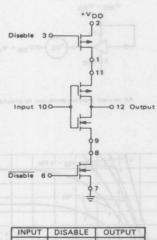
FIGURE 4 - SWITCHING TIME AND POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS OF MISCORDS



#### APPLICATIONS

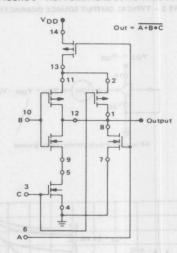
The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.

FIGURE 5 - 3-STATE BUFFER



1	0	0
0	0	1
X	1	Open

FIGURE 6 - AOI FUNCTIONS USING TREE LOGIC



Substrates of P-channel devices internally connected to  $V_{DD}$ : Substrates of N-channel devices internally connected to  $V_{SS}$ .



# MC14008B

#### 4-BIT FULL ADDER

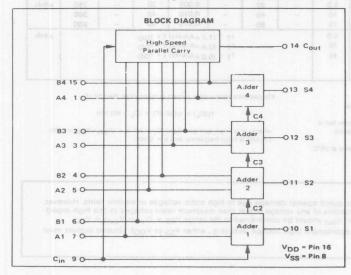
The MC14008B 4-bit full adder is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

- Look-Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc:
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

	(1000)		
Symbol	Parameter 8.8 - 0.5 -	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> . I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
IL	Lead Temperature (8-Second Soldering)	260	°C

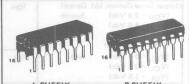
\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C



### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

4-BIT FULL ADDER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

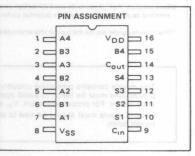
#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

# TRUTH TABLE (One Stage)

Cin	В	A	Cout	S
0 0 0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	100	0
1	0	0	0	1
1	0	1	1	. 0
1	1	0	1	0
1	1	1	1	1



ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS

		VDD	Tio	w*		25°C		Thi	gh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "0" Level	VOI	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0		10	-	0.05	-	0	0.05	-	0.05	-
·III · DD or o		15		0.05	-	0	0.05	- 1	0.05	
"1" Level	VOH	5.0	4.95		4.95	5.0	_	4.95	-	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	· OH	10	9.95		9.95	10	_	9.95	4	
vin = 0 or vDD		15	14.95	-	14.95	15	JS 718	14.95	_	
nput Voltage "0" Level	VIL								2710	Vdc
(VO 4.5 or 0.5 Vdc)	11.	5.0	FI 2016	15	mmano:	-2.25	1.5	4 8800	1.5	1
(VO · 9.0 or 1.0 Vdc)		10	nnoen sig	3.0	Baryab e	4.50	3.0	lenesria	3.0	charas
(V <sub>O</sub> · 13.5 or 1.5 Vdc)		15	ent diller	4.0	form mod	6.75	4.0	B 41 3	4.0	highid
"1" Level	VIH	10	ins nostil	ultin series	is no turb	0.70	BETHO VI	teo bear	s dright to	1331ni
(VO - 0.5 or 4.5 Vdc)	*IH	5.0	3.5	rugrug	3.5	2.75	d Lanoin	3.5	named inc	Vdc
(VO = 1.0 or 9.0 Vdc)		10	7.0	ing- is a	7.0	5.50	long-	7.0	A STATE OF THE PARTY	dona
(Vo = 1.5 or 13.5 Vdc)	4-11-2	15	11.0	DEAL P. U.	11.0	8 25	UDET IVO	11.0	nido pagi	- EASTH
		15	11.0		11.0	0 23	Tagair.	11.0	searla No	mAd
Output Drive Current (AL Device)	ЮН		20		-2.4	-4.2	Jon HA	-1.7		MAG
(VOH = 2.5 Vdc) Source		5.0	3.0	-	-0.51		-	-0.36	in a second	AB
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	1 9 TO W		-0.88	_			
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6		-1.3	-2.25	0.0 - 0	-0.9	la V-VI qu	112 中
(VOH = 13.5 Vdc)	PASSUE A	15	-4.2	10 70 0	-3.4	-8.8	out out	-2.4	to older	45 6
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	ons#Far	0.51	0 88	arti TravC	0.36	T valle	mAd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6		1.3	2.25		0.9		43 8
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	NOT THE	2.4	ar Luce	11111111
Output Drive Current (CL/CP Device)	ІОН	1								mAd
(VOH = 2.5 Vdc) Source	IN SERVICE	5.0	-2.5	-	-2.1	-4.2	-	-1.7	444	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	anger	-0.9	METAL !	BUNK
(VOH = 13.5 Vdc)		15	-3.6	W -	-3.0	-8.8	telemen	-2.4	-	les
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	orac mark	0.44	0.88	-	0.36	7-31 <del>-1</del> 1-3	mAd
(VOL = 0.5 Vdc)		10	1.3	-	1.1	2.25	-	0.9	-	
(VOL = 1.5 Vdc)		15	3.6	01/1/0	3.0	8.8	10 (20) 3	2.4	HO 30 P	e lips
nput Current (AL Device)	lin	15	- 0	± 0.1	COLF 160	±0.00001	±0.1	entit <u>u</u> itue	11.0	μAd
nput Current (CL/CP Device)	lin	15	- 00	± 0.3	-	±0.00001	± 0.3	no alces	±1.0	μAd
nput Capacitance	Cin	-5"	COAT.	1.00-		5.0	7.5	an econo	par spay	pF
(V <sub>in</sub> = 0)	Cin		1		-	3.0	7.5	anoning		pr
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAd
(Per Package)	00	10	197	10	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0.010	10	DES - 0.000	300	ST AND
The same of constants		15	-	20	Total State	0.015	20	9000013	600	S-mail
Quiescent Current (CL/CP Device)	IDD	5.0	1 -	20	-	0.005	20	-	150	μAd
(Per Package)	.00	10		40	_	0.000	40		300	MAG.
	The H	15		80	1	0.015	80	_	600	
Total Supply Current**†	IT	5.0	1	00	1 11				000	μAd
(Dynamic plus Quiescent,	"	10	In her h			1.7 µA/kHz)				μΑσ
Per Package)		15				3.4 μA/kHz) 5.0 μA/kHz)				
(C <sub>1</sub> = 50 pF on all outputs, all	197 10 141	15			.1 (5	).U HA/KHZ)	, , , DD			
buffers switching)	07 1797									

 $<sup>^*</sup>T_{low} = -55^\circ C$  for AL Device,  $-40^\circ C$  for CL/CP Device.  $T_{high} = +125^\circ C$  for AL Device,  $+85^\circ C$  for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.005.

\*\*The formulas given are for the typical characteristics only at 25°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{Out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{OUt}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

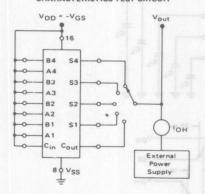
# MC14008B

SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

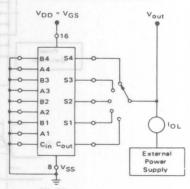
Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise and Fall Time	tTLH-					ns
$t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$	tTHL	5.0	-	100	200	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns		10	-	50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		15	_ an 4	40	80	
Propagation Delay Time	tPLH. TPHL		ggV-	14	2004	ns
Sum In to Sum Out					· · · · · · · · · · · · · · · · · · ·	ist V
tpLH, tpHL = (1.7 ns/pF) CL + 315 ns		5.0	EgV - J	400	800	and the same
tpLH, tpHL = (0.66 ns/pF) CL + 127 ns	S	10	-	160	320	
tpLH, tpHL = (0.5 ns/pF) CL + 90 ns	0-0-0	15	-	115	230	
Sum In to Carry Out	5 C					
tpLH, tpHL = (1.7 ns/pF) CL + 220 ns	A promotion of the same	5.0	-	305	610	1
tpLH, tpHL = (0.66 ns/pF) CL + 112 ns		10	-	145	290	
tpLH, tpHL = (0.5 ns/pF) CL + 85 ns		15	-	110	220	
Carry In to Sum Out		1				
tpLH, tpHL = (1.7 ns/pF) CL + 290 ns		5.0		375	750	
tpLH, tpHL = (0.66 ns/pF) CL + 122 ns		10		155	310	
tpLH, tpHL = (0.5 ns/pF) CL + 90 ns	75 38.000	15	_	115	230	
Carry In to Carry Out						
tpLH, tpHL = (1.7 ns/pF) CL + 85 ns		5.0	- 1	170	340	
tpLH, tpHL = (0.66 ns/pF) CL + 42 ns		10		75	150	
tplH, tpHL = (0.5 ns/pF) C1 + 30 ns		15	_	55	110	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#### FIGURE 1 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



#### FIGURE 2 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT



<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 3 - DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM TO A MANO COMMENTAL PROPERTY OF THE PROPERTY OF

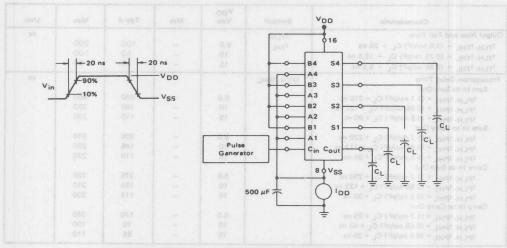
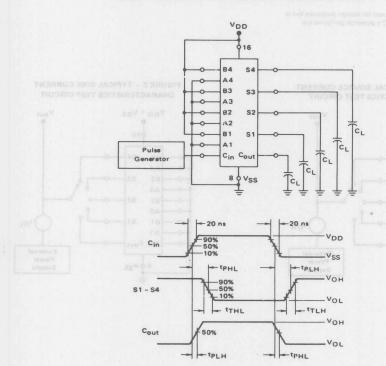
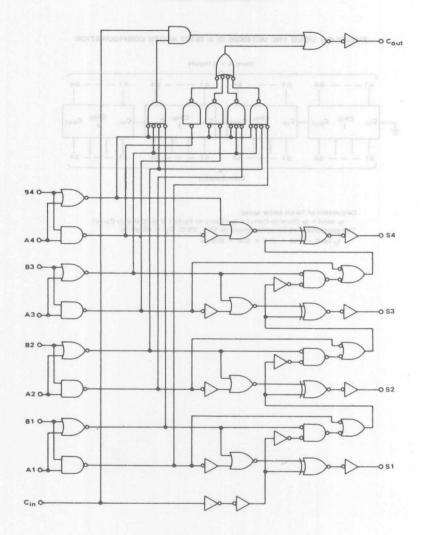


FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



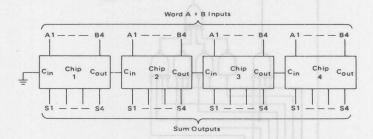
# FIGURE 5 - LOGIC DIAGRAM



# MC14008B

#### TYPICAL APPLICATION

# FIGURE 6 - USING THE MC14008B IN A 16-BIT ADDER CONFIGURATION



Calculation of 16-bit adder speed: tp total = tp (Sum to Carry) + tp (Carry to Sum) + 2 tp (Carry to Carry) The guaranteed 16-bit adder speed at 10 V, 25°C,  $C_L = 50$  pF is: tp total = 290 + 310 + 300 = 900 ns

# MOTOROLA

#### QUAD 2-INPUT "NAND" GATE

The MC14011B and MC14011UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14011B only)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14011B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4011B and CD4011UB

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter #20	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package – 12mW/°C from 65°C to 85°C

Ceramic "L" Package – 12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

# MC14011B MC14011UB

### **CMOS SSI**

(LOW POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE

For complete data see MC14001B or MC14001UB as applicable.





L SUFFIX CERAMIC PACKAGE CASE 632

P SUFFIX

GE PLASTIC PACKAGE

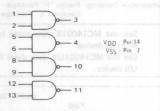
CASE 646

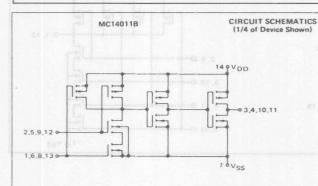
#### ORDERING INFORMATION

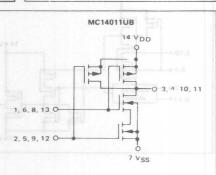
A Series: -55°C to +125°C MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP or UBCP (Plastic Package) MC14XXXBCL or UBCL (Ceramic Package)

#### LOGIC DIAGRAM









# MC14012B MC14012UB



#### **DUAL 4-INPUT "NAND" GATE**

The MC14012B and MC14012UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14012B only)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14012B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4012B and CD4012UB

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	HOTAMPONI D Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin-lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

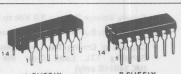
See the MC14001B data sheet for complete characteristics of the  $B ext{-}Series$  device.

See the MC14001UB data sheet for complete characteristics for the UB device.

### **CMOS SSI**

(LOW POWER COMPLEMENTARY MOS)

**DUAL 4-INPUT "NAND" GATE** 



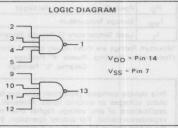
CERAMIC PACKAGE

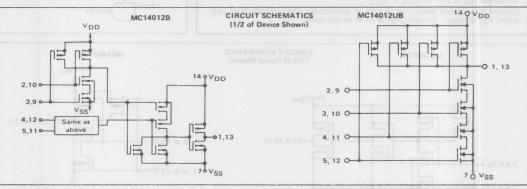
P SUFFIX PLASTIC PACKAGE CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP or UBCP (Plastic Package) MC14XXXBCL or UBCL (Ceramic Package)





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# MC14013B

#### DUAL TYPE D FLIP-FLOP

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and  $\overline{\rm Q}$ ). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design Logic state is retained indefinitely with clock level either high or
   low; information is transferred to the output only on the positive
   going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B

### CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

**DUAL TYPE D FLIP-FLOP** 





L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

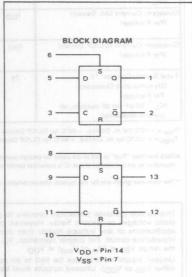
\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

# TRUTH TABLE

INPUTS				OUT	PUTS	
CLOCK	DATA	RESET	SET	Q	ā	٦
5	0	0	0	0	1	٦
5	10191	0	0	1	0	7
7	×	0	0	Q	ā	
×	×	1	0	0	to lar	
×	×	0	1	0100	0	
~	T v	1	1	1 ,	,	7

X = Don't Care
t = Level Change



	Symbol	V <sub>DD</sub> Vdc	T <sub>low</sub> *		25°C			Thigh*		-
Characteristic			Min Max		Min	Тур#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0		10		0.05		0	0.05	-	0.05	-
- III - DD		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95	-	Vdc
	· On	10	9.95	_	9.95	10		9.95	- 1	
V <sub>in</sub> = 0 or V <sub>DD</sub>		15	14.95	_	14.95	15	-	14.95		
Input Voltage "0" Level	VIL			1	Pall 7 13	1 1 12 11 1	1 1071	3.0		Vdc
(VO = 4.5 or 0.5 Vdc)	, IL	5.0		1.5	_	2.25	1.5	11-100	1.5	
(VO = 9.0 or 1.0 Vdc)		10	M righty	3.0	100 Et 400	4.50	3.0	and the	3.0	
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	Die 6 O	4.0	apam .	6.75	4.0	erla-VI br	4.0	2-76
"1" Level	VIH	13	T REVE	4.0	CHIPS CO	0.75		-		-
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	VIH	5.0	3.5	stugiti.	3.5	2.75	J919 Ft. 1	3.5	BUILDER TO	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	es bano s	7.0	5.50	I' till bri	7.0	EDG AURTO	100
(VO = 1.5 or 13.5 Vdc)		15	The state of the s	der 200s.	11.0	8.25	H ] 89	11.0	Grandinal of	197
diameter and the second		15	11.0		11.0	0.25		11.0		mAdo
Output Drive Current (AL Device)	ІОН				0.4	-4.2		1	La College	mAdd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-3.0	-	-2.4			-1.7	UC TARRE	-
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	间面外面	-0.36	129 650 C	0
(V <sub>OH</sub> = 9.5 Vdc)	9 991	10	-1.6	-	-1.3	-2.25	nge <u>=</u> 3,	-0.9	V ylanus	65
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	-	-3.1	-8.8		-2.4	-	_
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	THE PERSON	0.36	100 - 910	mAde
(V <sub>OL</sub> = 0.5 Vdc)	Lese I	10	1.6	is teuni	1.3	2.25	4504 09n	0.9	TOTAL TIME OF	
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	icno-ylm	3.4	8.8	rate (co)	2.4	tofra in o	
Output Drive Current (CL/CP Device)	ГОН					9	len You	3157 TOPS	SON WHAT	mAde
(VOH = 2.5 Vdc) Source		5.0	-2.5	to not since	-2.1	-4.2	1 00/1	-1.7	sk <del>h</del> ipsC	185
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	Confirmation	-0.44	-0.88	II SEVEL	-0.36	Schlettier!	
(V <sub>OH</sub> = 9.5 Vdc)	A E	10	-1.3	-	-1.1	-2.25	-	-0.9		-
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	of toem	-2.4	-	
(VOI = 0.4 Vdc) Sink	OL	5.0	0.52	-	0.44	0.88	_	0.36	-	mAde
(V <sub>OL</sub> = 0.5 Vdc)	. 00	10	1.3		1.1	2.25	-	0.9	_	The state of
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8	-	2.4	_	
Input Current (AL Device)	lin	15		± 0.1		±0.00001	±0.1	-	±1.0	μAdd
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	un TRESI	±1.0	μAdd
Input Capacitance		,,,			Joev.	5.0	7.5	37.21		pF
(V <sub>in</sub> = 0)	Cin	71883	aut	0//		3,0	7.5			pr
Quiescent Current (AL Device)	IDD	5.0	0.63 + 1	1.0	-	0.002	1.0	90252-39	30	μAdd
(Per Package)	.00	10	In # And	2.0	_	0.004	2.0	stille-teat	60	Trim's
		15	0	4.0	-	0.006	4.0	-	120	
Quiescent Current (CL/CP Device)	IDD	5.0	-	4.0		0.002	4.0		30	μAdo
(Per Package)	יטטי	10	DE	8.0		0.004	8.0	d 50050	60	μΑσο
. C. Schager		15	02140	16		0.006	16	or mante	120	4
Total Supply Current**†	IT	5.0						CONT TO		
(Dynamic plus Quiescent,	'1	10	$I_T = (0.75 \mu\text{A/kHz})  f + I_{DD}$ $I_T = (1.5 \mu\text{A/kHz})  f + I_{DD}$ $I_T = (2.3 \mu\text{A/kHz})  f + I_{DD}$						μAdd	
Per Package)		15							e mine	
(C <sub>1</sub> - 50 pF on all outputs, all		15							THE PERSON	
buffers switching)		KIL.	D. HOT							

 $<sup>^*</sup>T_{low} = -55^\circ\text{C}$  for AL Device,  $-40^\circ\text{C}$  for CL/CP Device.  $T_{high} = +125^\circ\text{C}$  for AL Device,  $+85^\circ\text{C}$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

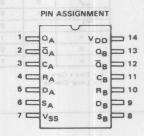
†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



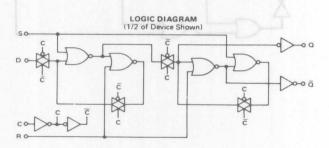
# 6

# SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

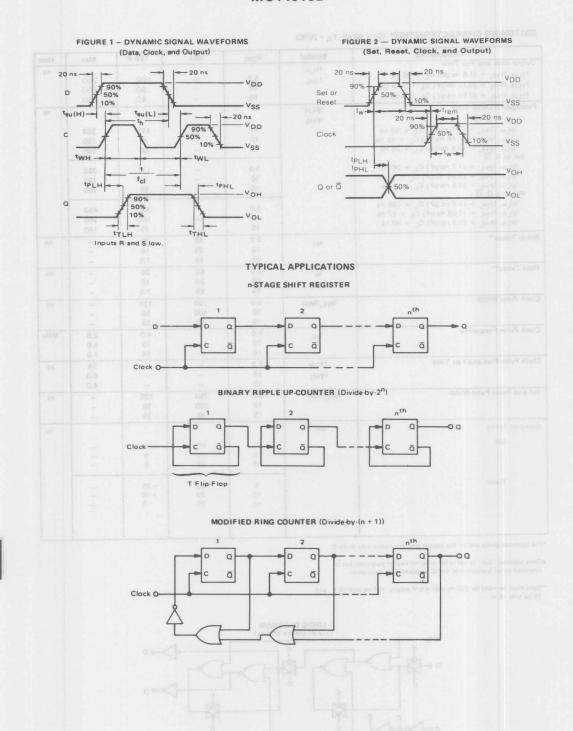
Symbol	VDD	Min	Typ #	Max	Uni
t <sub>TLH</sub> .		20 DE		was been an	ns
	5.0		100	200	
Inc	10	-	50	100	1
1 19 192	15	- 1	40	80	
tPLH	-000		Suria - Carrier	(ht))	ns
†PHL		The second second	Personal Party Committee	1000	
	5.0	1782	175	350	6
Manage	10	The Part of	75	150	
	15	- 1	50	100	
	5.0	-	175	350	
	10		75	150	
ā to a	15	The contract to	50	100	
	5.0	4	350	450	
	10		100	200	
	15		75	150	
	5.0	40	20	administration 1	ns
<sup>t</sup> su				1000000	
				_	
GIRROTT ACALITYSIS.	A DESCRIPTION OF THE PARTY OF T				ns
th	107000				l ns
BRITE REGISTER				_	
					-
tWL, tWH				-	ns
		and the same of th		-	
		The last war and			-
fcl		+	-		MH
6 0		a strong			1
New company		-	14		-
tTLH					μs
tTHL		-	-		1
		-	-	4.0	
tWL, tWH	5.0	250	125	-	ns
	10	100	50	-	1
5	15	70	35	-	
trem		10 00-			ns
	5	80	0	_	
la lanceron	10	45	5	_	
No.	15	35	5	-	-
1.0	E	700	25		1
	15	25			
Library on marriage		denesia			
	tyLH tpHL  tyLH tpHL  th  twL, twH  fcI  tTHL twL, twH	tTLH- tTHL tTHL tTHL tTHL tTHL tTHL tTHL tTHL	tTLH. tTHL tTHL tTHL tTHL tTHL tTHL tTHL tTHL	tTLH- tTHL  tTLH tTHL  5.0  10  - 50  15  - 40   tPLH tPHL  5.0  - 175  10  - 75  15  - 50  5.0  - 175  10  - 75  15  - 50  5.0  - 175  10  - 75  15  - 50  5.0  - 10  - 100  - 100  - 15  - 50   tsu  10  20  10  10  20  10  15  15  75  th  5.0  40  20  10  10  20  10  15  15  75  th  5.0  40  20  10  15  15  75  th  5.0  40  20  10  15  15  75  th  5.0  40  20  10  10  20  10  15  15  7.5  tWL, tWH  5.0  250  125  10  10  - 10  11  tTLH  5.0  - 14  tTLH  5.0  - 14  tTLH  5.0  - 10  10  10  15  70  35  twL, tWH  5.0  250  125  5  70  35  14  tWL, tWH  5.0  250  125  5  5  6  10  10  10  10  10  10  10  10  10	tTLH. tTHL tTHL tTHL tTHL tTHL tTHL tTHL tTHL

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>\*\*</sup>Data must be valid for 250 ns with a 5 V supply, 100 ns with 10 V, and 70 ns with 15 V.



<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

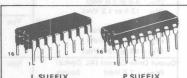


# MC14014B MC14021B

### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER



CERAMIC PACKAGE CASE 620 PSUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### 8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

TRUTH TABLE SERIAL OPERATION: 08 06 Ds t = n+7 CLOCK P/S t = n+6 t = n+8 0 0 0 0 0 n+2 0 0 0 X 0 Q6 08

PARALLEL OPERATION:

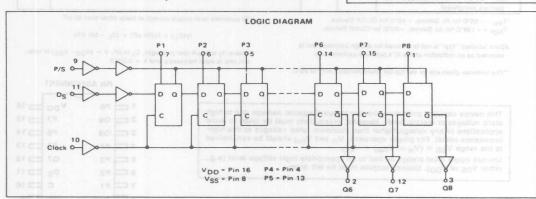
CLOCK

MC14014B MC14021B

X X 1 0 0

X X 1 1 1 1

\*Q6, Q7, & Q8 are available externally X = Don't Care



		VDD	Tic	ow*		25°C		Thi	gh *	-
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	ave, is	10	-	0.05	-	0	0.05	-	0.05	-
TELEPHONE NAME OF STREET		15	-	0.05	_	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95		4.95	5.0		4.95		Vdc
Vin = 0 or VDD	011	10	9.95	<u> 1</u> 131	9.95	10	DITAT	9.95		1
		15	14.95	_	14.95	15	_	14.95		
Input Voltage "0" Level	VIL		1	al Pinte	CHILDRE T	0 0 100	PERMIT	B GP/O	FF GIVE	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		5.0	PORMUNE	1.5	inggard	2.25	1.5	BOM HIT	1.5	GOVERN
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	and another	3.0	Thase	4.50	3.0	pro siprii	3.0	diveb
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	es suana	4.0	roitzara	6.75	4.0	lasen n	4.0	orino
"1" Level	VIH		0.70 0.48	0.00	1 1080 F	Galle Kirk	ia Pacri	Islianco	aucanoh 1	Seven
(VO = 0.5 or 4.5 Vdc)		5.0	3.5	union sons	3.5	2.75	lare se	3.5		Vdc
(VO = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50	-	7.0		1
(VO = 1.5 or 13.5 Vdc)		15	11.0		11.0	8.25		11.0	HILL SHOT	rigid
	- 286	13	11.0	- 10 May 1930	11.0	6.25	Transport I			
Output Drive Current (AL Device)	ІОН		-3.0		2.4	1.0	DESCRIPTION OF	DE PERSE		mAdd
(V <sub>OH</sub> = 2.5 Vdc) Source	L	5.0		BESOME	-2.4	-4.2	min le	-1.7	no retains	4 . =
(V <sub>OH</sub> = 4.6 Vdc)	ARBS 1	5.0	-0.64	-	-0.51	-0.88	2'aruant	-0.36	scorlan.	2 4
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	-	-0.9	obsezi in	2 0
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	- 146	-2.4		-
(VOL = 0.4 Vdc) Sink	OL	5.0	0.64	rapere	0.51	0.88	AL ALIXE	0.36	restal (	mAd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.25	1007019	0.9	O Fide	3 0
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	0.5.7.00	2.4	ota Tables	2 0
Output Drive Current (CL/CP Device)	ІОН	1110	and the same of the	of Days of the	1 17 mm	Canada a	at aut	The state of the s		mAdd
(VOH = 2.5 Vdc) Source	0	5.0	-2.5	Benga	-2.1	-4.2	OJ DWT	-1.7	o eldeci	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	-	-0.36	A KENNY	
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	_GR4	-1.1	-2.25	gaE m	-0.9	ATOM:	1911 19
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-875	-3.0	-8.8	ges aif	-2.4	115-11	12 10
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	_	0.36	-	mAdd
(VOL = 0.5 Vdc)		10	1.3	-	1.1	2.25		0.9	-	
(VOL = 1.5 Vdc)	DE BLAN	15	3.6	-	3.0	8.8	-	2.4		
Input Current (AL Device)	lin	15	-	±0.1	-	± 0.00001	± 0.1	_	± 1.0	μAdo
Input Current (CL/CP Device)	lin	15	-	± 0.3	1-W	±0.00001	± 0.3	in 48.29	± 1.0	μAdd
Input Capacitance	Cin	med 1			1997	5.0	7.5	-		pF
(V <sub>in</sub> = 0)	Cin	311/00	Toute		-	5.0	7.5			pr
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdd
(Per Package)	00	10	000V	10	-	0.010	10	dio/Liturgs	300	Voul
MOST A GOOD AND A	COLAD I	15	- 01	20	019 700	0.015	20	med hand	600	
Quiescent Current (CL/CP Device)	IDD	5.0	- 003	20	_	0.005	20		150	μAdd
(Per Package)		10	Gibi	40	and the same	0.010	40	a mourn	300	Ande
at soutow and	ALOM J	15	087 + 01	80	_	0.015	80	FIDE INCH	600	1 000
Total Supply Current**†	IT	5.0	094	- 00	110	.75 µA/kHz		SY marks	000	1
(Dynamic plus Quiescent,		10				.75 μΑ/KHZ .50 μΑ/KHZ				μAdd
Per Package)	200	15	The Parish			.25 µA/kHz				S Phillips
(C <sub>1</sub> = 50 pF on all outputs, all		15	The page 4							descende
buffers switching)			1							

 $^*T_{low}$  =  $-55^\circ$ C for AL Device,  $-40^\circ$ C for CL/CP Device.  $T_{high}$  =  $+125^\circ$ C for AL Device,  $+85^\circ$ C for CL/CP Device. †To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.0015.

\*\*The formulas given are for the typical characteristics only at 25°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in}$  or  $V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

PIN ASSIGNMENT 16 1 P8 VDD 2 06 P7 **1**5 3 - 08 P6 **14** 13 4 P4 P5 5 P3 Q7 12 6 P2 D<sub>S</sub> = 11 7 P1 C = 10 8 - VSS P/S □9

### MC14014B•MC14021B

SWITCHING CHARACTERISTICS (C1 = 50 pF, TA = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ#	Max	Unit
Output Rise and Fall Time	tTLH,					ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTHL	5.0	_	100	200	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns	(0)	10	_	50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	1	15	-	40	80	
Propagation Delay Time (Clock to Q, P/S to Q)	tPLH,					ns
tpHL, tpLH = (1.7 ns/pF) CL + 315 ns	tPHL	5.0	50.07	400	800	
tpHL, tpLH = (0.66 ns/pF) CL + 137 ns	- AD 2	10	Tours and	170	340	
$t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$	19	15		115	230	
Clock Pulse Width	twH	5.0	400	150	_	ns
	J	10	175	75	_	
	733 95	15	135	40	-	
Clock Frequency	fcl	5.0		3.0	1.5	MHz
	2.0	10	-	6.0	3.0	
7-0	HID 85	15	Bulga.	8.0	4.0	
Parallel/Serial Control Pulse Width	twH	5.0	400	150	_	ns
		10	175	75	_	
	1277	15	135	40	_	
Setup Time	t <sub>su</sub>	5.0	200	100	_	ns
P/S to Clock		10	100	50	_	
	/	15	80	40	-	
Hold Time	th	5.0	20	-2.5	_	ns
Clock to P/S	1-1011-2	10	20	-10	_	
		15	25	0		
Setup Time	t <sub>su</sub>	5.0	350	150	-	ns
Data (Parallel or Serial) to		10	80	50	_	
Clock or P/S		15	60	30	_	
Hold Time	th	5.0	45	0	-	ns
Clock to D <sub>S</sub>		10	35	0	_	
		15	35	5	_	
Hold Time	th	5.0	50	25	_	ns
Clock to Pn		10	45	20	_	
		15	45	20	-	
Input Clock Rise Time	tr(cl)	5.0		110	15	μѕ
		10	-		5	of district on D
		15	-		4	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - OUTPUT SOURCE CURRENT TEST CIRCUIT

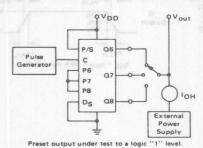
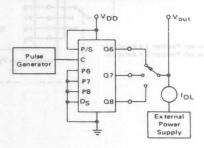
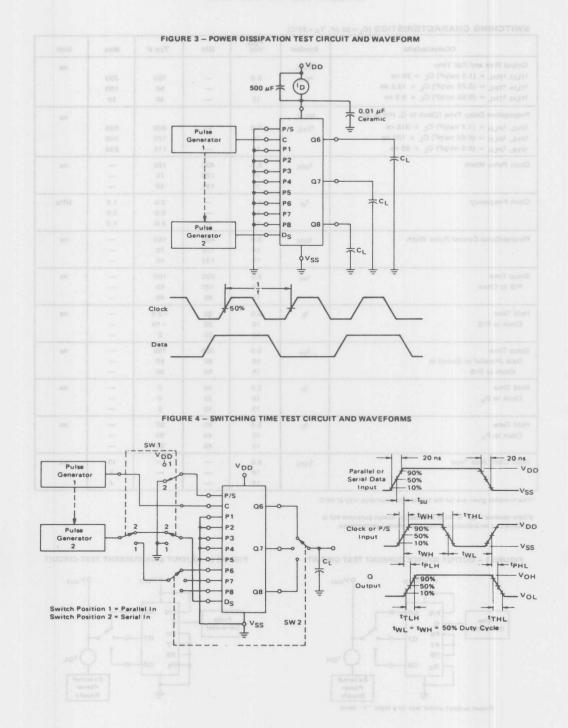


FIGURE 2 - OUTPUT SINK CURRENT TEST CIRCUIT



### MC14014B • MC14021B





### MC14015B

# DUAL 4-BIT STATIC SHIFT REGISTER

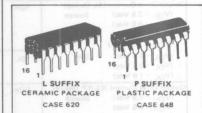
The MC14015B dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops, Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design —
   Logic state is retained indefinitely with clock level either high or
   low; information is transferred to the output only on the positive
   going edge of the clock pulse.
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.

### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT STATIC SHIFT REGISTER



#### ORDERING INFORMATION

A Series: -55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/"C from 65°C to 85°C Ceramic "L" Package: - 12mW/"C from 100°C to 125°C

#### TRUTH TABLE

C	D	R	QO	Qn
_	0	0	0	Q <sub>n-1</sub>
	Ato	0	1	Q <sub>n-1</sub>
~	×	0	No Change	No Change
X	X	1	0	0

X = Don't Care  $Q_n = Q0, Q1, Q2, or Q3, as applicable.$   $Q_{n-1} = Output of prior stage.$ 

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tio	w*		25°C		Thi	gh °	1
Characteristic	Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	- 1	0.05	Vdc
Vin = VDD or 0		10	-	0.05		0	0.05	-	0.05	-
		15	-	0.05	-	0	0.05	- 1	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95		Vdc
Vin = 0 or VDD	011	10	9.95	_	9.95	10	_	9.95		
III COLUDO		15	14.95	_	14.95	15	_	14.95	-	
Input Voltage "0" Level	VIL									Vdc
(Vo : 4.5 or 0.5 Vdc)		5.0	- 83	1.5	10 731	2.25	1.5	A JAU	1.5	
(Vo 9 0 or 1.0 Vdc)		10	-	3.0	-	4.50	3.0	_	3.0	
(VO = 13.5 or 1.5 Vdc)		15	w below	4.0	Delega II	6.75	4.0	0 85100	4.0	
"1" Level	VIH	1015	1-15 E. E. E. E. E.	CHAMP 2	WHI PERIL	STORESCHOOL S	STEEDING!	CKER GITT	HARD TO S	100
(VO = 0.5 or 4.5 Vdc)		5.0	3.5	ntical,	3.5	2.75	00 11.	3.5	oid libric	Vdc
(VO = 1.0 or 9.0 Vdc)		10	7.0	deiper d	7.0	5.50	ro-Ibritan	7.0	siring old	304
(VO = 1.5 or 13.5 Vdc)		15	11.0	os G-lain	11.0	8.25	gni-juse	11.0	elO Jhab	day .
Output Drive Current (AL Device)	ГОН	(10)	12 202 LB	Data is I	ganit-o	7 9 45 13 19 1	SZW CI B	P27 =25 E	STATE NOTE	mAdd
(VOH = 2.5 Vdc) Source	'OH	5.0	-3.0	neve tino	-2.4	-4.2	r puitori	-1.7	of spare	ne
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	ofe - A fu	-0.51	-0.88	made h	-0.36	00/2-19/02	best
(VOH = 9.5 Vdc)		10	-1.6	one true to	-1.3	-2.25	a pent	-0.9	mm-1 43	NT.
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	o symmetric	-3.4	-8.8	Latinary	-2.4	han - land	1000
(VOI = 0.4 Vdc) Sink	6.	5.0	0.64	-	0.51	0.88	tion to be	0.36		mAdo
(V <sub>OL</sub> = 0.5 Vdc)	OL	10	1.6		1.3	2.25	NED-SI A	0.9	0630-101	MAGG
	91	15	4.2		3.4	8.8		2.4		
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2		3.4	0.0	of It a	2.4	HS 90010	100
Output Drive Current (CL/CP Device)	ІОН		0.5		-2.1	-4.2		-1.7		mAdd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-2.5	-	-0.44	-4.2	-	-0.36		
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52		-1.1	THE PERSON NAMED IN	Plant b	-0.36	DF 1964	1 *
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	e tëvel	-3.0	-2.25 -8.8	bnl ben	-2.4	in Digg.	1
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6		The Cold of	THE REPORTS	ducket a	0.000	milya war	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	lock nur	0.36	gris Trill o	mAdd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3	-	1.1	2.25		0.9		
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	1 10-008	3.0	8.8	d days t	2.4	plosos	
Input Current (AL Device)	lin	15	-/80	± 0.1	1802181	± 0.00001	± 0.1	BOY 71.1	± 1.0	μAdo
Input Current (CL/CP Device)	lin	15	-	± 0.3	775	±0.00001	± 0.3	-	±1.0	μAdo
Input Capacitance (V <sub>in</sub> = 0)	Cin	-			1 - 10	5.0	7.5	-	-	pF
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdo
(Per Package)	100	10	- 1	10	_	0.003	10		300	1
		15		20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device)	lee	5.0	-		-	0.005	20			1
(Per Package)	lDD	10	_	20	-	0.005	40	0.52.00	150	μAdo
(rei rackage)		15	-	40 80	15	0.010	80	-	300	
Table and Committee			-	80					600	Linde
Total Supply Current**†	IT	5.0	0.80 - 0			1.2 µA/kHz				μAdd
(Dynamic plus Quiescent,		10				2.4 µA/kHz				
Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)		15	91		T - (3	3.6 µA/kHz	) I + IDD	man in the		nu2

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: IT is in  $\mu$ A (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

PIN ASSIGNMENT 1 CB VDD 16 2 - Q3B D<sub>B</sub> 15 3 - Q2A R<sub>B</sub> 14 4 01A Q0B 13 Q1B 12 5 - Q0A 6 RA Q2B 11 7 DA Q3A 10 8 VSS CA 9

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

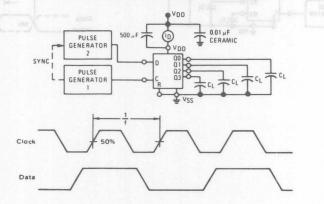
<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	t <sub>TLH</sub> ,					ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	THL	5.0	_	100	200	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns		10		50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		15	-	40	80	
Propagation Delay Time	tPLH,	LIA LINE				ns
Clock, Data to Q	tPHL		dgY	7		
tpLH, tpHL = (1.7 ns/pF) CL + 225 ns		5.0	- 1	310	750	1
tpLH, tpHL = (0.66 ns/pF) CL + 92 ns	10 755	10		125	250	ethor;
tpLH, tpHL = (0.5 ns/pF) CL + 65 ns		15	-0-10	90	170	
Reset to Q	1				particular programme	Justas
tpLH, tpHL = (1.7 ns/pF) CL + 375 ns		5.0	201	460	750	
tPLH, tPHL = (0.66 ns/pF) CL + 147 ns		10	7 -0100	180	250	to A
tpLH, tpHL = (0.5 ns/pF) CL + 95 ns	1	15	15 = A	120	170	
Clock Pulse Width	twH	5.0	400	185	_	ns
		10	175	85	_	
1027   Section 10		15	135	55	_	
Clock Pulse Frequency	fcl	5.0	-	2.0	1.5	MHz
	2000	10	-	6.0	3.0	
		15	-	7.5	3.75	
Clock Pulse Rise and Fall Times	TLH, THL	5.0	-	_	15	μs
		10	-	-	5	
		15	_	-	4	
Reset Pulse Width	twH	5.0	400	200	-	ns
		10	160	80	-	
		15	120	60	-	
Setup Time	t <sub>su</sub>	5.0	350	100	_	ns
		10	100	50	-	
	TOTAL PROPERTY.	15	75	40	_	

<sup>\*</sup>The formulas given are for typical characteristics only at 25°C.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### MC14015B

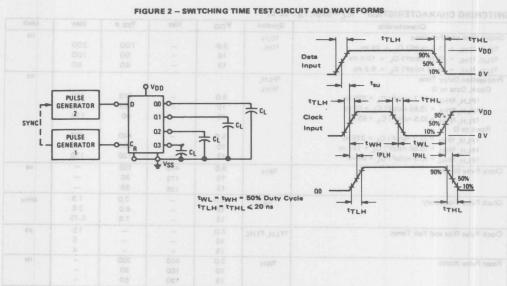
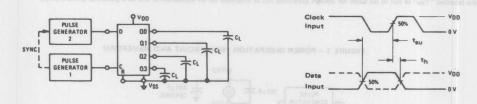
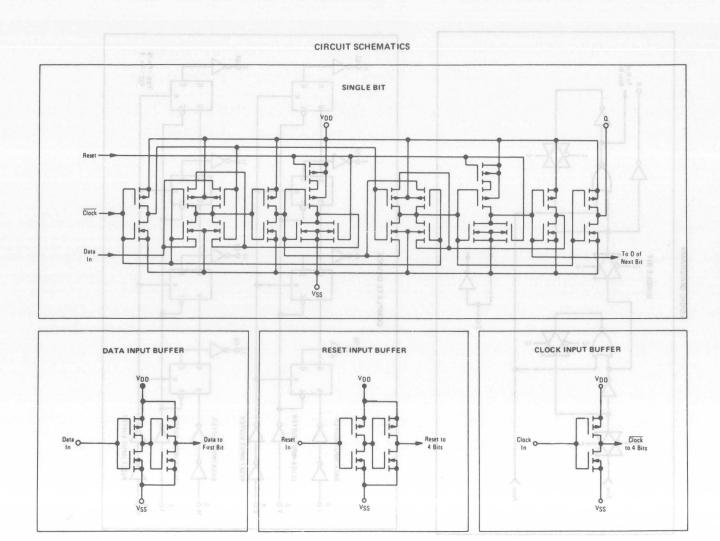
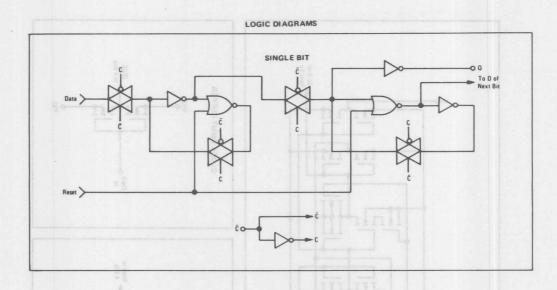


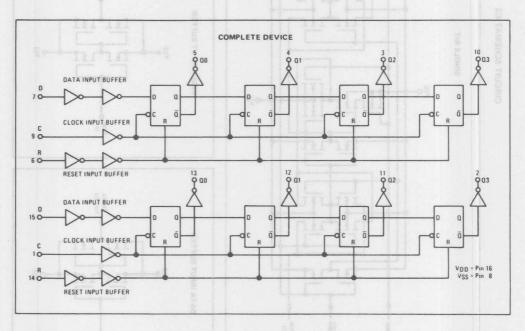
FIGURE 3 - SETUP AND HOLD TIME TEST CIRCUIT AND WAVEFORMS





### MC14015B







### MC14016B

#### QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise 12nV/√Cycle, f≥1 kHz typical
- Pin-for-Pin Replacement for CD4016B, CD4066B
- For Lower R<sub>ON</sub>, Use The HC4016 High-Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.

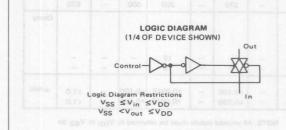
MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin	Input Current (DC or Transient), per Control Pin	± 10	mA
Isw	Switch Through Current	± 25	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C
Ceramic "L" Package: -12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



#### **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH QUAD MULTIPLEXER





CERAMIC PACKAGE
CASE 632

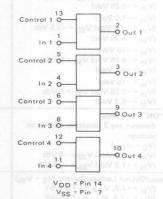
P SUFFIX PLASTIC PACKAGE CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### BLOCK DIAGRAM



CONTROL	SWITCH
0 = V <sub>SS</sub>	JA vol O'OFF = roleT
1 = V <sub>DD</sub>	ON

# ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

			VDD	TI	ow*		25°C		Th	igh*	
Characteristics	Figure	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
nput Voltage	1	VIL	5.0	-	-	-	1.5	0.9	_	-	Vdc
Control Input			10	-	-	-	1.5	0.9	-	-	
			15	(3-19)	LITIM	DAU	1.5	0.9	1/5/1/	GAL	2
	10011	VIH	5.0	GNOW IN	-	3.0	2.0	-	-	0.000	Vdc
			10	Danie Di		8.0	6.0	IO_DOD	-	MICIN :	12.0
OW POWER CONFLEMENTARY MOST	(4)		15	pq12-6	- 110	13	10911900	- 19	10040-	1 1 - 1	Enerto
nput Current (AL Device) Control	-	lin	15	ricin <u>i</u> n	±0.1	-	±0.00001	±0.1	63_5	±1.0	μAdc
nput Current (CL/CP Device) Control	-	lin	15	ALK TANK	±0.3	7 12/21	±0.00001	±0.3	10 30	±1.0	μAdc
nput Capacitance	-	Cin				zuolen	triamelismi	oleon 20		at vende	pF
Control			-	-	-	-	5.0	-	-	-	
Switch Input		1	_	-	-	-	5.0	All inp	no mois	e Protes	piG =
Switch Output Feed Through			_	_		s Vels	5.0	00 = 3	Nasis an	on Volta	NS W
	0.0		5.0	-	0.05		0.001001001	0.05	satenet		
Quiescent Current (AL Device)** (Per Package)	2,3	IDD	5.0	_	0.25	- 100mv1	0.0005	0.25	V-2	7.5 15	μAdc
(i of Fackage)	Dia I		15		1.00	-	0.0015	1.00		30	Land in
	6.0				100000	1000			nashik.	E DESTRUCTION	19 6
Quiescent Current (CL/CP Device)**	2,3	IDD	5.0	SOM	1.0	ingtel	0.0005	1.0	-Mgf	7.5	μAdc
(Per Package)			10	N	4.0	Di	0.0010	2.0	7380	15 30	PRET
La Station Co. L. Station C		-	10	in America	4.0	0.51	0.0013	4.0	Table I vs.	30	-
'ON" Resistance (AL Device)**	4,5,6	RON			1						Ohms
$V_C = V_{DD}, R_L = 10 \text{ k}\Omega$ $(V_{in} = +5.0 \text{ Vdc})$			5.0		600	_	300	660		960	
$(V_{in} = -5.0 \text{ Vdc}) V_{SS} = -5 \text{ Vdc}$			3.0		600		300	660		960	
(Vin = ±0.25 Vdc)				_	600	- i-	280	660		960	ALL TRACT
(V <sub>in</sub> = +7.5 Vdc)			7,5		360	87.91	240	400	1 45-90	600	NO MAIN
(Vin = -7.5 Vdc) VSS = -7.5 Vdc	h	Steel .	7.5	lav	360	-	240	400	_	600	10
(Vin = ±0.25 Vdc)		V - 3	0.814	01.5.10	360	_	180	400	09 E 01	600	101
(Vin = +10 Vdc)	6	- V 3	10	gy or 8	600	_(2)	260	660	loV_Luci	960	of book
(Vin = +0.25 Vdc) VSS = 0 Vdc		Am			600	-	310	660	D = 10	960	
(Vin = +5.6 Vdc)		Am		_	600	-	310	660	-	960	
(Vin = +15 Vdc)			15	_	360	-	260	400	an Jan	600	10
(Vin = +0.25 Vdc) VSS = 0 Vdc		Wen		700	360	_	260	400	nolisa	600	
(V <sub>in</sub> = +9.3 Vdc)		01	160	61.20	360	-	300	400	unam di	600	18
'ON" Resistance (CL/CP Device)**	4,5,6	RON		181			ill Solderen	poell-8	emine	STREET PA	Ohms
$V_C = V_{DD}$ , $R_L = 10 k\Omega$ )			record gr	m sple	o to this d	ganni	nation arms	ed caul		ings are	aS mus
(Vin = +5.0 Vdc)			5.0	10-01	610	D +100	300	660	Shirt 9	840	mustania
$(V_{in} = -5.0 \text{ Vdc}) V_{SS} = -5 \text{ Vdc}$			0.98	01-076	610	15-15	300	660	-	840	
$(V_{in} = \pm 0.25 \text{ Vdc})$				-	610	-	280	660	_	840	-
(V <sub>in</sub> = +7.5 Vdc)		trico	7.5	enzage	370	loanu0	240	400	TOTA DE	520	iveb a
$(V_{in} = -7.5 \text{ Vdc}) V_{SS} = -7.5 \text{ Vdc}$		-0136	e or nex	500 E	370	- Library	240	400	DENISON O	520	BOY ON
(V <sub>in</sub> = ±0.25 Vdc)	1 1	- Dani	s Harmo	od olo	370	bhis a	180	400	3 -5-1	520	nebec
(V <sub>in</sub> = +10 Vdc)			10	-	610	-	260	660	四年) 3	840	ten ent
(Vin = +0.25 Vdc) VSS = 0 Vdc		10.4	19,00	ORMOV	610	ligno	260	660	eals to	840	disect of
(V <sub>in</sub> = +5.6 Vdc)				-	610	THE B	310	660	love (	840	18 × 103
(V <sub>in</sub> = +15 Vdc)		-	15	-	370	-	260	400	-	520	-
(V <sub>in</sub> = +0.25 Vdc) V <sub>SS</sub> = 0 Vdc (V <sub>in</sub> = +9.3 Vdc)	1 - A			_	370 370	_	260 300	400		520 520	
		10		-	1	-		1.50		020	101
"ON" Resistance Between any 2 circuits in a common	7.0	ARON	1,275			anna	DAIN NO			P I BELL	Ohms
package					1	PAICS-C	Someo s	2356			
(VC = VDD)				75	1						
(V <sub>in</sub> = ±5.0 Vdc) V <sub>SS</sub> = -5 Vdc			5.0	_	_	_	15	_	_	_	
(V <sub>in</sub> = ±7.5 Vdc) V <sub>SS</sub> = -7.5 Vdc			7.5	-	10-	-<	10	T (0_2) r/ (0	_	_	
nput/Output Leakage Current (V <sub>C</sub> = V <sub>SS</sub> )	_	_									
(V <sub>in</sub> = +7.5, V <sub>out</sub> = -7.5 Vdc)			7.5	-	±0.100	_	±0.0015	±0.100	_	±1.0	μAde
(V <sub>in</sub> = -7.5, V <sub>out</sub> = +7.5 Vdc)		100	7.5		±0.100		±0.0015	±0.100		±1.0	

 $<sup>^{\</sup>circ}$ T $_{low}$  =  $-55^{\circ}$ C for AL Device,  $-40^{\circ}$ C for CL/CP Device. T $_{high}$  =  $+125^{\circ}$ C for AL Device,  $+85^{\circ}$ C for CL/CP Device.

NOTE: All unused inputs must be returned to  $V_{\mbox{DD}}$  or  $V_{\mbox{SS}}$  as appropriate for the circuit application.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*For voltage drops across the switch (ΔV<sub>switch</sub>) >600 mV (>300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn; i.e., the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

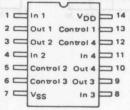
### MC14016B

### ELECTRICAL CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

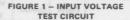
Characteristic	Figure	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Propagation Delay Time (VSS = 0 Vdc)	7	tPLH,	5.0	-	15	45	ns
Vin to Vout	-	tPHL	10	-	7.0	15	
(V <sub>C</sub> = V <sub>DD</sub> , R <sub>L</sub> = 10 kΩ)	1 1		15	_	6.0	12	
Control to Output	8	tPHZ.	5.0	+	34	90	ns
$(V_{in} \le 10 \text{ Vdc}, R_L = 1.0 \text{ k}\Omega)$	-3/3/	tPLZ.	10		20	45	
17 In 7 10 700, 11 1.0 KW	4463	tPZH-	15	_	15	35	
Crosstalk, Control to Output (VSS = 0 Vdc)	9	†PZL	5.0	+	30		mV ·
$(V_C = V_{DD}, R_{in} = 1.0 \text{ k}\Omega, R_{out} = 10 \text{ k}\Omega,$	1186		10		50		
f = 1kHz)			15		100	_	
	-	W # (2 W 100	5.0	21 SARIES	-80		dB
crosstalk between any two switches (VSS = 0 Vdc) (R <sub>I</sub> = 1.0 k $\Omega$ , f = 1.0 MHz,	V asv	sV. etta A	5.0	STY -	-80	_	db.
$crosstalk = 20 log_{10} \frac{Vout1}{V_{out2}}$	DOM: THE BY	Follows Arts	BON D	W-SYN	Alle: Apple		
							111/0
loise Voltage (VSS = 0 Vdc)	10,11	-	5.0	-	24	-	nV/√Cycle
(VC = VDD, f = 100 Hz)		1 10	10	ne amor	25	10000 10	IRUDA
			15	THE	30	elinist - 2	INSTRUCTION OF THE PERSON OF T
(VC = VDD, f = 100 kHz)	10.01		5.0	-	12	-	
	101		10	-	12	-	
			15	07V e	15		
Second Harmonic Distortion (VSS = -5 Vdc)	-	-	5.0	- 1	0.16	-	%
(Vin = 1.77 Vdc RMS Centered @ 0.0 Vdc,	141 E						
R <sub>L</sub> = 10 kΩ, f = 1.0 kHz)	1. 18		and the same	1			
nsertion Loss ( $V_C = V_{DD}$ , $V_{in} = 1.77$ Vdc, $V_{SS} = -5$ Vdc, RMS centered = 0.0 Vdc, $f = 1.0$ MHz)	12	-	5.0	-(a			dB
$I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$	20.	E. S		nie V o	auv		
(R <sub>L</sub> = 1.0 kΩ)		Kors			2.3	WALL TO	
$(R_L = 10 \text{ k}\Omega)$	100		- 1 9	lotted.	0.2	110.2	401.JS
$(R_1 = 100 \text{ k}\Omega)$	1 3			high	0.1	_	Gunnerstor
$(R_L = 1.0 M\Omega)$		-	1		0.05		
andwidth (-3 dB)	12,13	BW	5.0	44-4	DEV.		MHz
(VC = VDD, V <sub>in</sub> = 1.77 Vdc, V <sub>SS</sub> = -5 Vdc, RMS centered @ 0.0 Vdc)	12,10		3.0	+		017 00	W = C1 4
$(R_L = 1.0 k\Omega)$		TO BE SEE		-	54	_	
(R <sub>L</sub> = 10 kΩ)		1		-	40	_	
(R <sub>L</sub> = 100 kΩ)				-	38	-	
$(R_L = 1.0 M\Omega)$	PIL PLICE	Lineral La	SHEET	-	37	-	
OFF Channel Feedthrough Attenuation (Vss = -5 Vdc)	-	-	5.0	DMA V D	5- × 20V	- a arkus	kHz
$(V_C = V_{SS}, 20 \log_{10} \frac{V_{out}}{V_{in}} = -50 \text{ dB})$		-					700
(R <sub>L</sub> = 1.0 kΩ)	-	+ ace - /	9	-	1250	4-0	1
$(R_L = 10 \text{ k}\Omega)$		- 31/25 - A	1	-	140		000
$(R_1 = 100 \text{ k}\Omega)$				_	18		
$(R_L = 1.0 M\Omega)$	100				2.0		

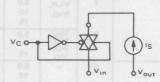
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

PIN ASSIGNMENT



#### MC14016B

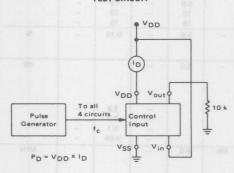




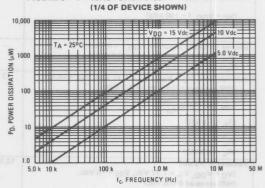
$$\begin{split} &V_{IL} \colon V_{C} \text{ is raised from V}_{SS} \text{ until } V_{C} = V_{IL}, \\ &\text{at } V_{C} = V_{IL} \colon I_{S} = \pm 10 \text{ } \mu\text{A} \text{ with } V_{in} = V_{SS}, V_{out} = V_{DD} \text{ or } V_{in} = V_{DD}, V_{out} = V_{SS}. \end{split}$$

VIH: When VC = VIH to VDD, the switch is ON and the RON specifications are met.

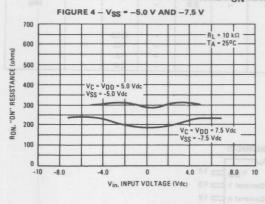
# FIGURE 2 – QUIESCENT POWER DISSIPATION TEST CIRCUIT



### FIGURE 3 - TYPICAL POWER DISSIPATION PER CIRCUIT



#### TYPICAL RON versus INPUT VOLTAGE



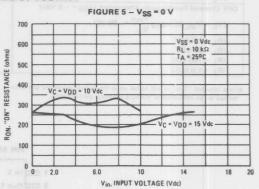


FIGURE 6 - RON CHARACTERISTICS TEST CIRCUIT

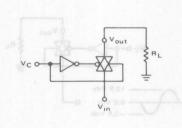


FIGURE 7 - PROPAGATION DELAY TEST CIRCUIT

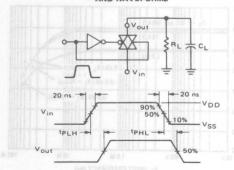


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT
AND WAVEFORMS

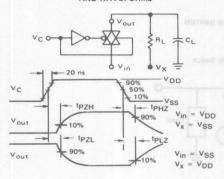


FIGURE 9 - CROSSTALK TEST CIRCUIT

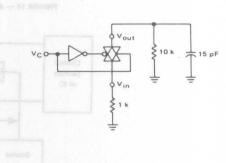


FIGURE 10 - NOISE VOLTAGE TEST CIRCUIT

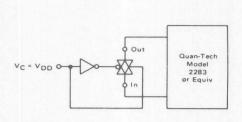
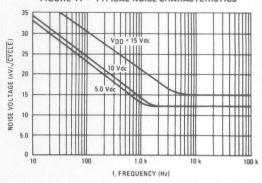


FIGURE 11 - TYPICAL NOISE CHARACTERISTICS



.

### MC14016B

FIGURE 12 — TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS

2.0

R<sub>L</sub> = 1 M $\Omega$  and 100 k $\Omega$ 10 k $\Omega$ -3.0 d8 (R<sub>L</sub> = 1.0 M $\Omega$ )

-3.0 d8 (R<sub>L</sub> = 1.0 k $\Omega$ )

-10

-10

-10

10 k 100 k 1.0 M 10 M 100 M

fin. INPUT FREQUENCY (Hz)

FIGURE 13 - FREQUENCY RESPONSE TEST CIRCUIT

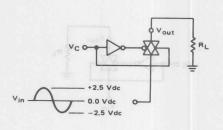
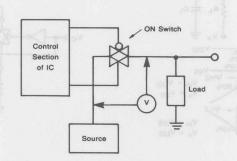


FIGURE 14 - AV ACROSS SWITCH





#### MC14016B

#### **APPLICATIONS INFORMATION**

Figure A illustrates use of the Analog Switch. The 0-to-5 V Digital Control signal is used to directly control a 5  $V_{p-p}$  analog signal.

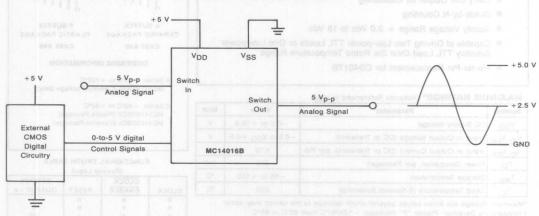
The digital control logic levels are determined by  $V_{DD}$  and  $V_{SS}$ . The  $V_{DD}$  voltage is the logic high voltage; the  $V_{SS}$  voltage is logic low. For the example,  $V_{DD} = +5V = logic$  high at the control inputs;  $V_{SS} = GND = 0V = logic$  low.

The maximum analog signal level is determined by  $V_{DD}$  and  $V_{SS}$ . The analog voltage must not swing higher than  $V_{DD}$  or lower than  $V_{SS}$ .

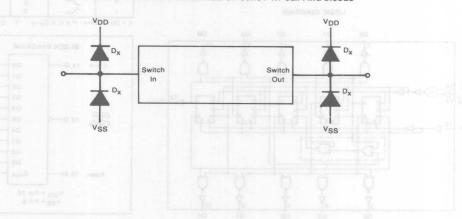
The example shows a 5  $V_{p-p}$  signal which allows no margin at either peak. If voltage transients above  $V_{DD}$  and/or below  $V_{SS}$  are anticipated on the analog channels, external diodes  $(D_X)$  are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between Vpp and Vss is 18.0V. Most parameters are specified up to 15V which is the recommended maximum difference between Vpp and Vss.

#### FIGURE A - APPLICATION EXAMPLE



#### FIGURE B - EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES



### MC14017B

#### **DECADE COUNTER**

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

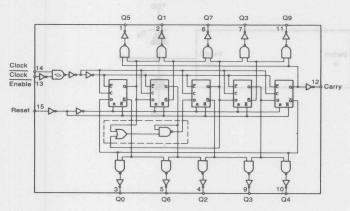
- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TI	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

#### LOGIC DIAGRAM



#### **CMOS MSI**

(LOW POWER COMPLEMENTARY MOS)
DECADE COUNTER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

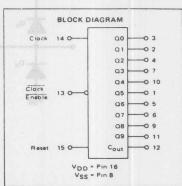
A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

# FUNCTIONAL TRUTH TABLE (Positive Logic)

CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT : n
0	×	0	n
×	1	0	n
×	×	1	00
5	0	0	n+1
~ me	×	0	n
×	5	0	n
1	~	0	n+1

X = Don't Care If n <5 Carry = "1", Otherwise = "0"



.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to Voc.) 10088 8 AT 18 68 8 JOIN 2010 BERTOARANO BY MOTURE

Held wild brend	este	VDD	Tic	w*		25°C		Thigh*		
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	1	0.05	-	0	0.05	Pinyan d.1	0.05	Vdc
V V 0000	0.	10	-	0.05	-	0	0.05	-upan u.	0.05	14.144
vin = vDD or u		15	-	0.05	-	0	0.05	Gign GXA	0.05	14317
	VOH	5.0	4.95		4.95	5.0		4.95	edsti novi	Vdc
	- OH	10	9.95	197	9.95	10	_	9.95	WHEN HOW	(Sedistra
V <sub>in</sub> = 0 or V <sub>DD</sub>		15	14.95	HPHI	14.95	15		14.95	south of t	Pese
Input Voltage "0" Level	VIL	-				-		-	- 1777	Vdc
0.00	12	5.0		1.5	1	2.25	1.5	0.08 hard 10.5 Taurit	1.5	1
$(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$ $(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$		10	La	3.0	_	4.50	3.0	MAN GOLD	3.0	4,197
		15		4.0		6.75	4.0	giniT	4.0	figration, a
(V <sub>O</sub> = 13.5 or 1.5 Vdc) "1" Level	VIH			11/41					1004 02 X	-
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$	·III	5.0	3.5		3.5	2.75	(E 1575)	3.5	a Telai i	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)	7 1277	10	7.0	_ 1	7.0	5.50	+ 10.13	7.0	* 4Hq1 .	1141
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0		11.0	8.25	1 501	11.0	" algorithm	A PAIL
Output Drive Current (AL Device)	lou	10	11.0	1341	11.0	0.20		11.0	rateChoose	mAdo
(V <sub>OH</sub> = 2.5 Vdc) Source	ЮН	5.0	-3.0	1114	-2.4	-4.2		-1.7	s to Daud	IIIAGG
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88	10 + 10 (	-0.36	* JMQF.,	1995
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6		-1.3	-2.25	100	-0.36	- JEST /	1:12
(V <sub>OH</sub> = 13.5 Vdc)	-	15	-4.2		-3.4	-8.8	N F 33 1	-2.4	7 <u>98</u> 97	1192
		-	0.64	191	-	1	Day Laborator		T VIII	- A d
(V <sub>OL</sub> = 0.4 Vdc) Sink	OL	5.0	1.6		0.51	0.88	-	0.36	nuo Dour	mAde
(V <sub>OL</sub> = 0.5 Vdc)		10 15	4.2	-	3.4	8.8	57.610 an 581	2.4	25.77	197
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	0.0	an Cat o	2.4		Just .
Output Drive Current (CL/CP Device)	ІОН	L' BY				1.0	m 001	10 (39)		mAdd
(V <sub>OH</sub> = 2.5 Vdc) Source	950	5.0	-2.5	- T	-2.1	-4.2	-	-1.7	STORY OF	Atroit I
$(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$	001	5.0	-0.52	1000-	-0.44	-0.88	-	-0.36	-	
(V <sub>OH</sub> = 3.5 Vdc)	25	10	-1.3	-	-1.1	-2.25		-0.9	_	
	1	15	-3.6	-	-3.0	-8.8		-2.4	-	100010
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdo
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3	-	1.1	2.25	-	0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)	1000	15	3.6		3.0	8.8	-	2.4	September 1987	
Input Current (AL Device)	lin	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 1.0	μAdd
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	± 1.0	μAdd
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	- 0.1		mgs <sup>2</sup>	-	5.0	7.5	- ac	T letoms	pF
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdd
(Per Package)	00	10		10	-	0.010	10	Files ba	300	1000
Signal Lacet		15		20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20		0.005	20	- 1	150	μAdd
(Per Package)	386	10	-	40	_	0.010	40	smiT o	300	prior.
	000	15		80		0.015	80	40000	600	
Total Supply Current**1	IT	5.0		- 00	1 10	.27 µA/kHz			000	μAdo
(Dynamic plus Quiescent,		10				.55 μA/kHz		12.11		
Per Package)	0.8%	15								Stock E
(C <sub>1</sub> = 50 pF on all outputs, all	200-				1T = (0	.83 μA/kHz	) 1 + 1 DD	)		1
buffers switching)	01-7									

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is

intended as an indication of the IC's potential performance.

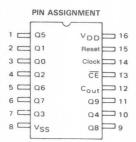
†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: I\_T is in  $\mu$ A (per package), C\_L in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.0011.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in})$  or  $V_{out}) \leq V_{DD}$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.



<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

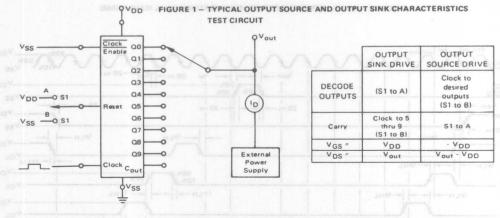
SWITCHING CHARACTERISTICS\* (C1 = 50 pF. TA = 25°C)

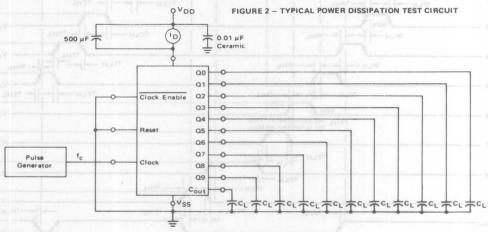
Characteristic		Symbol	V <sub>DD</sub> Vdc	Min	Typ#	Max	Unit
Output Rise and Fall Time		tTLH.					ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns		THL	5.0	JOV	100	200	How Turque
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns		140.0	10	_	50	100	BUT HE
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	40.0 -	15		40	80		
Propagation Delay Time	4-1	-	moV -	The second second	-	ns	
Reset to Decade Output		tPLH,				Voc	1 2 - m
tplH tpHL = (1.7 ns/pF) CL + 415 ns		tPHL	5.0		500	1000	
tp_H, tpHL = (0.66 ns/pF) CL + 197 ns			10	nV.	230	460	array ros
		8.7	15		175	350	0.00
tPLH, tPHL = (0.5 ns/pF) CL + 150 ns		20.0	15	_	175	350	
Propagation Delay Time		tPLH,				WEI HER	ns
Clock to Cout		tPHL		1 4/4	west to the		1
tpLH, tpHL = (1.7 ns/pF) CL + 315 ns			5.0	-	400	800	N + 849
tPLH, tPHL = (0.66 ns/pF) CL + 142 ns			10	-	175	350	(VO +
tPLH, tPHL = (0.5 ns/pF) CL + 100 ns			15	-	125	250	1 - 16:30
Propagation Delay Time		tPLH,			Teores C	CAL Thomas of	ns
Clock to Decode Output		tPHL		HOT	and the same of	IDDV 8 S	weeks A
tpLH, tpHL = (1.7 ns/pF) CL + 415 ns		1 45	5.0	-	500	1000	HOV3
tPLH. tPHL = (0.66 ns/pF) CL + 197 ns			10	-	230	460	H ROV
tpLH, tpHL = (0.5 ns/pF) CL + 150 ns		0	15	-	175	350	HOW
Turn-Off Delay Time		tPLH		-		Dod Vision	ns
Reset to Cout		1		104	No. of the latest	(500 670	1 1000
to = (1 7 ns/nF) C. + 315 ns		- 1 3	5.0	- 1	400	800	+ JOY)
tpl H = (0.66 ns/pF) Cl + 142 ns			10		175	350	JOY
tplH = (0.5 ns/pF) CL + 100 ns			15	1 0401	125	250	-I-O lunt
Clock Pulse Width	-	t <sub>w(H)</sub>	5.0	250	125		ns
86.0-1-56.0-		·W(H)	10	100	50	CHOV B.	No.
			15	75	35	F2 3 E 2	HOW
Clock Frequency	0.0	-	5.0		5.0	2.0	MHz
BE O BE O		fcl	10	100	12	5.0	1000
		- 1 0	15		16	6.7	4 1941
Reset Pulse Width				500	250	0.7	H ROAT
Reset Pulse Width		tw(H)	5.0	500 250	125	salvo G JAJ n	ns
		1000	15	190	95	0 830 F31 B	STATE OF THE
	-	-			-	2000	1000
Reset Removal Time		trem	5.0	750	375	-	ns
		-	10	275	135	-	3 - 100
0.008 5.0 - 150 BAd		0.8	15	210	105	O 1 12 7 7 1 1 1 1 1 1 1	H Tracks
Clock Input Rise and Fall Time		tTLH-	5.0				-
	tTHL	10		No Limit			
0.005 20 1.000		20	15	l ost	Figures)	931 JUL78011	J 719382
Clock Enable Setup Time		t <sub>su</sub>	5.0	350	175	- 3996	ns
		08	10	150	75	-	
			15	115	52	L'ingress	la sur al
Clock Enable Removal Time	05 = +1		5.0	420	260	SCHOOL SOUR	ns
	trem	10	200	100	Espis	Par P ac	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

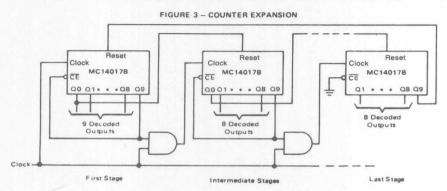
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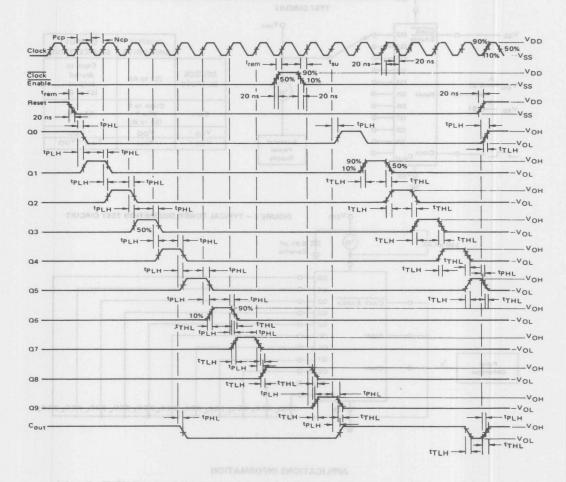
#### APPLICATIONS INFORMATION

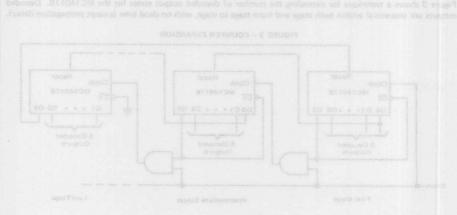
Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



### MC14017B

#### FIGURE 4 - AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS







## PRESETTABLE DIVIDE-BY-N COUNTER

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective  $\overline{\Delta}$  outputs (inverted). A logic 1 on the reset input will cause all  $\overline{\Delta}$  outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate  $\overline{\Omega}$  outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

- Fully Static Operation
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018B

### MAXIMUM RATINGS\* (Voitages Referenced to VSS)

Symbol	Parameter Place	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	N.
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{Out}) \leqslant V_{DD}.$  Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

### MC14018B

### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

PRESETTABLE DIVIDE-BY-N COUNTER





L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

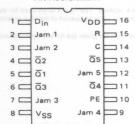
C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	Ön
~	0	0	×	Qn
	0	0	×	D <sub>n</sub>
X	0	1	0	1
X	0	1	1	0
×	1	X	X	1

\*Dn is the Data input for that stage Stage 1 has Data brought out to Pin 1.

#### PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD		ow*		25°C		Thi	igh *	1
Characteristic	Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Uni
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdd
Vin = VDD or 0	0.	10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05		0.05	
130M VAATMAMA 19MO1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	_	Vdd
V <sub>ID</sub> = 0 or V <sub>DD</sub>	TOH	10	9.95		9.95	10		9.95	_	
III O S. V DD		15	14.95	27-01	14.95	15	CD 02-1103	14.95	200-	
Input Voltage "0" Level	VIL				1					Vdo
(VO = 4.5 or 0.5 Vdc)	- IL	5.0	e double	15	HURSE OF	2.25	1.5	D B810	1.5	1
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	42 STB C	3.0	arl 7 als	4.50	3.0	92174	3.0	asyn
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	zlock	4.0	De palo	6.75	4.0	don't house	4.0	prets
"1" Level	VIH	13	elor side	4.0	Britt No.	0.73	S Device le	00000000	D00318-9	1
(VO = 0.5 or 4.5 Vdc)	VIH	5.0	3.5	South par	3.5	2.75	The st	3.5	WHE 65	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50		7.0		- vac
	Street, Street	15		NA -THE		8.25	str f ore	11.0	1 5000	1 %
(V <sub>O</sub> = 1 5 or 13.5 Vdc)	1000	15	11.0		11.0	8.25	28 T 319	11.0	09 134 17	mAd
Output Drive Current (AL Device)	ЮН	A	05866	THE REAL PROPERTY.	24	01 5 mo	AND PRESENTA	-1.7		
(VOH = 2.5 Vdc) Source	In Inc.	5.0	-3.0	in part, al	-2.4	-4.2	Ne-D o	-0.36	E 501738	1000
(V <sub>OH</sub> - 4.6 Vdc)	it.	5.0	-0.64	MODE SI	-0.51	-0.88	01051 71	-0.36	numerius?	antz
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	BE TROOT	-0.9	or 1820 ft 104	SIM
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	-		- ·	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	051	0.88	- I	0.36	-	mAd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.25	EL STORY	0.9		6
(VOL = 1.5 Vdc)		15	4.2	3 12 160	3.4	8.8	AT THE	2.4	o ordede	200
Output Drive Current (CL/CP Device)	IOH		1	man Bill	o fuldin	DESTRUCT D	ELL TENTO	0200 210	S. FABRURE	mAd
(VOH = 2.5 Vdc) Source	2 1	5.0	-2.5	- 1	-2.1	-4.2	not-snerr	-1.7	n 9 - ot - o	9 10
(VOH = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(VOH = 13.5 Vdc)		15	-3.6		-3.0	-8.8	-	-2.4		
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88		0.36	-	mAd
(VOI = 0.5 Vdc)	0.	10	1.3	-	1.1	2.25		0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	_	3.0	8.8	-	2.4		
Input Current (AL Device)	lin	15		± 0.1		±0.00001	±0.1	_	± 1.0	μAdo
Input Current (CL/CP Device)		15	1	± 0.3	-	±0.00001	± 0.3		±1.0	μAde
	lin		-	20.5	-	5.0			-1.0	DF
(V <sub>in</sub> 0)	Cin					5.0	7.5			PF
Quiëscent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAd
(Per Package)		10		10	(SS)	0.010	10	SAL CHA	300	20 660 27
100 x 2 2 1		15	aul	20	-	0.015	20	9	600	Store
Quiescent Current (CL/CP Device)	IDD	5.0	D. 771 1	20		0.005	20	mindel	150	μAd
(Per Package)	200	10	-	40	-	0.010	40	-	300	1
		15	102 00	80	-	0.015	80	MINOV PUR	600	Line
Total Supply Current**†	IT	5.0	1 107	B. L.	1 <sub>T</sub> = (0	).3 µA/kHz)	f+ Inn	pur Duras	UG. 10 ) / 9	μAd
(Dynamic plus Quiescent,		10	100			).7 µA/kHz)				
Per Package)	Se 1	15				I.O µA/kHz)				1
(C <sub>1</sub> 50 pF on all outputs, all	310		TRUE AND							1
buffers switching)			86							

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: IT is in  $\mu$ A (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

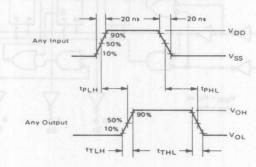
<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

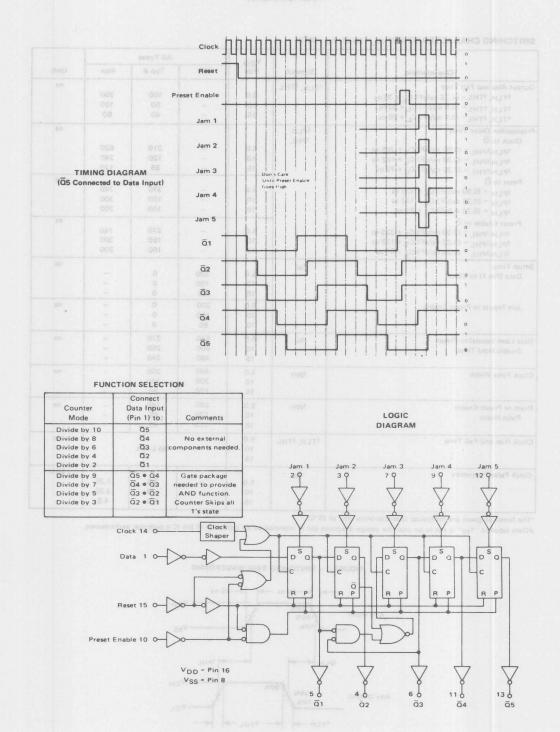
	The state of the s	VDD		All Types		
Characteristic	Symbol	Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	TLH, THL					ns
tTLH, tTHL = (1.35 ns/pF) C1 + 32 ns	1.2.1.,	5.0	algeriä rager	100	200	
tTLH tTHL = (0.6 ns/pF) CL + 20 ns		10	-	50	100	
tTLH, tTHL = (0.4 ns/pF) CL + 20 ns		15	- 1	40	80	
Propagation Delay Time	tPLH,					ns
Clock to Q	tPHL					
tpLH,tpHL = (0.90 ns/pF) CL + 265 ns	1 4 4 1 1 1	5.0	2.020	310	620	
tpLH,tpHL = (0.36 ns/pF) CL + 102 ns		10	-	120	240	
tpLH.tpHL = (0.26 ns/pF) CL + 72 ns		15	0.070	85	170	
Reset to Q	1 300 February	-u		favorit sa	on barrens	ns
tpLH = (0.90 ns/pF) CL + 325 ns		5.0	-	370	740	
tpLH = (0.36 ns/pF) CL + 132 ns		10	Pringe.	150	300	
tPLH = (0.26 ns/pF) CL + 81 ns		15	-	100	200	
Preset Enable to Q		TITT	101195			ns
tpLH,tpHL = (0.90 ns/pF) CL + 325 ns		5.0	-	370	740	
tpLH,tpHL = (0.36 ns/pF) CL + 132 ns		10	10	150	300	
tPLH, tPHL = (0.26 ns/pF) CL + 81 ns	-	15	-	100	200	
Setup Time	t <sub>su</sub>	Territ				ns
Data (Pin 1) to Clock	100	5.0	200	0	-	
		10	100	0	- 1	
		15	80	0	_	
Jam Inputs to Preset Enable		5.0	200	0	-	ns
		10	100	0	_	
		15	80	0	-	
Data (Jam Inputs)-to-Preset	th	5.0	540	270	-	ns
Enable Hold Time		10	500	250	_	
		15	480	240	_	
Clock Pulse Width	twH	5.0	400	200	_	ns
	1	10	200	100	5(1)-(u <del>n</del> 2)-3	
		15	160	80	311 (3812-1	
Reset or Preset Enable	tWH	5.0	290	145	-	ns
Pulse Width		10	130	65	1 _ 100	Rest O
WARDARD		15	110	55		traft/
Clock Rise and Fall Time	tTLH, tTHL	5.0	Guerra no oct	124	81.0	ns
	TLH, THE	10	amountains make	No Limit	8.99	Fight of
		15		Cirint		Miles II
Clock Pulse Frequency	f <sub>cl</sub>					MHz
	,CI	5.0	BRYSHE RIED	2.5	1.25	deline of
	57	10		6.5	3.25	ab v
	1 X	15	AND THE	8.0	4.0	able 0
		10	THE R. P. LEWIS CO. P.	0.0	4.0	Paradolis (1)

<sup>\*</sup>The formulas given are for typical characteristics only at 25°C.

#### FIGURE 1 - SWITCHING TIME WAVEFORMS



<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.





### MC14020B

#### 14-BIT BINARY COUNTER

The MC14020B 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4020B

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

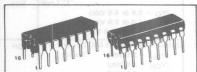
Symbol	Parameter Parameter	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin. lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

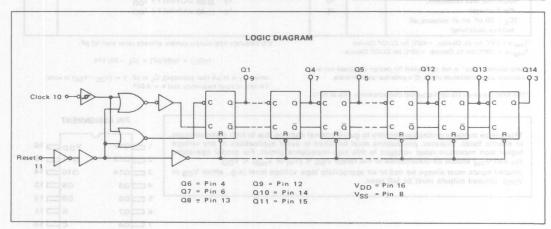
A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
5	0	No Change
~	0	Advance to next state
X	1	All Outputs are low

X = Don't Care



FI FCTRICAL CHARACTERISTICS (Voltages Referenced to VS

		VDD	Tio	w*		25°C		Thi	gh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "O" Level	VOI	5.0	-	0.05		0	0.05	-	0 05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	-	10	-	0.05	-	0	0.05		0.05	
Vin VDD or o		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	(F) LIZ T	4.95	-	Vdc
Vin = 0 or VDD	- On	10	9.95	_	9.95	10	_	9.95		
M POWER COMPLEMENTARY MOST		15	14.95	i desta Transco	14.95	15	-1	14.95		100
	VIL	-								Vdc
	AIL	5.0	nom sign	1.5	CHARD SIX	2.25	1.5	INPROD-M	1.5	STATE OF THE PARTY
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		10	Closus 8	3.0	io ne dia	4.50	3.0	BIET SE	3.0	offile.
$(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$		15	101010 37	4.0	Noo Alei	6.75	4.0	SECRETE 1	4.0	estic
(V <sub>O</sub> = 13.5 or 1.5 Vdc) "1" Level		15	All Parks	4.0	Pagino e	0.75	part male	10 1111111	0117 616	the late
	VIH	5.0	100	controls	3.5	2.75		3.5		Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$		5.0	3.5		1000	5.50		7.0	r-bigib-	VUC
$(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$		10	7.0		7.0 .			1		
(V <sub>0</sub> = 1.5 or 13.5 vdc)		15	11.0	-	11.0	8.25		11.0		-
Output Drive Current (AL Device)	ІОН					111		ETP GROUP		mAde
(V <sub>OH</sub> = 2.5 Vdc) Source	E llas	5.0	-3.0	-	-2.4	-4.2	GET HA	-1.7	1007 900	0 9
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	75	-0.51	-0.88	0 5 = 00	-0.36	InV vior	2 6
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6		-1.3	-2.25		-0.9	- 1	
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	enG-re.	-3.4	-8.8	wall aw	-2.4	to elder	0 8
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	<u> 100000</u>	0.51	0.88	an sev	0.36	F. F. Methods	mAde
$(V_{OL} = 0.5 \text{ Vdc})$		10	1.6	1 15/19	1.3	2.25	oline line	0.9	er East	
$(V_{OL} = 1.5 \text{ Vdc})$		15	4.2		3.4	8.8	-	2.4	-	
Output Drive Current (CL/CP Device)	ІОН							SHLL 7901	OF THE REAL PROPERTY.	mAde
(VOH = 2.5 Vdc) Source	0	5.0	-2.5	_	-2.1	-4.2	to the	-1.7	ni@not-	19 0
(V <sub>OH</sub> = 4.6 Vdc)	t A	5.0	-0.52	-	-0.44	-0.88		-0.36	-	
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	_	-0.9	-	
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6		-3.0	-8.8	-	-2.4	-	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	_	0.36	_	mAde
(V <sub>OL</sub> = 0.5 Vdc)	·OL	10	1.3		1.1	2.25		0.9		-
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	_	3.0	8.8	á -ma	2.4	STAR W	LINELD
nput Current (AL Device)	1.	15	-	± 0.1	-	± 0.00001	±0.1	-	11.0	μAdo
	lin	15	1912/19	± 0.3	-	±0.00001	± 0.3	-	11.0	μAdd
nput Current (CL/CP Device)	lin	15	100-0	₹0.3	-			bandos	3 1.0	-
nput Capacitance (V <sub>in</sub> = 0)	Cin	V	9+ 60	p 8 0 -	-	5.0	7.5	alloV heg	aO to tuju	pF
Quiescent Current (AL Device)	1pp	5.0		5.0	18-19-1	0.005	5.0	1812 100	150	μAde
(Per Package)		10	- 00	10	-	0.010	10	Pation, pa	300	1
nghan2 ovi 8	-1	15	The same	20	-	0.015	20	anulose	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20		150	μAd
(Per Package)	UU	10	- 00	40		0.010	40	OT BYWEIGH	300	
A STATE OF THE PARTY OF THE PAR	I	15	1000 years	80	t of appar	0.015	80	disv_prevo	600	FF Noue
Total Supply Current**†	IT	5.0	91	11 11 11 11	1= = (0	.42 µA/kHz	-	0.0412804	geotessy	μAd
(Dynamic plus Quiescent,		10	J. Bar			.85 µA/kHz				I AAU
Per Package)		15				.43 µA/kHz				
(CL = 50 pF on all outputs, all buffers switching)		13			.1 - (1	אחזיים בייי	,			

 $<sup>^{\</sup>circ}\text{T}_{\text{low}} = -55^{\circ}\text{C}$  for AL Device,  $-40^{\circ}\text{C}$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

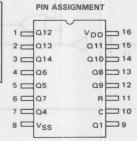
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



Thigh = + 125°C for AL Device, +85°C for CL/CP Device.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

AND AT Characteristic MAGE SECTION	Symbol	V <sub>DD</sub> V <sub>dc</sub>	Min	Typ#	Max	Unit
Output Rise and Fall Time	tTLH,		TUT			ns
T <sub>TLH</sub> , T <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTHL	5.0		100	200	1020
T <sub>TLH</sub> , T <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns		10	-	50	100	
T <sub>TLH</sub> , T <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		15		40	80	- 10
Propagation Delay Time	tpLH,					- 10
Clock to Q1	tPHL		lane.			ns
tpHL, tpLH = (1.7 ns/pF) CL + 175 ns		5.0	_	260	520	85
tpHL, tpLH = (0.66 ns/pF) CL + 82 ns		10	_	115	230	-
t <sub>PHL</sub> , t <sub>PLH</sub> = (0.5 ns/pF) C <sub>L</sub> + 55 ns		15	_	80	160	YD
Clock to Q14						ns
tpHL, tpLH = (1.7 ns/pF) CL + 1735 ns		5.0		1820	3900	- ao-
tpHL, tpLH = (0.66 ns/pF) C <sub>L</sub> + 772 ns		10	_	805	1725	
t <sub>PHL</sub> , t <sub>PLH</sub> = (0.5 ns/pF) C <sub>L</sub> + 535 ns		15	-	560	1200	010
Propagation Delay Time Reset to Qn	<sup>†</sup> PHL					ns
tpH = (1.7 ns/pF) C <sub>1</sub> + 285 ns		5.0	_	370	740	810
tpHL = (0.66 ns/pF) C <sub>L</sub> + 122 ns		10	_	155	310	
t <sub>PHL</sub> = (0.5 ns/pF) C <sub>L</sub> + 90 ns		15	_	115	230	200
Clock Pulse Width	twH	5.0	500	140	_	ns
		10	165	55	_	
		15	125	38	_	
Clock Pulse Frequency	f <sub>cl</sub>	5.0	_	2.0	1.0	MHz
		10		6.0	3.0	
		15	_	8.0	4.0	
Clock Rise and Fall Time	tTLH, tTHL	5.0	TENSET.			_
		10		No Limit		
		15				
Reset Pulse Width	twL	5.0	3000	320	_	ns
		10	550	120	-	
		15	420	80	_	
Reset Removal Time	t <sub>rem</sub>	5.0	130	65	_	ns
		10	50	25	_	
	3	15	30	15	_	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C. #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

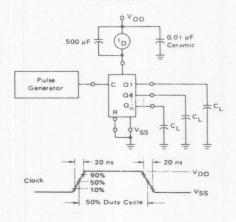
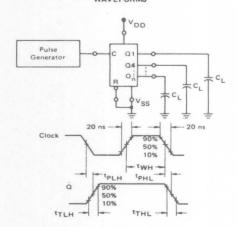
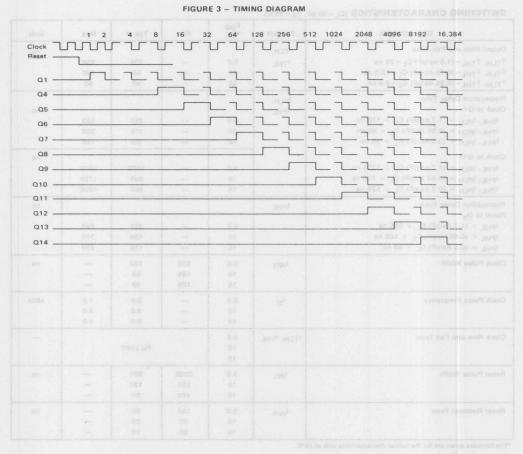


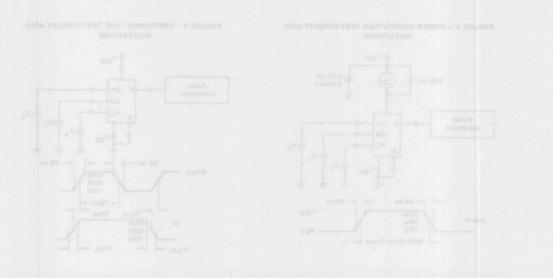
FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



### MC14020B







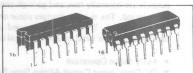
## MC14021B

FOR COMPLETE DATA **SEE MC14014B** 

### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER



CERAMIC PACKAGE

PLASTIC PACKAGE CASE 620 CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

# TRUTH TABLE

ERI	AL OPER			TABLE		
t	CLOCK	DS	P/S	Q6 t = n+6	Q7 t=n+7	Q8 t = n+8
n		0	0	0	2	?
n+1	5	1	0	1	0	7
n+2	_	0	0	0	25.11	0
n+3	5	1	0	1	0	1
2		X	0	06	Q7	08

#### PARALLEL OPERATION:

CLOCK		0	PiS	D.	•QM	
MC14014B N	DS	P/S	РМ			
	X	X	1	0	0	
	X	X	1	1	1	

\*Q6, Q7, & Q8 are available externally X = Don't Care

#### 8-BIT STATIC SHIFT REGISTER

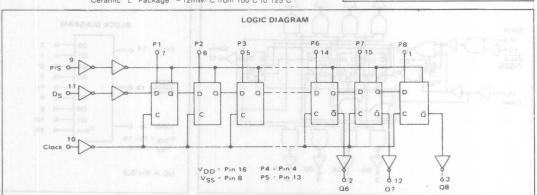
The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- · Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit	
VDD	DC Supply Voltage	-05 to +180	V	
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧	
lin-lout	Input or Output Current (DC or Transient), per Pin	± 10	mA	
PD	Power Dissipation, per Package†	500	mW	
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C	
TL	Lead Temperature (8-Second Soldering)	260	°C	

\*Maximum Ratings are those values beyond which damage to the device may occur †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C



### MC14022B

### **OCTAL COUNTER**

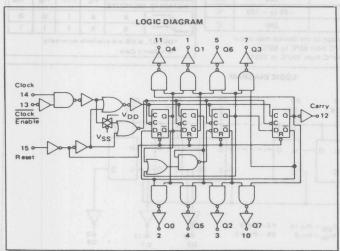
The MC14022B is a four-stage Johnson octal counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4022B

#### MAXIMUM RATINGS\* (Voltages Referenced to Vec.)

Symbol	Parameter	Value	Unit	
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V	
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧	
lin. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA	
PD	Power Dissipation, per Package†	500	mW	
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C	
TL	Lead Temperature (8-Second Soldering)	260	°C	

\*Maximum Ratings are those values beyond which damage to the device may occur †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C



### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS) OCTAL COUNTER



L SUFFIX CERAMIC PACKAGE PLASTIC PACKAGE **CASE 620** 

**CASE 648** 

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

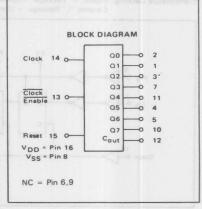
### FUNCTIONAL TRUTH TABLE

(Positive Logic)

CLOCK	CLOCK ENABLE	RESET	OUTPUT - n			
0	×	0	n			
×	1	0	n			
5	0	0	n+1			
~	×	0	n			
1	~	0	n+1			
×	_	0	n n			
×	×	1	00			

Don't Care

If n< 4 Carry = 1, Otherwise = 0



ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

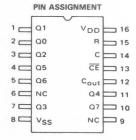
'0" Level	Symbol	V <sub>DD</sub> Vdc	Min	Max	Min	Tvp#	Max			11-
'0" Level				10107	Min	Тур #	Max	Min	gh <sup>®</sup> Max	Unit
	VOL	5.0	11-	0.05	-	0	0.05	EL BET-DO	0.05	Vdd
	6.0	10	-	0.05	-	0	0.05	m #1) =	0.05	
4	02	15		0.05	-	0	0.05	- (0.75	0.05	
'1" Level	VOH	5.0	4.95	_	4.95	5.0	JU THINK	4.95	JETTLAL	Vdd
	· On		9.95	-	Annual Control Special Control				1 прідзятс	144
		15	14.95	_	14.95	15	-160	14.95	S of And	
"0" Level	VII					40 BIA 6	J-2-1980V	Tall No.	agr PLA	Vdd
	DE 1	5.0	-	1.5	-	2.25	1.5	90.01	1.5	
2 - 1	ar I	10	-	3.0	-	4.50	3.0	F 9.01 = 7	3.0	
		15	-	4.0	-	6.75	4.0	mil-usia	4.0	14
"1" Level	VIH	10.03						510	of spol	
	na		3.5	-	3.5	2.75	10-138N	3.5	8914401	Vdc
	01			_	10000	The second second	O Little		191 <del>- 1</del> 1 151	
-	ei -	15	11.0	-	The second second second	8.25	13-19:00	11.0	eni pica	
levice)	lou	50 (6)						mill yels	neamin.	mAd
Sept. Checkler	·On	5.0	-3.0	_	-2.4	-4.2	- 640	-1.7	Barutael.	
	0.0		-0.64	_	-0.51	-0.88	304 Pes	-0.36	H97-HJ9	
	or i	10	-1.6	-	-1.3	-2.25	O Gener	-0.9	H이글CIS	
	ar I	15	-4.2	-	-3.4	-8.8	12.170	-2.4	ggif _pi_rv	
ink	loi	5.0	0.64	_	0.51	0.88	_	0.36	HARD THOU	mAd
	OL			_			_	1	3 mjano-	
- 11	oa d	15	4.2	-	3.4	8.8	215+3	2.4	The Lange	
P Device)	lou					100	Section 1	100000	91 15,14	mAd
ource	·OH	5.0	-2.5	1	-21	-4.2	1001	-1.7	01 - N. I.	
085	0.8			_	1		_	2000	William S.	10
007	01 - 1		10	-			L		_	
76	81	15		-			-		-	
ink	lou	5.0	-	_	-	-	_	-	Support or	mAd
112	GI			_	-0.00	100000000000000000000000000000000000000			_	
	Br	15	3.6	_	3.0	8.8	-	2.4	_	
003 1	0.01in	15	-	+01	-	±0 00001		_ 1970	+10	μAde
e)			-		-	-		1 -		μAd
100			-		-					pF
760	O.B.	man				5.0	7.5	92817 4	women:	a a R
ce)	Ipp	5.0	-	5.0	-	0.005	5.0	-	150	μAd
012		10		10		0.010	10	- 1	300	100
mile I	0.8	15	-	20	-	0.015	20	1.00.05 1000	600	
levice)	IDD	5.0	-	20	-	0.005	20	-	150	μAd
-		10		40	-	0.010	40		300	
389	50.00	15	-	80	-	0.015	80		600	
	IT	5.0		ET TES	IT = (0	.28 µA/kHz	) f + Ipp			μAd
- 61		10								
its, all	01	15								010
	evice)	"1" Level VIH  evice) IOH  purce IOH  ink IOL  P Device) IOH  ource Inn  in Inn  Cin  e) Ipp  evice) IDD	"0" Level VIL 5.0 10 15 15 15 10 10 15 15 15 15 15 15 15 15 15 15 15 15 15	"0" Level VIL 5.0 - 10 - 15 - 15 - 14.95  "1" Level VIH 5.0 3.5 - 10 7.0 15 11.0  evice) IOH 5.0 -3.0 5.0 -0.64 10 -1.6 15 -4.2  ink IOL 5.0 0.64 10 1.6 15 4.2  P Device) IOH 5.0 -2.5 5.0 -0.52 10 -1.3 15 -3.6  ink IOL 5.0 0.52 10 13 3.6  ink IOL 5.0 0.52 10 10 1.3  ib 3.6  III 15	"0" Level VIL 5.0 - 1.5   10 - 3.0   15 - 4.0   "1" Level VIH 5.0 3.5 - 10 7.0 - 15 11.0 - 15 11.0 - 15 11.0 - 15 11.0 - 15 11.0 - 15 11.0 - 15 11.0 - 16 15 15 1.0 - 16 15 15 1.0 - 16 15 15 1.0 - 16 15 15 1.0 - 16 15 15 1.0 - 16 15 15 1.0 - 16 15 15 1.0 16 15 15 1.0 - 16 15 15 1.0 - 16 15 15 1.0 - 16 15 15 1.0 - 16 15 15 1.0 - 16 15 15 1.0 15 15 15 1.0 15 15 15 15 15 15 15 15 15 15 15 15 15	15	15	15	**************************************	***Time

 $<sup>^*</sup>T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_{T}$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.00125

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$  Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



NC = No Connection

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

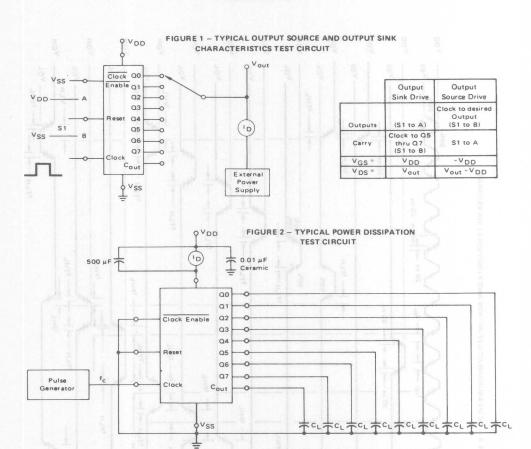
<sup>†</sup>To calculate total supply current at loads other than 50 pF:

Charac	teristic			oild	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise and Fall Time	8 1		60.0		tTLH-	yV 1	ovaJ "6"		eganioV II	ns
tTLH, tTHL = (1.5 ns/pF) CL +	25 ns			-	tTHL	5.0		100	200	-27
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub>					IIIL	10	-	50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub>	+ 9.5 ns			60 A		15	sun t	40	80	
Propagation Delay Time	10.0	28.0		20.0	tPLH.				gV to U	ns
Reset to Decode Output				- ee b	tPHL					1
tplH tpHL = (1.7 ns/pF) CL					THE	5.0	1 -4	500	1000	Tuggi
tpLH tpHL = (0.66 ns/pF) CL						10		230	460	1/2
tpLH tpHL = (0.5 ns/pF) CL						15	112	175	350	tor.
Propagation Delay Time	30 00		IL A			1		067 0 1	1000	ns
Clock to Cout				Secretary Services	tPLH,	100	100			1
tplH tpHL = (1.7 ns/pF) CL	315 ns			8.5	THE	5.0		400	800	5/3
tp_H, tpHL = (0.66 ns/pF) CL				7.0		10	100	175	350	W
tpLH, tpHL = (0.5 ns/pF) CL				0-13		15		125	250	3/3
Propagation Delay Time	199.00	10.7.5			tPLH.	100	beorus/	JAI Tress	all eviral	ns
Clock to Decode Output				0.0	tPHL	100	Souther	1454	rac Hu	100
tplH tpHL = (1.7 ns/pF) CL				0.84	PHL	5.0	-	275	1000	W.
tp_H, tpHL = (0.66 ns/pF) CL				- 8 1		10	_	125	460	Wit .
tp_H, tpHL = 0.5 ns/pF) CL +				4.2		15	_	95	350	3/3
Turn-Off Delay Time	88.0	18.0		88.0	tPLH	01	Sont	(58	/ b B = 1	ns
Reset to Cout				5.4	0	1		(38)	V 80	191
tpLH = (1.7 ns/pF) CL + 315 n				5.0		5.0	_	400	800	121
tpl H = (0.66 ns/pF) CL + 142						10		175	350	1
tpLH = (0.5 ns/pF) CL + 100 m				a c		15	a Tuesday	125	250	100
Clock Pulse Width	98.0-	55.0-		52.0	twH	5.0	250	125	73 ± 4 L	ns
				8.1	01	10	100	50	7 Z = 1	VI.
				8.6		15	75	35	8.5	LVS.
Clock Frequency	88.0	88.0		0.80	fcl	5.0	- 1002	5.0	2.0	MH
90				2.5	Of .	10	-	12	5.0	101
				1 00		15	_	16	6.7	lva.
Reset Pulse Width	10000 01		104	1	tWH	5.0	500	250	0.00	ns
				-	1 21	10	250	125	1 Tal.	Juga
				1		15	190	95	-	Teller
Reset Removal Time	2.0			1	trem	5.0	750	375	-	ns
				parami		10	275	135		
						15	210	105	1011U.J.	STATE OF
Clock Input Rise and Fall Time	819.0		05		TLH, THL	5.0				-
				-		10	(bayes)	No Limit		position C
	800.6		96			15		The state of	Lancis d'un Cl	001
Clock Enable Setup Time					tsu	5.0	350	175	-	ns
						10	150	75	wo viens	1676
	Total Control of	OF - 1			1 00	15	115	52	-	401
Clock Enable Removal Time					trem	5.0	420	260	Spottoe 9	ns
						10	200	100	TaTe :	1

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

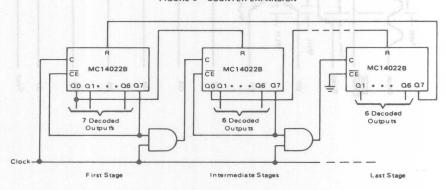
### MC14022B

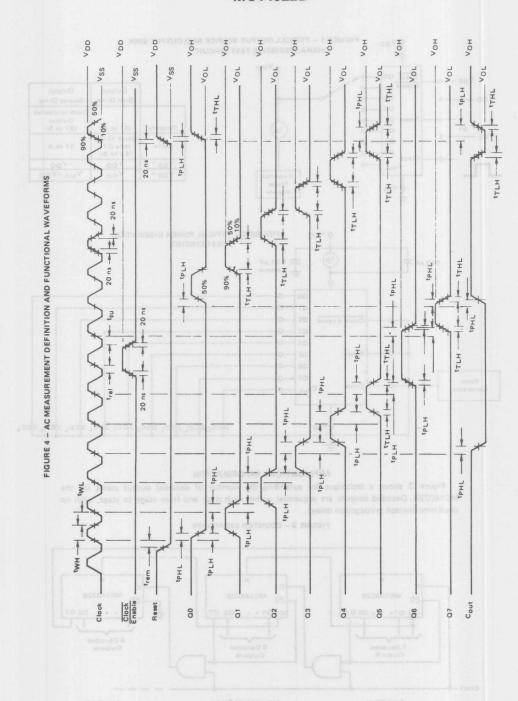


#### **APPLICATIONS INFORMATION**

Figure 3 shows a technique for extending the number of decoded output states for the MC14022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

#### FIGURE 3 - COUNTER EXPANSION







# MC14023B MC14023UB



# TRIPLE 3-INPUT "NAND" GATE

The MC14023B and MC14023UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14023B only)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14023B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4023B and CD4023UB.

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	- 0.5 to + 18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin-lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Package: -12mW/°C from 65°C to 85°C
Ceramic "L" Package: -12mW/°C from 00°C to 125°C

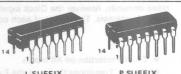
See the MC14001B data sheet for complete characteristics of the B-Series device.

See the MC14001UB data sheet for complete characteristics for the UB device.

# **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NAND" GATE



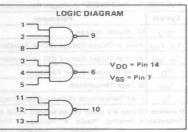
CERAMIC PACKAGE

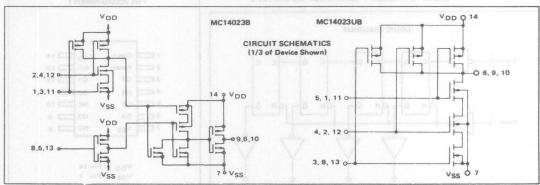
P SUFFIX PLASTIC PACKAGE CASE 646

ORDERING INFORMATION

A Series: -55°C to +125°C
MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP or UBCP (Plastic Package) MC14XXXBCL or UBCL (Ceramic Package)





This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance cir-

cuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub>  $\leq$  (V<sub>in</sub> or V<sub>out</sub>)  $\leq$  V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



# MC14024B



# **SEVEN STAGE RIPPLE COUNTER**

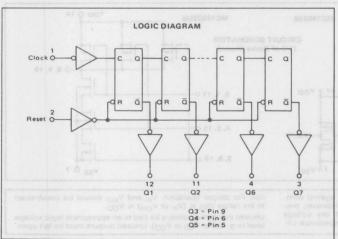
The MC14024B is a seven stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity, however the Clock input has increased noise immunity due to Hysteresis. The output of each counter stage is buffered.

- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4024B

MAXIMUM RATINGS\* (Voltages Referenced to Ves)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C



# **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

SEVEN STAGE RIPPLE COUNTER





L SUFFIX
CERAMIC PACKAGE
CASE 632

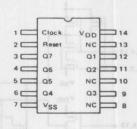
P SUFFIX
PLASTIC PACKAGE
CASE 646

## ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



V<sub>DD</sub> = Pin 14 V<sub>SS</sub> = Pin 7

NC = No Connection

# MC14024B

EI	ECTRICAL	CHARACTERIS	TICS (Voltages	Referenced to Vool

Called Till Service of Called	44.00	VDD	Tlo	w	-	25°C		Thi	gh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	Righte 8.1	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	01	10	-	0.05	-	0	0.05	0.75-000	0.05	tervi.
08 08 -	27	15	_	0.05	-	0	0.05	glan-88 0	0.05	urd
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	Illia - norte	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	- OH	10	9.95		9.95	10	-	9.95	10-rub	45)
Vin = 0 of VDD	0.8	15	14.95	_	14.95	15	(545-6)	14.95	uni Turk	
Input Voltage "0" Level	VIL					an 519 4	a D. Filturiae	86.61 = 1	saint as rec	Vdc
(VO 4.5 or 0.5 Vdc)	81	5.0		1.5		2.25	1.5	N 21.122 W 1	1.5	1
(VO 9.0 or 1.0 Vdc)		10		3.0	-	4.50	3.0	-	3.0	10
(V <sub>O</sub> 13.5 or 1.5 Vdc)	0.2	15		4.0	_	6.75	4.0	1000	4.0	
"1" Level	VIH	10		4.0	1	50 TOE +	13 Phalas	38.01 = 1	H187 to 141	_
(VO = 0.5 or 4.5 Vdc)	HIV	5.0	3.5		3.5	2.75	10JPet	3.5	MEE - M. 197	Vdc
(VO 1.0 or 9.0 Vdc)		10	7.0	-	7.0	5.50		7.0	willer: 70	THE STATE OF
(VO = 1.5 or 13.5 Vdc)	0.8	15	11.0	-	11.0	8.25	100 Pep	11.0	HS1 41 10	
		15	11.0		11.0	0.23	O Charles	11.0	Mar H a	mAdo
Output Drive Current (AL Device)	ІОН	5.0	-3.0		-2.4	-4.2	12 1910	-1.7	HIRLE TRIN	MAGG
(VOH 2.5 Vdc) Source	0.0	5.0	-0.64		-0.51	-4.2	-	-0.36	Philip of u	(Rock)
(*OH 4.0 voc)	- 08	5.0	-1.6	-	-1.3	-2.25	_	-0.36	_	
(AOH - 3.2 AGC)	80	10		-	-3.4	-2.25		-0.9		1
140H 13.3 AGC1		15	-4.2	-	-	-		-		1
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	BENAN WITH	mAdd
(Voc = 0.5 Vdc)	21	10	1.6	-	1.3	2.25	-	0.9	-	1
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2		3.4	8.8		2.4		
Output Drive Current (CL/CP Device)	10Н							9/35		mAdd
(VOH = 2.5 Vdc) Source	90	5.0	-2.5	-	-2.1	-4.2	-	-1.7		1
(VOH = 4.6 Vdc)	81	5.0	-0.52		-0.44	-0.88		-0.36		
(V <sub>OH</sub> = 9.5 Vdc)	0.0	10	-1.3	-	-1.1	-2.25	-mm	-0.9	not Platon	Clock
(V <sub>OH</sub> = 13.5 Vdc) —	10	15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36		mAdd
(VOL = 0.5 Vdc)	-0.6	10	1.3	-	1.1	2.25	-	0.9	0017 10 8	9 Hight
(VOL = 1.5 Vdc)	01	15	3.6	-	3.0	8.8	_	2.4		
Input'Current (AL Device)	lin	15	-	± 0.1	-	± 0.00001	±0.1	-	± 1.0	μAdd
Input Current (CL/CP Device)	lin	15	-	+03	5785-04 vi	±0.00001	±0.3	of the part of	±1.0	μAdd
Input Capacitance	Cin		-		-	5.0	7.5	-	_	pF
(V <sub>in</sub> - 0)	Cin				21 Jug 343	3.0	7.5	ed of lish of	legT 5all	DEC 150
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdd
(Per Package)	00	10	-	10	-	0.010	10	-	300	
		15	-	20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	1	0.005	20	-	150	μAdd
(Per Package)	.00	10	-	40		0.010	40	_	300	1 4700
		15		80	-	0.015	80	_	600	
Total Supply Current**†	İT	5.0	1	00	110	31 μA/kHz			000	μAdo
(Dynamic plus Quiescent,	.1	10				.31 μΑ/kHz .60 μΑ/kHz				μAdd
Per Package)		15	1			89 μA/kHz				
(C <sub>1</sub> = 50 pF on all outputs, all		13			1 - (0.	DO HAIRIIZ	, , , , , , ,			1
buffers switching)			BUSKY							

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.001.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS\* (C1 = 50 pF, TA = 25°C)

Characteristic			Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	3 30000	75/1/23	tTLH.	MIDAYS		2010/183	SETERIO	ns
tTLH, tTHL = (1.5 ns/pF) CL + 25 ns			tTHL	5.0	(4×8.1)	100	200	V mate
tTLH, tTHL = (0.75 ns/pF) CL + 12.5 ns			07	10	-	50	100	" not
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns			- 81	15	-	40	80	
Propagation Delay Time	4 85		tPLH,	ROY	Teve	28"		ns
Clock to Q1			tPHL				COV NA D	Vin F
tpLH, tpHL = (1.7 ns/pF) CL + 295 ns			AS TA'S	5.0	-	380	600	
tpLH tpHL = (0.66 ns/pF) CL + 117 ns				10	hn=1 "0	150	230	HOV THE
tPLH, tPHL = (0.5 ns/pF) CL + 85 ns			0.2	15	-	110	175	1630
Clock to Q7			100			tobly	0.1.10.01	03/1
tpLH, tpHL = (1,7 ns/pF) CL + 915 ns			- 31	5.0	-	1000	2000	(V)
tpLH, tpHL = (0.66 ns/pF) CL + 367 ns				10	(199 <del>4)</del> 5 "1	400	750	
tpLH, tpHL = (0.5 ns/pF) CL + 275 ns			88 08	15	-	300	565	POVE
Reset to Qn			0.7 01			EphV	0.0 10.0	030
tPLH, tPHL = (1.7 ns/pF) CL + 415 ns			E-11 81	5.0	-	500	800	I OV
tpLH, tpHL = (0.66 ns/pF) CL + 217 ns				10	- (40	250	400	ve tum
tpLH, tpHL = (0.5 ns/pF) CL + 155 ns	2.4		50 -30	15	-	180	300	Lugar
Clock Pulse Width			twh	5.0	500	200	IST B.B.	ns
			81 01	10	165	60	Caree	HOW
8.8-	108-	le su	S A	15	125	40	N V T.EL	LIGVI
Reset Pulse Width			tWH	5.0	600	375	1107 40	ns
			87 81	10	350	200	0.5740	FROVI
24 24	1 02		15 4.9	15	260	150	SOUTE D	L.SVI
Reset Removal Time			trem	5.0	625	250		ns
			10-10-	10	190	75	130 - 8 5	Land Vi
			2 0 To 0 8	15	145	50	4.6.7.del	1.59
Clock Input Rise and Fall Times	111-	-	TLH, THL	5.0	-	_	1.0	S
			15 -3.5	10	-	-	8.0	ms
			186 88	15	-	w2 -	200	μѕ
Input Pulse Frequency	1.1		f <sub>cl</sub>	5.0	-	2.5	1.0	MHz
			'CI	10	-	8.0	3.0	H SVS
				15	_	12	4.0	1

\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TRUTH TABLE

CLOCK	RESET	STATE
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
	0	No Change
	1	All Outputs Low
_	0	Advance One Count
	int termina pass	All Outputs Low

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

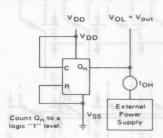


FIGURE 2 - TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

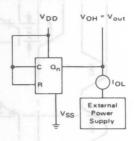
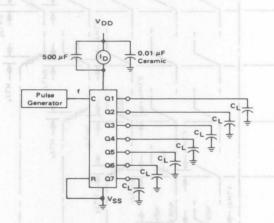
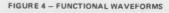
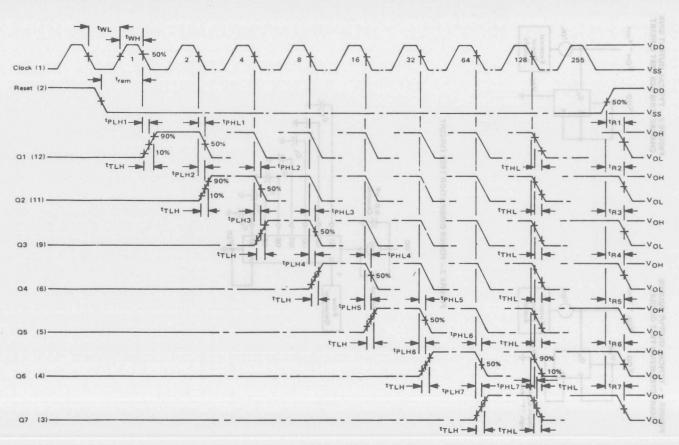


FIGURE 3 - POWER DISSIPATION TEST CIRCUIT







Input tTLH and tTHL = 20 ns



# MC14025B MC14025UB

# TRIPLE 3-INPUT "NOR" GATE

The MC14025B and MC14025UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14025B only)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14025B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4025B and CD4025UB

# MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	MORAM Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

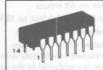
See the MC14001B data sheet for complete characteristics of the B-Series device.

See the MC14001UB data sheet for complete characteristics for the non-B device.

# **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NOR" GATE





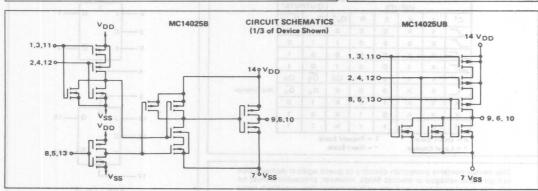
CERAMIC PACKAGE CASE 632 P SUFFIX PLASTIC PACKAGE CASE 646

ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP or UBCP (Plastic Package) MC14XXXBCL or UBCL (Ceramic Package)

# LOGIC DIAGRAM 1 2 8 3 4 4 0 6 VDD = Pin 14 VSS = Pin 7



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained

to the range  $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open



MC14027B

# **DUAL J-K FLIP-FLOP**

The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design —
   Logic state is retained indefinitely with clock level either high or
   low; information is transferred to the output only on the positive going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027B

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-05 to V <sub>DD</sub> +05	V
lin-lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TE	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur †Temperature Derating: Plastic "P" Package: -12mW"C from 65°C to 85°C Ceramic "L" Package: -12mW"C from 100°C to 125°C

		INPL	ITC	OUTE	PUTS*			
	-				1		-	
CT	J	K	S	R	Qn \$	Qn+1	Q <sub>n+1</sub>	
5	1	Х	0	0	0	1	0	to Datt
	х	0	0	0	1	1	0	
	0	X	0	0	0	0	1	
7	×	1	0	0	1	0	1	wWga1
_	1	1	0	0	Qo	Qo	Qo	No.
7	×	×	0	0	×	an	an	No Change
X	×	X	1	0	X	1	0	1
X	×	х	0	1	×	0	1	in the
X	×	×	1	1	×	1	1	The state of the s

† = Level Change \* = Next State

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$  Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

# CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

**DUAL J-K FLIP-FLOP** 



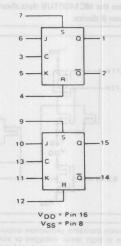
L SUFFIX CERAMIC PACKAGE CASE 620 PSUFFIX
PLASTIC PACKAGE
CASE 648

# ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to Vos)

Matt I walk I support I state	only I	VDD	Tlo	w*		25°C		Thi	gh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	110,611 c.	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	or I	10	-	0.05	-	0	0.05	10,00 047	0.05	1187145
115 016	31	15		0.05	_	0	0.05	leken 88.	0.05	MATT!
"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95	MINE THOSE	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	- OH	10	9.95	_	9.95	10		9.95	0.000	0010
Vin - 0 of VDD	0.8	15	14.95	_	14.95	15	+ 00	14.95	Hell is	101
	VIL	10	14.55		14.00	201 22	19 (10	14.55	19774	Vdc
The state of the s	AIT	5.0		1.5		2.25	1.5	Sub-Billion I	1.5	Vac
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		10	- 1		_		3.0		3.0	165
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	0.8		-	3.0		4.50		Sept. T. (1)	the state of the state of	epi
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15		4.0	-	6.75	4.0		4.0	-
981 81 "1" Level	VIH					70 85		ten 2.00		9
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	45.4	5.0	3.5	-	3.5	2.75	-	3.5	0.00	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)	0.2	10	7.0	-	7.0	5.50	+ 30 (9)	7.0	nation is	o) I
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	0.0	15	11.0	-	11.0	8.25	3100	11.0	La Company	lat.
Output Drive Current (AL Device)	Іон	94 .		Programme and the			5 O (3)	an a m		mAdc
(VOH = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	-1.7		Gursi'i
(V <sub>OH</sub> = 4.6 Vdc)	0.2	5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	- Maritina
(Vou = 9.5 Vdc)	101	10	-1.6	-	-1.3	-2.25	1	-0.9	_	
(VOH = 13.5 Vdc)	. 61	15	-4.2		-3.4	-8.8	_	-2.4	_	F 5-5-51
(VOI = 0.4 Vdc) Sink	lou	5.0	0.64	-	0.51	0.88	_	0.36	_	mAdc
(VOL = 0.5 Vdc)	IOL	10	1.6		1.3	2.25		0.9	_	111700
	37	15	4.2		3.4	8.8		2.4		0
(V <sub>OL</sub> = 1.5 Vdc)	-	15	4.2	-	3.4	8.8	_	2.4	alah We ass	E Joseph
Output Drive Current (CL/CP Device)	ІОН									mAdc
(VOH = 2.5 Vdc) Source	- 37	5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	-	-0.36	Acres of Secretaria	R vrocti
(V <sub>OH</sub> = 9.5 Vdc)	0.8	10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(V <sub>OH</sub> = 13.5 Vdc)	- 01	15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	_	0.44	0.88	-	0.36	ico Pierra	mAdo
(VOL = 0.5 Vdc)	D. I.	10	1.3		1.1	2.25	_	0.9	0.445.2 230	STREET,
(V <sub>OL</sub> = 1.5 Vdc)	- 01	15	3.6	-	3.0	8.8	-	2.4		
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Current (CL/CP Device)	_	15		± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdc
	lin				-					-
Input Capacitance (V <sub>in</sub> = 0)	Cin	1		-	-	5.0	7.5	-	-	pF
Quiescent Current (AL Device)	IDD	5.0	-	1.0	-	0.002	1.0	-	30	μAdc
(Per Package)		10	-	2.0	-	0.004	2.0	-	60	
	200	15		4.0	-	0.006	4.0	-	120	
Quiescent Current (CL/CP Device)	IDD	5.0	-	4.0	-	0.002	4.0	-	30	μAdo
(Per Package)	.00	10		8.0		0.004	8.0		60	, and
(rer rackage)	0.8	15	-	16		0.006	16	risport e	120	bring 10
				10	1		_		120	1
rotal dapply darrent	IT	5.0				.80 μA/kHz				μAdo
(Dynamic plus Quiescent,						.60 μA/kHz				
Per Package) (CL = 50 pF on all outputs, all buffers switching)		15			T = (2	.40 μA/kHz	) ( + IDE	Section to the		TERM SHEET

 $^*T_{low}$  = -55°C for AL Device, -40°C for CL/CP Device.  $T_{high}$  = +125°C for AL Device, +85°C for CL/CP Device.

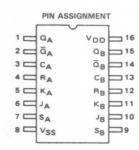
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: IT is in  $\mu A$  (per package),  $C_L$  in pF, V = (VDD-VSS) in volts, f in kHz is input frequency, and k = 0.002.



# MC14027B

SWITCHING CHARACTERISTICS\* (C1 = 50 pF, TA = 25°C)

Characteristic							Symbol	VDD	Min	Typ #	Max	Unit
Output Rise an	d Fall Time	Spaging .	1 09T	6497	234(4)	-	tTLH.	DON'TS		- Informati	e Articol	ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns							†THL	5.0	I the suit	100	200	W suddy
tTLH. THL							GI I	10	_	50	100	West of
	= (0.55 ns/pF							15	-	40	80	
Propagation D		-	70.5	20:11		201	tPLH,	HOV	feve_L	100		ns
Clock to Q.	Q					10	tPHL		P The state of		Diese Vene	- W
	L = (1.7  ns/s)	pF) CL +	90 ns				84 65	5.0	_	175	350	
tplH, tpH	L = (0.66 ns	/pF) C <sub>1</sub> +	42 ns					10	Savata "6"	75	150	PoV Su
tpi H, tpH	L = (0.5  ns/s)	pF) C <sub>1</sub> +	25 ns					15	-	50	100	IVo.
Set to Q, Q									-	1500	U. T. 50 T/	0.40
tPLH, tPH	IL = (1.7  ns/	pF) CL +	90 ns					5.0	-	175	350	- OVI
tPLH, tPH	L = (0.66 ns	/pF) CL +	42 ns					10	19955 TY	75	150	
	L = (0.5 ns/							15	-	50	100	i ovi
Reset to Q.	Q								-	Luis V	0.6 /5 0.1	- 610
tPLH, tPH	$_{1L} = (1.7 \text{ ns})$							5.0	-	350	450	- 0VI
tPLH, tPH	L = (0.66 ns	s/pF) CL -	+ 67 ns					10	Tea	100	200	C top
tPLH. tPH	IL = (0.5 ns/	pF) CL +	50 ns					15	- 190	75	150	4.00.571
Setup Times	ar a		00 n	18.0-		10	t <sub>su</sub>	5.0	140	70	4.57436	ns
						0	01	10	50	25	-b.1-0.0	HOVE
			- 10.00	2.0			4 1 1	15	35	17	- V = V I	1
Hold Times							th	5.0	140	70	Land Target	ns
								10	50	25		10.4
								15	35	17	WTA I	1000
Clock Pulse Wi	dth			ot on the			tWH, tWL	5.0	330	165	-	ns
								10	110	55	say Etc	Luny VI
						1 3		15	75	38	30 V C/L	THE YES
Clock Pulse Fr	equency		2.25	11		1 2	fcl	5.0	_	3.0	1.5	MHz
	20-					1 3	,CI	10	-	9.0	4.5	MOA)
						-		15	-	13	6.5	1910
Clock Pulse Ri	se and Fall Ti	me	98.9	777			tTLH, tTHL	5.0	_	-	15	из
	5.0					1	LII, THE	10	_	_	5.0	367
						1	2	15	_	-	4.0	100
JUPAN DI		1 01	1.0000		-	1		-				
Removal Time	S						trem	5	90	10	UNITED IN	ns
								10	45	5	danatio	402.10
								15	35	3	_ 1	1 m V
Set								met		troved J	a) mems	100000
								5	50	- 30	topus	Par Par
						1		10	25	- 15	_	
Reset								15	20	-10	1 Inni	10000
								10	20	10	(sout)	
Set and Reset	Pulse Width	av.	200.0		2.0		TWH	5.0	250	125	-	ns
	and a second					ā,,		10	100	50	001=3.9	A ALBOYS AND A
								15	70	35	1 2 1 2 1 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1000

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

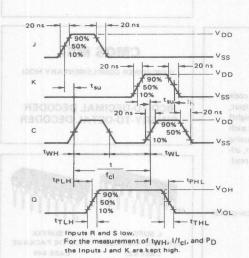
<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Reset

Clock

# FIGURE 1 — DYNAMIC SIGNAL WAVEFORMS (J, K, Clock, and Output)

# FIGURE 2 — DYNAMIC SIGNAL WAVEFORMS (Set, Reset, Clock, and Output)



20 ns 20 ns VDD

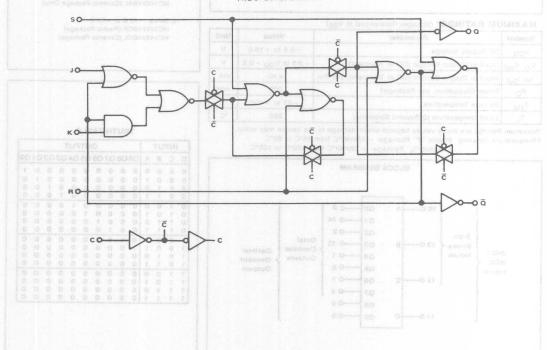
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III HA no stoppo O would be

METUPGO or winned W

## LOGIC DIAGRAM (1/2 of Device Shown)



# MC14028B

# BCD-TO-DECIMAL DECODER BINARY-TO-OCTAL DECODER

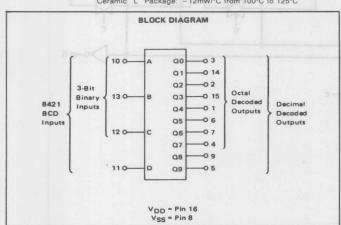
The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Positive Logic Design
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B.

MAXIMUM RATINGS\* (Voltages Referenced to Vos)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

"Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/"C from 65°C to 85°C
Ceramic "L" Package: -12mW/"C from 100°C to 125°C



# **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-DECIMAL DECODER BINARY-TO-OCTAL DECODER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

## ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

# TRUTH TABLE

	INF	TU					0	UT	PU	T			
D	C	В	A	Q9	90	07	Q6	Q5	Q4	Q3	Q2	Q1	QO
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

Non-Page 1 March 1500 Pages	no.V	VDD	Tio	w*		25°C		Thi	gh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	(3) er 2	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	OL	10	- 1	0.05	-	0	0.05	100 mm 255	0.05	an net
VIN - VDD OI O	81	15		0.05	_	0	0.05	late # 58	0.05	an arri
"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95	mater en cit	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	- OH	10	9.95		9.95	10	004.0	9.95	W 1800 1	DEST
Vin - O OI VDD	01	15	14.95		14.95	15	01-51	14.95	S 155/01 N	1.00
nput Voltage "0" Level	VIL		11.00				BL F 10	Tolero et C	3 Date 1	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	11	5.0		1.5	-	2.25	1.5	- 1	1.5	
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10		3.0	PES to stre	4.50	3.0	toril right drug	3.0	mail part
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15		4.0	J 11 - 11	6.75	4.0		4.0	
"1" Level	VIH	13	-	4.0		0.75	and i Or		tied ex us b	
(Vo = 0.5 or 4.5 Vdc)	VIH	5.0	3.5	-	3.5	2.75		3.5		Vdc
(VO = 1.0 or 9.0 Vdc)		10				5.50	_	7.0	_	***
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	7.0		7.0	8.25	_	11.0	_	
		15	11.0		11.0	0.25		11.0		0
Output Drive Current (AL Device)	ЮН		0.0							mAdc
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0-	-3.0	-	-2.4	-4.2	-	-1.7	-	
(V <sub>OH</sub> = 4.6 Vdc)	25(2)	5.0	-0.64	BUR AVANCE	-0.51	-0.88	-	-0.36	-	
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	-	-1.3	2.25	-	-0.9	, -	
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	_	-3.4	-8.8		-2.4		-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.25	-	0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-tr-	3.4	8.8	-	2.4	-	
Output Drive Current (CL/CP Device)	ОН	7		-				73 Acres 15	D'anternation	mAdo
(VOH = 2.5 Vdc) Source		5.0	-2.5	W 100	-2.1	-4.2	-	-1.7	printing	
(VOH = 4.6 Vdc)		5.0	-0.52	_	-0.44	-0.88	-	-0.36	004 : 0	
(VOH = 9.5 Vdc)	18 <sub>A</sub>	10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(VOH = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	L -	-2.4	-	
(VOI = 0.4 Vdc) Sink	loL	5.0	0.52	_	0.44	0.88	_	0.36	-	mAdo
(V <sub>OL</sub> = 0.5 Vdc)	OL.	10	1.3	-	1.1	2.25	_	0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6		3.0	8.8	-	2.4		
Input Current (AL Device)	lin	15	-	± 0.1	<u></u>	±0.00001	±0.1	-	± 1.0	μAdc
Input Current (CL/CP Device)	-	15	1997 1997	± 0.3	,	±0.00001	± 0.3	-	±1.0	μAdc
	lin		-		-			-	11.0	-
Input Capacitance (V <sub>in</sub> = 0)	Cin	-	A MON	-	IX.	5.0	7.5	-	-	pF
Quiescent Current (AL Device)	IDD	5.0	1134	5.0	-	0.005	5.0	-	150	μAdc
(Per Package)		10	100	10	-	0.010	10	eal <u>0</u> 5m	300	
		15	-	20	-	0.015	20		600	
Quiescent Current (CL/CP Device)	IDD	5.0	100	20	-	0.005	20	_	150	μAdo
(Per Package)	00	10	-	40	-	0.010	40	_ 1	300	
		15	-	80	14.14	0.015	80	_	600	
Total Supply Current**†	IT	5.0		-	IT = 10	3 MA/KHZ			000	μAdc
(Dynamic plus Quiescent,		10	100			).6 µA/kHz				MAGE
Per Package)		15				).9 µA/kHz				
(C <sub>1</sub> = 50 pF on all outputs, all					1 10		UL			
buffers switching)			1							

 $<sup>^{*}</sup>T_{low} = -55^{\circ}C$  for AL Device.  $-40^{\circ}C$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

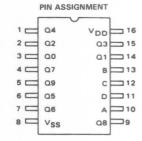
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



Thigh = + 125°C for AL Device. +85°C for CL/CP Device.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C

# MC14028B

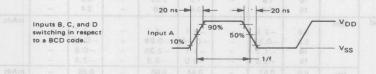
SWITCHING	CHARACTERISTICS*	(C1 = 50 pF, TA = 25°C)
-----------	------------------	-------------------------

Characteristic		terut	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	- one	nots!	tTLH.	166my2		gilm'red	Charactic	ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns			tTHL	5.0	Tores.I	100	200	3/ 100
$t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$			- 1 01	10	-	50	100	- mil
$t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$			+ 21	15	-	40	80	
Propagation Delay Time	4,05	- 1	tPLH,	HOV	L. Bread	Trans.		ns
tpLH, tpHL = (1.7 ns/pF) CL + 215 ns			TPHL	5.0	1'-	300	600	= 400
tpLH, tpHL = (0.66 ns/pF) CL + 97 ns			de st 1 81	10	-	130	260	100
tpLH tpHL = (0.5 ns/pF) CL + 65 ns				15	10/01/11/0	90	180	Link to

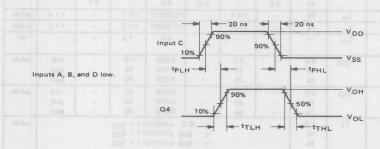
\*The formulas given are for the typical characteristics only at 25°C.

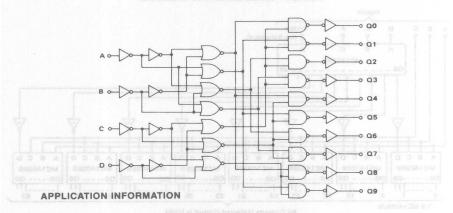
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## FIGURE 1 - DYNAMIC SIGNAL WAVEFORMS



All outputs connected to respective C<sub>L</sub> loads. f in respect to a system clock.

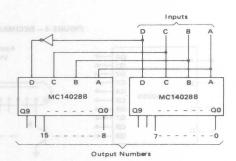




Expanded decoding can be performed by using the MC14028B and other CMOS Integrated Circuits. The circuit in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028B circuits and two MC14069UB inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

FIGURE 2 – CODE CONVERSION CIRCUIT
AND TRUTH TABLE



																					E AND				D
																				Hexad	ecimal		Decin	nal	
1	NPI	UTS	5					(	סטו	TPL	יו דנ	NUN	иве	RS						4-Bit Binary	4-Bit Gray	xcess-3	xcess-3 Gray	Aiken	4221
D	С	В	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4 · · · ·	40	Ex	Exc	A	A
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	1 :
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	Γ
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			1:
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6	4	3	1		1
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5			Γ
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			1
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	10	12	7	9		1
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5	1
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	Γ
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	1
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	1

# MC14028B

FIGURE 3 - SIX-BIT BINARY 1-OF-64 DECODER

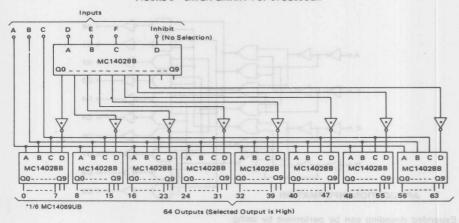
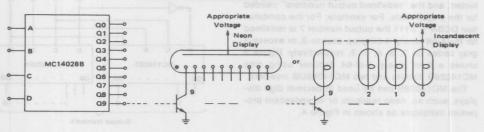


FIGURE 4 - DECIMAL DIGIT DISPLAY APPLICATION







# MC14029B

# **CMOS MSI**

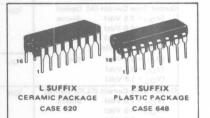
(LOW-POWER COMPLEMENTARY MOS)

BINARY/DECADE UP/DOWN COUNTER

# BINARY/DECADE UP/DOWN COUNTER

The MC14029B Binary/Decade up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide toggle flip-flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Diode Proection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- · Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin for Pin Replacment for CD4029B



# ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

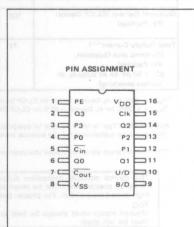
Symbol	Parameter 810.5	Value Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
In- lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

# TRUTH TABLE

Carry In	Up/Down	Preset Enable	Action
olu <b>1</b> baspril	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
×	X	1	Preset

X = Don't Care



ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tic	w*		25°C		Thi	igh "	1
Characteristic	Symbol	Vdc	Min	Мах	Min	Тур#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	manage g	10		0.05		0	0.05	-	0.05	-
		15	-	0.05	-	0	0.05	- 1	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	_	4.95	_	Vdd
Vin = 0 or VDD	0	10	9.95	_	9.95	10		9.95	_	
BOM YEATHSMELISHED REWORKS	0 1	15	14.95	-	14.95	15	-	14.95	_	
nput Voltage "0" Level	VIL		65.2	TERL KEN	1.001557	WINDLE DA	a bard	VCAN	33	Vdd
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	10	5.0	1753	1.5	C. R. C. L. D. C.	2.25	1.5	-	1.5	1
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	1.1	10	1115-111	3.0	a menina	4.50	3.0	oneos:	3.0	
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	111	15	1 -1	4.0	_	6.75	4.0	- 11	4.0	
"1" Level	VIH			1.0		0.70				
(VO = 0.5 or 4.5 Vdc)	- 111	5.0	3.5	STREETON T	3.5	2.75	D 107 . 216	3.5	algnik, a	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)	1.1	10	7.0	or strive	7.0	5.50	TOTAL B.	7.0	dz ostli-o	***
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	meened	15	11.0	o visniš	11.0	8.25	PRO 1953	11.0	ะหม่เรื่อด	10
		13	11.0		11.0	0.25		11.0		
Output Drive Current (AL Device)	ІОН	5.0	-3.0	ers A man	-2.4	-4.2		-1.7		mAd
(V <sub>OH</sub> = 2.5 Vdc) Source				CONTROL TO	10-00-01	Andrew Street,	2013/1	A STATE OF THE PARTY OF	maren o	255
(V <sub>OH</sub> = 4.6 Vdc)	Sec.	5.0	-0.64	aummi.	-0.51 -1.3	-0.88 -2.25	tolfisqus	-0.36	svoT-lose	100
(V <sub>OH</sub> = 9.5 Vdc)	翻一十十	10	-1.6	est test by	And in which the first on a	A PART OF THE PART	ben Gu	-0.9	ru ords ži	100
(V <sub>OH</sub> = 13.5 Vdc)	827	15	-4.2	-	-3.4	-8.8	_	-2.4	-	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	district to	mAd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.25	62 STA 20	0.9	Binds P.	0
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	id tijk ni	2.4		13.
Output Drive Current (CL/CP Device)	Іон	1111111111			Sp.K-40	DI SOA IV	a phys	T. RELEASE	Aldding	mAd
(VOH = 2.5 Vdc) Source	Mad.	5.0	-2.5	-	-2.1	-4.2	il attoine	-1.7	ing and	0
(VOH = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(VOH = 9.5 Vdc)	1 1	10	-1.3	312825 (10	-1.1	-2.25	1450[] 110	-0.9	14.00004	100
(VOH = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	340E	-2.4	mio2	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	in Serve	0.36	rform) A	mAd
(V <sub>OL</sub> = 0.5 Vdc)	0.	10	1.3	in Hose	1.1	2.25	-	0.9	Catholic	
(VOL = 1.5 Vdc)		15	3.6	in abe or	3.0	8.8	Black Riv	2.4	HILLIAND LA	
nput Current (AL Device)	lin	15	- C	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAd
nput Current (CL/CP Device)	lin	15	-	± 0.3	- 0	±0.00001	± 0.3	PROPERTY.	±1.0	μAd
			-					-		-
nput Capacitance (V <sub>in</sub> = 0)	Cin		-	-	-	5.0	7.5	-		pF
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	- 1	150	μAd
(Per Package)		10	-	10	-	0.010	10	-	300	
	MACONIMIST OF THE PARTY OF THE	15	-	20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	_	20	(82V D	0.005	20	5 500	150	μAd
(Per Package)		10	+ intellig	40	-	0.010	40	-	300	- LOND!
		15	-	80	-	0.015	80	-	600	
Total Supply Current**†	IT	5.0			1== 10	.58 µA/kHz		1175		μAd
(Dynamic plus Quiescent,		10	V- only			1.2 µA/kHz)		Her hert		μΑσ
Per Package)		15	07.4			1.7 μA/kHz)				
(C <sub>1</sub> = 50 pF on all outputs, all	1 1		-		11-1					199
buffers switching)	1 3 4		0.03							1 0

 $<sup>^{\</sup>circ}$ T<sub>low</sub> =  $-55^{\circ}$ C for AL Device,  $-40^{\circ}$ C for CL/CP Device. T<sub>high</sub> =  $+125^{\circ}$ C for AL Device,  $+85^{\circ}$ C for CL/CP Device.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

<sup>†</sup>To calculate total supply current at loads other than 50 pF  $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.001.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

# SWITCHING CHARACTERISTICS\* (C<sub>I</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH.					ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	THL	5.0	-	100	200	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns	THE	10		50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	34	15		40	80	
				-		
Propagation Delay Time	tPLH,			1		ns
Clk to Q	tPHL	5.0	75	200	400	
tpLH, tpHL - (1.7 ns/pF) CL + 230 ns	35	10		100	200	
tpLH, tpHL (0.66 ns/pF) CL + 97 ns	05	15		90	180	
tpLH, tpHL - (0.5 ns/pF) CL + 75 ns	19	15		90	160	
Clk to Cout	tPLH.					ns
tp_H, tpHL = (1.7 ns/pF) C <sub>L</sub> + 230 ns tp_H, tpHI = (0.66 ns/pF) C <sub>I</sub> + 97 ns	tPHL	5.0	-	250	500	
		10	-	130	260	
tpLH, tpHL (0.5 ns/pF) CL + 75 ns		15	-	85	190	
Cin to Cout	tPLH.				0.5.5	ns
tpLH, tpHL (1.7 ns/pF) CL + 95 ns	tPHL .	5.0	-	175	360	
tpLH, tpHL (0.66 ns/pF) CL + 47 ns		10	-	50	120	
tpLH, tpHL = (0.5 ns/pF) CL + 35 ns	and Hill	15		50	100	
PE to Q	tPLH.	and a				ns
tPLH, tPHL = (1.7 ns/pF) CL + 230 ns	10111	5.0	-	235	470	
tpLH, tpHL = (0.66 ns/pF) CL + 97 ns		10	-	100	200	
tplH, tpHL = (0.5 ns/pF) CL + 75 ns		15	-	80	160	
PE to Cout	tPLH.					ns
tpLH, tpHL - (1.7 ns/pF) CL + 465 ns		5.0	52552	320	640	
tpLH, tpHL = (0.66 ns/pF) CL + 192 ns		10		145	290	
tpLH, tpHL (0.5 ns/pF) CL + 125 ns		15	-	105	210	
Clock Pulse Width	tW(cl)	5.0	180	90	_	ns
30000 7 3000 77 3000	.AA (C1)	10	80	40	_	
		15	60	30	_	
Clock Pulse Frequency	-	5.0	_	4.0	2.0	MHz
Jock Pulse Frequency	fcl	10	enimier surv	8.0	4.0	IVIPIZ
	- 0 - 0	15	sulq/1	10	5.0	
			120, 1077,016	-	-	
Preset Removal Time	trem	5.0	160	80	-	ns
The Preset Signal must be low prior to a positive-going transition of the clock.		10	80	40		
transition of the clock.		15	60	30	_	
Clock Rise and Fall Time	t <sub>r(cl)</sub>	5.0	-	-	15	μς
	tf(cl)	10		-	5	
		15	-	-	4	
Carry In Setup Time	t <sub>su</sub>	5.0	150	75		ns
中 中 中 中 中	'su	10	60	30		
	June 1, 17 17 P.	15	40	20	_	
In/Down Satura Time	w			+		
Up/Down Setup Time		5.0	340 140	170	- 1	ns
				70	-	
		15	100	50		
Binary/Decade Setup Time		5.0	320	160	-	ns
		10	140	70	-	
	100-1-	15	100	50	-	
Preset Enable Pulse Width	210/	5.0	130	65	_	ns
reset chapte i dise Midth	, tM	10	70	35	-	115
	and the same of	15	50	25		
		10	30	25	-	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

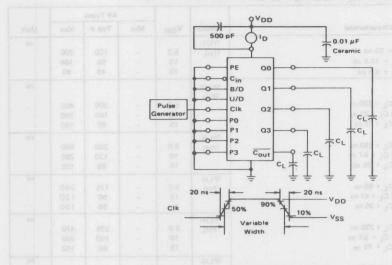
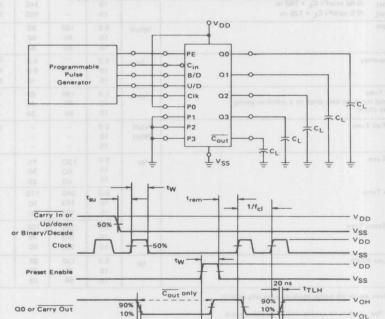


FIGURE 2 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



6

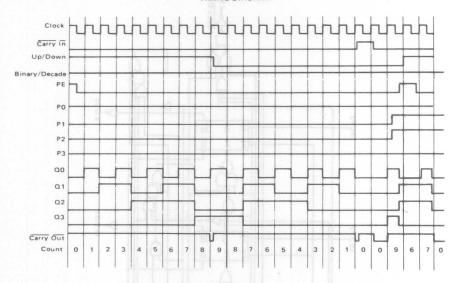
tPHL-

tTHL-

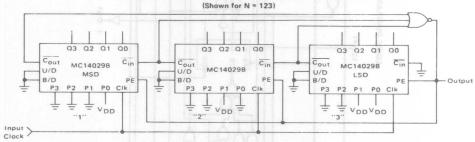
-tPLH

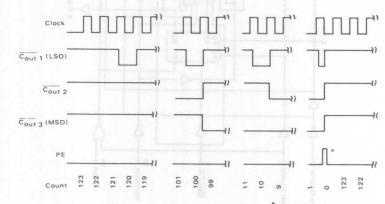
# MC14029B

## TIMING DIAGRAM



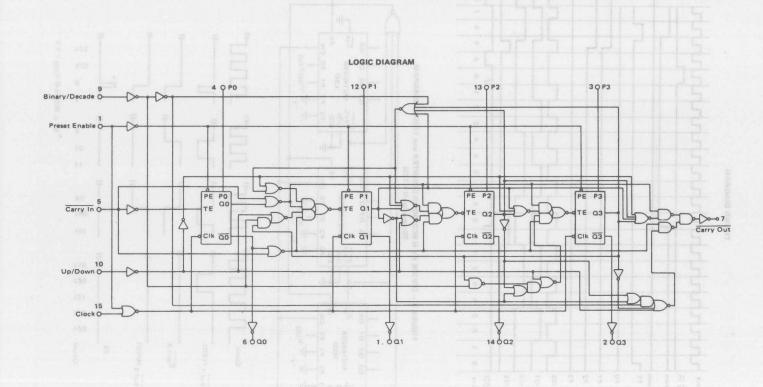
# FIGURE 3 — DIVIDE BY N BCD DOWN COUNTER and TIMING DIAGRAM





 $^*$  t<sub>W</sub>  $\cong$  900 ns @  $V_{DD}$  = 5 V

6-98



# MC14032B MC14038B

# **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

# TRIPLE SERIAL ADDERS

Positive Logic - MC14032B Negative Logic - MC14038B

LSUFFIX CERAMIC PACKAGE CASE 620

PSUFFIX PLASTIC PACKAGE

CASE 648

# ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

# MOTOROLA

# TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers

- Buffered Outputs
- Single-Phase Clocking
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- · Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B.

# MAXIMUM RATINGS\* (Voltages Referenced to VSS)

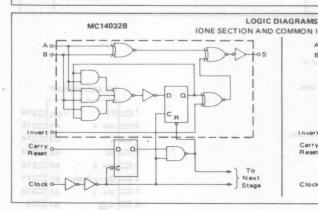
Symbol	Parameter 88.9	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In-lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	-65 to +150	°C
Tı	Lead Temperature (8-Second Soldering)	260	°C

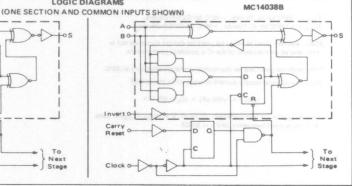
\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\text{in}}$  and  $V_{\text{out}}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

#### BLOCK DIAGRAM A1 10 o B1 11 0-Adder 1 Invert 1 70-A2 13 0-B2 12 0-Adder 2 -04 S2 Invert 2 5 o-VDD = Pin 16 VSS = Pin 8 A3 15 0-B3 14 0-Adder 3 Invert 3 2 0-Clock 3 0-Carry Reset 6 0-





r	6	
r.	0 II	

1255 2010		VDD	Tio	w*		25°C		Thi	gh *	1
Characteristic	Symbol	Vdc	Min	Max	Min	Typ#	Max	Min	Max	Uni
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05		0.05	Vde
Vin VDD or 0	0.	10	-	0.05	-	0	0.05		0.05	
55		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	_	4.95		Vde
Vin = 0 or VDD	· On	10	9.95	_ 4	9.95	10	18 374	9.95	_	1
		15	14.95	uset-male	14.95	15	04/4084	14.95	LECHAL CO	-
nput Voltage "0" Level	VIL		CONTROL SI	T mate	s senti	the or our	F05700 0	Ivini to	na verke	Vd
(VO = 4.5 or 0.5 Vdc)		5.0	S SCHOOL	1.5	sel-noi	2.25	1.5	on it	1.5	1
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	100	10		3.0	- aut 10	4.50	3.0	_	3.0	- Day
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	1	4.0	-	6.75	4.0	amob as	4.0	no
"1" Level	VIH									
(VO = 0.5 or 4.5 Vdc)	- 111	5.0	3.5	Bila boi	3.5	2.75	87571 81	3.5	021000 - 6	Vdo
(VO = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50	_	7.0	pudicing.	maa
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	_	11.0	8.25	_	11.0	) baseliu	
Output Drive Current (AL Device)	ТОН		11.0		11.0	0.20		11.0	edStates	mAc
(V <sub>OH</sub> = 2.5 Vdc) Source	HO	5.0	-3.0		-2.4	-4.2	100	-1.7	Krita-arben	1111
(VOH = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88	9.E = 955	-0.36	V ylana	0
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	1 10_ abi	-1.3	-2.25	20T	-0.9	glasms.	0
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	malanie	-3.4	-8.8	II 1490	-2.4	ugasela.	
THE PERSON NAMED IN COLUMN TWO IS NOT THE OWNER.	1.	5.0	0.64	Assenta	0.51	0.88		0.36		mAd
	IOL	10	1.6	RECOR	1.3	2.25	OT THERE	0.36	ing rotten	mAd
(V <sub>OL</sub> = 0.5 Vdc)		15	4.2		3.4	8.8		2.4		
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	_	3.4	0.0		2.49		-
Output Drive Current (CL/CP Device)	ЮН			-		-				mAd
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	A constitu	-1.7	17731.53 4/6	13811
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88		-0.36		
(V <sub>OH</sub> = 9.5 Vdc)	11	10	-1.3	-	-1.1	-2.25	ademore .	-0.9	-	306
(V <sub>OH</sub> = 13.5 Vdc)	terreneral I	15	-3.6	285	-3.0	-8.8		-2.4	ulan Plac	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52		0.44	0.88	2001 000	0.36		mAd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3	-	1.1	2.25	-	0.9	-	100
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6		3.0	8.8	DOL IN	2.4	D No-Sugn	Tug
nput Current (AL Device)	lin	15	- 003	± 0.1	-	±0.00001	±0.1	7-50	±1.0	μΑс
nput Current (CL/CP Device)	Iin	15	20 H 11	± 0.3		±0.00001	± 0.3	punitea n	±1.0	μΑс
nput Capacitance (Vin = 0)	Cin	5-	- 685	- 1	-	5.0	7.5	o The st	mel bee	pF
Quiescent Current (AL Device)	IDD	5.0	-	5.0		0.005	5.0		150	μΑс
(Per Package)		10	Q*1757 05	10	1 7 -	0.010	10	N. Prinsing	300	11515
A PROPERTY OF THE PARTY OF THE		15	-	20	-	0.015	20	- I	600	
Quiescent Current (CL/CP Device)	IDD	5.0	1 11-11	20	-	0.005	20	-	150	μΑс
(Per Package)	.00	10	-	40	DOI-	0.010	40	mad som	300	m. arch
- o zi za		15	niciani we	80	Tier enum	0.015	80	Silies un	600	latte l
Total Supply Current**1	İT	5.0	100000000000000000000000000000000000000	30	110	.96 μA/kHz		30 10 1 10	13113 8011	μΑο
(Dynamic plus Quiescent.	''	10				.96 μΑ/KHZ				μΑο
Per Package)		15	laval size			.8 · μA/kHz)				bituni
(C <sub>1</sub> = 50 pF on all outputs, all	Ozen	15			1 - 12	.υ·μΑ/κη2)	Odi			upritie
buffers switching)	minimum 1		1							1

\*T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

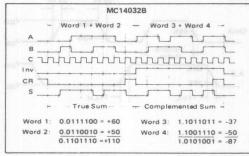
where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.003.

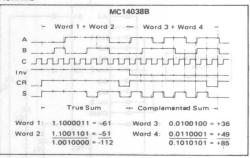
#### PIN ASSIGNMENT 1 53 VDD 16 2 - Inv 3 A3 \_\_\_\_\_ 15 3 C B3 14 4 C S2 A2 13 5 - Inv 2 B2 12 6 Carry Reset B1 11 A1 10 7 - Inv 1 8 - VSS S1 9

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit	
Output Rise and Fall Time	tTLH.					ns	
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTHL	5.0	24-1	100	200		
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns	71.12	10	- 1	50	100		
$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		15	au-rid	40	80		
Propagation Delay Time	tPLH.		-			ns	
A, B or Invert to Sum	tPHL	poseQue	Lite	14-0-		-	
tpLH, tpHL = (1.7 ns/pF) CL + 195 ns		5.0	-	280	1400		
tPLH, tPHL = (0.66 ns/pF) CL + 87 ns		10		120	300		
tpLH, tpHL = ( 0.5 ns/pF) CL + 65 ns		15	-	90	230		
Clock to Sum				bol - c		ns	
tpLH, tpHL = (1.7 ns/pF) CL + 415 ns		5.0	LIVE S	500	2400	1	
tPLH, tPHL = (0.66 ns/pF) CL + 147 ns		10	-	180	600	1.6	
tpLH, tpHL = (0.5 ns/pF) CL + 110 ns		15	-	135	450		
Input Setup Time	tsu	5.0	10	-10		ns	
	100	10	10	0	-		
		15	10	0	-	1	
Clock Pulse Frequency	fcl	5.0	-	4.0	1.0	MHz	
	lemus x 8	10	-	10	2.5		
	1011117	15	20719	12	4.0		
Clock Rise and Fall Times	tTHL, tTLH	5.0	- 1	-	15	μs	
		10	- 27	-	5		
		15	-	-	4		

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

# TIMING DIAGRAMS





Note: Unused input pins must be connected to either  $V_{\mbox{DD}}$  or  $V_{\mbox{SS}}$ .

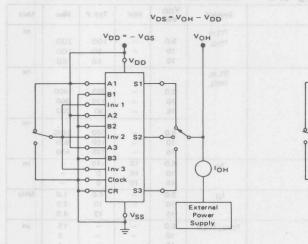
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<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14032B•MC14038B

FIGURE 1 - TYPICAL OUTPUT SOURCE TEST CIRCUIT

FIGURE 2 - TYPICAL OUTPUT SINK TEST CIRCUIT



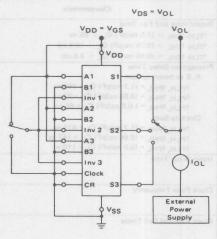
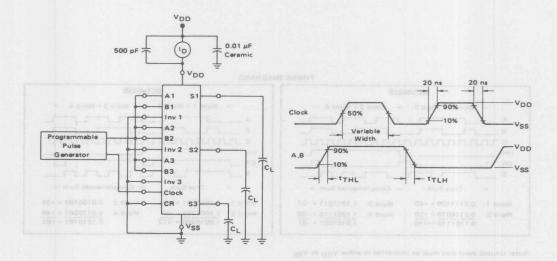
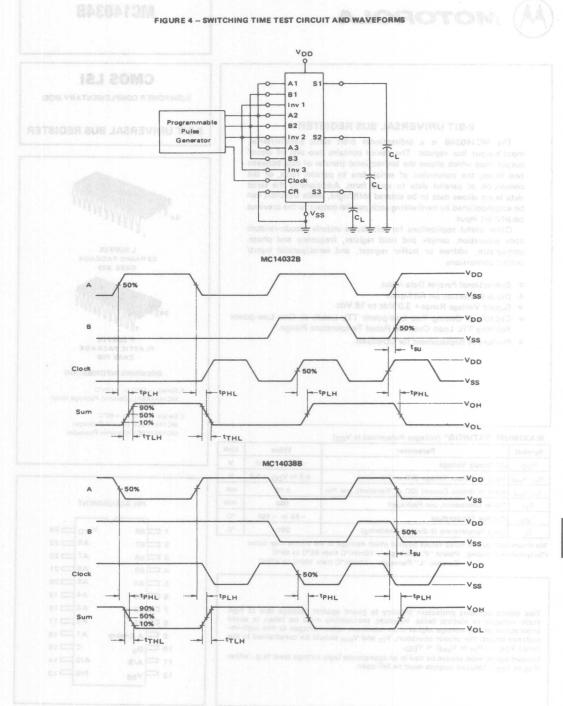


FIGURE 3 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



# MC14032B•MC14038B





# MC14034B

# **CMOS LSI**

(LOW-POWER COMPLEMENTARY MOS)

**8-BIT UNIVERSAL BUS REGISTER** 

# 8-BIT UNIVERSAL BUS REGISTER

The MC14034B is a bidirectional 8-bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allows the bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. Additionally the serial data input allows data to be entered shift/right, while shift/left can be accompolished by hard-wiring each parallel output to the previous parallel bit input.

Other useful applications for this device include pseudo-random code generation, sample and hold register, frequency and phase-comparator, address or buffer register, and serial/parallel input/output conversions.

- Bidirectional Parallel Data Input
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4034B.

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

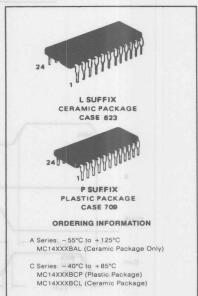
\*Maximum Ratings are those values beyond which damage to the device may occur.

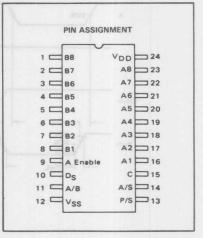
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\rm in}$  and  $V_{\rm out}$  should be constrained to the range  $V_{\rm SS} \leqslant (V_{\rm in} \text{ or } V_{\rm out}) \leqslant V_{\rm DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.





ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

Mary Type of York their	004	VDD	Tie	ow*		25°C	Lance Committee	Th	igh <sup>*</sup>	
Characteristic	Symbol	Vdc	Min Max		Min Typ#		Max	Min Max		Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	11 10 JA 1	0.05	Vdc
Vin = VDD or 0	0.0	10	-	0.05	-	0	0.05	30 Etyle	0.05	71
m dea ee	0.0	15	-	0.05	-	0	0.05	go Grova	0.05	177
"1" Level	VOH	5.0	4.95	-	4.95	5.0	86.01	4.95	STATE N	Vdd
Vin - 0 or VDD	-01	10	9.95	_	9.95	10	_	9.95	Post Time	Guerra
002 001	OLB	15	14.95	_	14.95	15	10_01	14.95	vist <u>i</u> – j	177
nput Voltage "0" Level	VIL						A GLAFF	S 1309/05	1 - 1U.F.	Vdd
(VO = 4.5 or 0.5 Vdc)	91	5.0	-	1.5	_	2.25	1.5	O Frights	1.5	4.12
(VO = 9.0 or 1.0 Vdc)		10	-	3.0	-	4.50	3.0	regit y	3.0	Second 1
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	-	4.0	-	6.75	4.0	PAST Exerts	4.0	2 . A
"1" Level	VIH	工程中					Tiese	PRINCE STREET	SELLIEN LES	4 8
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	0.8	5.0	3.5	_	3.5	2.75	9-4-TO14	3.5	CHELL R	Vdc
(VO = 1.0 or 9.0 Vdc)	61	10	7.0	-	7.0	5.50	- D III	7.0	11691	5477
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	- BE	15	11.0	-	11.0	8.25	6.4.70.4.	11.0	1021	101
Output Drive Current (AL Device)	ГОН							06/87	elett (2010	mAd
(VOH = 2.5 Vdc) Source	•	5.0	-1.2	-	-1.0	-1.7	ristQ_tolla	-0.7	None A II	2 A
(VOH = 4.6 Vdc)		5.0	-0.25	-	-0.2	-0.36	- 198	-0.14	mi La i	A 8
(V <sub>OH</sub> = 9.5 Vdc)	0.0	10	-0.62	-	-0.5	-0.9	- 10 U	-0.35	Librar F	141
(V <sub>OH</sub> = 13.5 Vdc)	01	15	-1.8	-	-1.5	-3.5	1 70 1.00	-1.1	* JP#P .N	101
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	_	0.51	0.88	sea Times	0.36	20.50	mAd
(Vol. = 0.5 Vdc)	0.8	10	1.6	-	1.3	2.25	-	0.9	SERVICE DESIGNATION	Side Side
(VOL = 1.5 Vdc)	0.0	15	4.2	-	3.4	8.8	-	2.4	-	1
Output Drive Current (CL/CP Device)	ГОН									mAd
(VOH = 2.5 Vdc) Source	85.8	5.0	-1.0	-	-0.8	-1.7	-	-0.6	per Lagra	SolboiU
(VOH = 4.6 Vdc)	01 1	5.0	-0.2	-	-0.16	-0.36	-	-0.12		
(V <sub>OH</sub> = 9.5 Vdc)	01	10	-0.5	-	-0.4	-0.9	-	-0.3	-	
(V <sub>OH</sub> = 13.5 Vdc)	0.8	15	-1.4	-	-1.2	-3.5	-	-1.0	op/Files	94900
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAd
(VOL = 0.5 Vdc)	81	10	1.3	-	1.1	2.25	-	0.9	_	
(V <sub>OL</sub> = 1.5 Vdc)	0.8	15	3.6	-	3.0	8.8	-	2.4	pursi2 is o	18 A
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μAd
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	±0.3		±1.0	μAd
Input Capacitance	Cin	1517		-	-	5.0	7.5	-	1000	pF
(V <sub>in</sub> = 0)	o in									
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.010	5.0	-	150	μAd
(Per Package)	טטי	10	_	10	to give a	0.020	10	TOUGHS HE	300	O PAT
		15	-	20	-	0.030	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	50	BO - 375	0.010	50	00-000	375	μAd
(Per Package)	יטטי	10		100	_	0.020	100		750	μΑσ
(i ci i denage)		15	_	200	_	0.030	200	_	1500	1
Total Supply Current**†	IT	5.0	-		1 -				1000	μAd
(Dynamic plus Quiescent,	'1	10	STRAT P			(2.2 μA/kH; (4.4 μA/kH;				μΑσ
Per Package)	MOLLAR	15				(6.6 μA/kH				
(C <sub>1</sub> = 50 pF on all outputs, all	I Price I Price	13				υ.υ μΑ/κτι	, , , , , ,			-
buffers switching)	th lethouse	S BING A A	Can ateb							
		-				T				
3-State Output Leakage Current	ITL	15	erado tello	±0.1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	±0.0001	±0.1	-	±3.0	μAdc
(AL Device)	-1,-1		-	and the same	-		1	-		
3-State Output Leakage Current	ITL	15	-	±1.0	1	±0.0001	±1.0	1	±7.5	μAdc
(CL/CP Device)			-		-		market find	and the same		1

 $<sup>^*</sup>T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ V1k}$ 

where: IT is in  $\mu A$  (per package),  $C_L$  in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.004.

Charact	eristic	250	100	T ST	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise Time A or B  tTLH = (3.0 ns/pF) CL + 30 ns  tTLH = (1.5 ns/pF) CL + 15 ns  tTLH = (1.1 ns/pF) CL + 10 ns	0 0		80.6 80.0 80.0		tTLH	5.0 10 15	lava J 10	180 90 65	360 180 130	en V
Output Fall Time A or B tTHL = (1.5 ns/pF) CL + 25 ns tTHL = (0.75 ns/pF) CL + 12.5 n tTHL = (0.55 ns/pF) CL + 9.5 ns	81 81	69.8 20.81		80.0	tTHL	5.0 10 15	m, J 0	100 50 40	200 100 80	ns
Propagation Delay Time A (B) Synchronous Paralles Data B (A) Parallel Data Output tp_H, tpHL = (1,7 ns/pF) C_L + 4 tpH, tpHL = (0.66 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpH, tpHL = (0.55 ns/pF) C_L + tpHL = (0.55 ns/	Input, 40 ns 172 ns	8.6	3.0	8.0	tPLH, tPHL	5.0 10 15	acas nen	525 205 145	1050 410 290	ovi ovi ovi
Propagation Delay Time  A (B) Asynchronous Parallel Date B (A) Parallel Date Output  tp_H, tpHL = (1.7 ns/pF) CL + 4  tp_H, tpHL = (0.66 ns/pF) CL +  tp_H, tpHL = (0.5 ns/pF) CL + 1	120 ns 147 ns	0.1- 0.0- 0.9- 2.1-		2.1 85.1 58/8	tPLH, tPHL	5.0 10 15	tsosia ismuo	505 180 130	1010 360 260	HOVI HOVI
Clock Pulse Width	2.25	6.1 h G		B.	WH	5.0 10 15	340 140 110	170 70 55	o∨ 50 × o∨ 5 ×	ns
Clock Pulse Frequency	7.3- 80.9- 8.0-	8.0- 81.0- 4.0-	7	0.1 5.0 8.0	f <sub>cl</sub>	5.0 10 15	- T5:sun	2.5 6.0 8.0	1.2 3.0 4.0	MH
Clock Pulse Rise	-0.5 0.48 0.39	\$4.0 14.0		52	TLH, THL	5.0 10 15	- 300	- (ab	15 5 4	μs
A, B Input Setup Time	8.8	3.0	101	3.1	t <sub>su</sub>	5.0 10 15	100 45 35	35 15 12	AV 3-1 o	ns
High Level SE, P/S, A/S Pulse Width	0.0				₩H	5.0 10 15	600 270 200	200 90 80	constitue (0)	ns

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

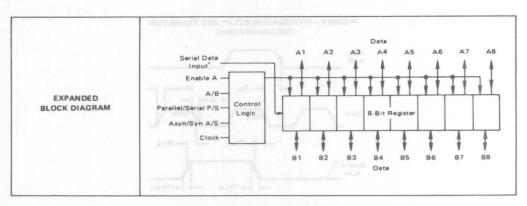
# TRUTH TABLE

					armanacia alla permanyo
"A" Enable	P/S	A/B	A/S	MODE	OPERATION!
0	0	0	×	Serial	Synchronous Serial data input, A and B parallel data outputs disabled.
0	0	1	×	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs.
1	0	0	×	Serial	Synchronous serial data input, A Parallel data output.
1	0	1	×	Serial	Synchronous serial data input, B-Parallel data output.
1	1	0	0	Parallel	B-Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B-Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A-Synchronous Parallel data input, B-Parallel data output.
Say no 1 pp V	1	V.10	1	Parallel	A-Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

<sup>†</sup>Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode.

During transfer from parallel to serial operation, A/S should remain low in order to prevent D<sub>S</sub> transfer into flip-flops.



# **OPERATING CHARACTERISTICS**

The MC14034B is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D" master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input — When high, this input enables the bus A data lines.

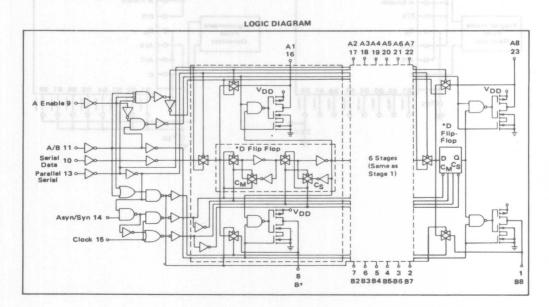
A/B Input (Data A or B) - This input controls the direction of data flow: when high, the data flows from

bus A to bus B; when low, the data flows from bus B to bus A.

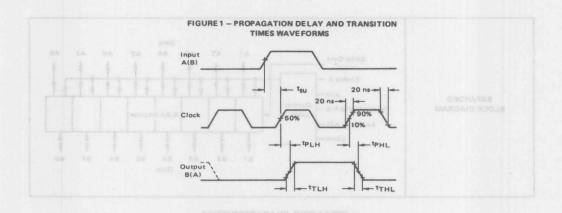
P/S Input (Parallel/Serial) — This input controls the data input mode (parallel or serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

A/S Input (Asynchronous/Synchronous to the Clock)

When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.



# MC14034B



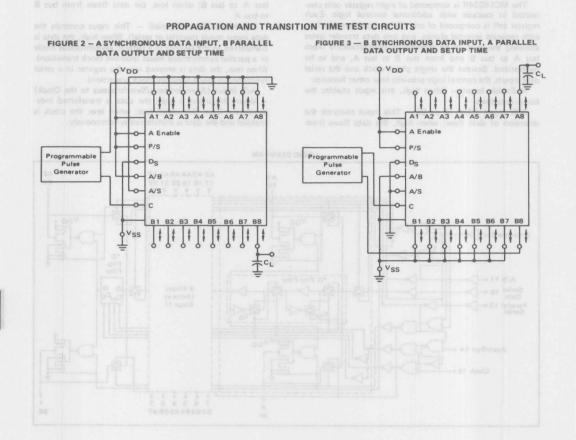
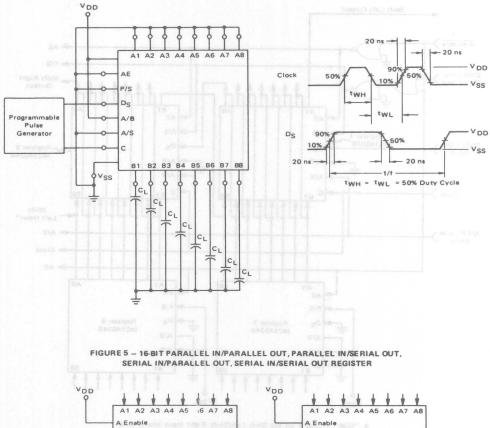
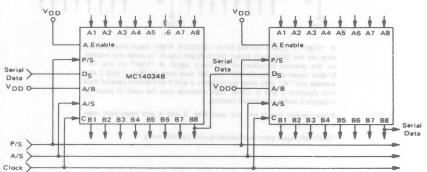
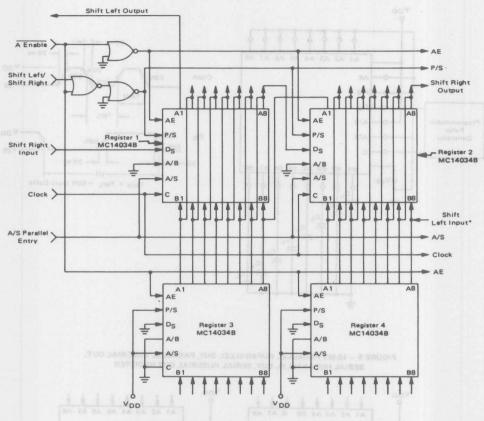


FIGURE 4 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS





# FIGURE 6 - SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

\*Shift left input must be disabled during parallel entry.



# MC14035B

# 4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

The MC14035B 4-bit shift register is constructed with MOS Pchannel and N-channel enhancement mode devices in a single monolithic structure. It consists of a 4-stage clocked serial-shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial-right shifting of data or synchronous parallel loading via inputs Dpo thru Dp3. The True/Complement (T/C) input determines whether the outputs display the Q or Q outputs of the flip-flop stages. J-K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial "D" input.

This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers,

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J-K Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- No Limit on Clock Rise and Fall Times
- · All Inputs are Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

# **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER



CERAMIC PACKAGE CASE 620

PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

# MAXIMUM RATINGS\* (Voltages Referenced to Voc)

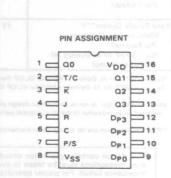
Symbol	Parameter and	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	0.5 to + 18.0	V.
Vin. Vout	Input or Output Voltage (DC or Transient)	0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> . I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	+ 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	65 to - 150	С
TL	Lead Temperature (8-Second Soldering)	260	C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: 12mW/°C from 65°C to 85°C Ceramic "L" Package: 12mW/°C from 100°C to 125 °C

# TRUTH TABLE

1		INP	UTS	tn OUTPUT	
	C	J	K	R	QO
	_	0	0	0	0
1	5	0	1	0	Q0 (n - 1)
1		1	0	0	Q0 (n - 1)
T		1	1	0	1
1	7	×	×	0	Q0:(n-1)
1	×	×	ж	1	0

x = Don't Care P/S = 0 = Serial Mode T/C = 1 = True Outputs



		VDD	Tic	w*		25°C		Thi	gh *	1
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
$V_{in} = V_{DD}$ or 0	00	10	-	0.05	_	0	0.05		0.05	-
111 00		15	-	0.05	E N.	0	0.05	100 to 100	0.05	
"1" Level	VOH	5.0	4.95	-	4:95	5.0	VIII.0-1.1/4	4.95	_	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	- OH	10	9.95	_	9.95	10	FRIENCE	9.95	_	1
		15	14.95	tion Trains	14.95	15	-	14.95		-
Input Voltage "0" Level	VIL		77.00	other posts			-311002-31			Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	VIL.	5.0	Audin 215	1.5	DIVISO BE	2.25	1.5	9000000	1.5	1000
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	Striffer 35	3.0	00900010	4.50	3.0	100 11 3	3.0	Serious.
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	A4 I	15	ET Jibuqi	4.0	iq betst	6.75	4.0	160 11-0	4.0	drive
(VO = 13.5 of 1.5 vdc)	VIH	13	100	4.0	1000 000	0.75	tulis iut	1017	OF STREET	Vdc
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	VIH	5.0	3.5	Be Fine	3.5	2.75	S BOY-DIT	3.5	neg_sue	Vac
(V <sub>O</sub> = 1.0 or 9.0 Vdc)			THE RESERVE AND ADDRESS.	stib atuo	U-125 23255	5.50	minutate	7.0	DATA SHE	male
	and the second	10	7.0	ting the s	7.0	8.25	a dolt o	11.0	PERMIT	5 10
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	-	15	11.0		11.0	8.25	N 1 1111	11.0	10 13312 0	-
Output Drive Current (AL Device)	IOH						brani	-1.7		mAdd
(VOH = 2.5 Vdc) Source	Section 1	5.0	-3.0	TitleAres	-2.4	-4.2	ALTHUR IS		- 11 - 10 H	pipiyo
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88	V177-3118	-0.36	OIVE) IN	1
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	uantes .	-1.3	-2.25	G)-11119	-0.9	400年16月	A183
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	a mehma	-3.4	-8.8	0.01 TIES	-2.4	Notion of the last	noir
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	Horl-Inne	0.51	0.88	on exact	0.36	euten?	mAde
(VOL = 0.5 Vdc)		10	1.6	-	1.3	2.25		0.9	-	inte
(VOL = 1.5 Vdc)		15	4.2	-	3.4	8.8	OUT S. Sel	2.4	in annual	
Output Drive Current (CL/CP Device)	ГОН		150000		Linia and	F	4			mAdo
(VOH = 2.5 Vdc) Source	0	5.0	-2.5	- "	-2.1	-4.2	WDEGJ I	-1.7	pue nisa	40 0
(V <sub>OH</sub> = 4.6 Vdc)	*	5.0	-0.52	-	-0.44	-0.88	12119	-0.36	feine? 2	(L. 8
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	Guilput	-1.1	-2.25	Paris Of	-0.9	nositione	0
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4		
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88		0.36	_	mAdo
(VOL = 0.5 Vdc)	·OL	10	1.3	_	1.1	2.25	TOWN US	0.9	tordany	
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	meral stor	3.0	8.8	ns on the	2.4	nas Trans	1 0
Input Current (AL Device)	lin	15	-	± 0.1		±0.00001	±0.1	SISKED IN	± 1.0	μAdo
Input Current (CL/CP Device)		15	-	± 0.3	-	±0.00001	± 0.3	3102 00	±1.0	μAdo
	lin									1
nput Capacitance	Cin	-		-	39. V	5.0	7.5	sR-spot	oh Aldih	pF
(V <sub>in</sub> = 0)		181	Low-poly	ent) pag	peod 45	1 189/cm-1	coul cerT	aniving.	s alden	0.0
Quiescent Current (AL Device)	IDD	5.0	-	5.0	British 160	0.005	5.0	b bet 1	150	μAdo
(Per Package)		10	-	10	-	0.010	10	-	300	
		15		20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20	-	150	μAdo
(Per Package)		10	-	40	1507	0.010	40	Al -6-01	300	20011
	the said	15	- 300	80	-	0.015	80	-	600	Tesus
Total Supply Current**†	IT	5.0	Tr. 29	134.0	I= (1	.0 μA/kHz)	f + Inc	- about	Vinisus II	. μAdα
(Dynamic plus Quiescent,		10				.0 μA/kHz)				1
Per Package)		15	8- GO			.0 µA/kHz)				Law
(C <sub>1</sub> = 50 pF on all outputs, all		Ame	61		11 - 13	PAIN1121				nun
buffers switching)										1

 $<sup>^*</sup>T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 pF) + (C_L - 50) Vfk$ 

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where:  $I_T$  is in  ${\mu}A$  (per package),  $C_L$  in pF,  $V=(V_{\mbox{DD}}-V_{\mbox{SS}})$  in volts, f in kHz is input frequency, and k=0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\text{in}}$  and  $V_{\text{out}}$  should be constrained to the range  $V_{\text{SS}} \leqslant (V_{\text{in}} \text{ or } V_{\text{out}}) \leqslant V_{\text{DD}}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{\text{SS}}$  or  $V_{\text{DD}}$ ). Unused outputs must be left open.

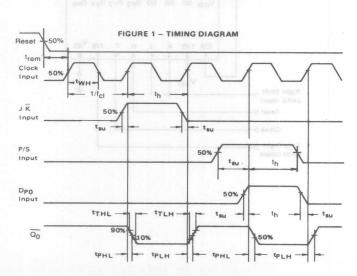
<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C, See Figure 1)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise and Fall Time TTLH, TTHL= (1.5 ns/pF) C <sub>L</sub> +25 ns TTHL, TTHL= (0.75 ns/pF) C <sub>L</sub> +12.5 ns T <sub>TLH</sub> , T <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> +12.5 ns	<sup>t</sup> TLH, <sup>t</sup> THL	5.0 10 15	=	100 50 40	200 100 80	ns
Propagation Delay Time, Clock or Reset to Q  TPLH, TPHL= (1.75 ns/pF) C <sub>L</sub> + 223 ns  TPLH, TPHL= (0.70 ns/pF) C <sub>L</sub> + 89 ns  TPLH, TPHL= (0.53 ns/pF) C <sub>L</sub> + 67 ns	<sup>†</sup> PLH, <sup>†</sup> PHL	5.0 10 15	Ξ	300 130 95	600 260 190	ns
Clock Pulse Width	tWH	5.0 10 15	335 165 125	135 45 40		ns
Reset Pulse Width	twH	5.0 10 15	400 175 130	80 40 35	=	ns
Reset Removal Time	trem trem	5.0 10 15	80 30 25	40 15 10	Œ	ns
Clock Pulse Rise and Fall Time	tTLH, tTHL	5.0 10 15		No Limit		- 78
Clock Pulse Frequency	fcl	5.0 10 15	=	2.5 6.0 10	1.2 2.0 3.0	MHz
J-K to Clock Setup Time	t <sub>su</sub>	5.0 10 15	500 200 150	120 50 30	=	ns
Clock to J-K Hold Time	th	5.0 10 15	40 30 25	- 40 - 5 0	=	ns
P/S to Clock Setup Time	t <sub>su</sub>	5.0 10 15	500 200 150	25 10 7.5	=	ns
Clock to P/S Hold Time		5.0 10 15	30 20 20	- 70 - 20 - 10	=	ns
Dp to Clock Setup Time	t <sub>su</sub>	5.0 10 15	500 200 150	90 20 15	=	ns
Clock to Dp Hold Time	th	5.0 10 15	90 40 40	- 25 0 5	=	ns

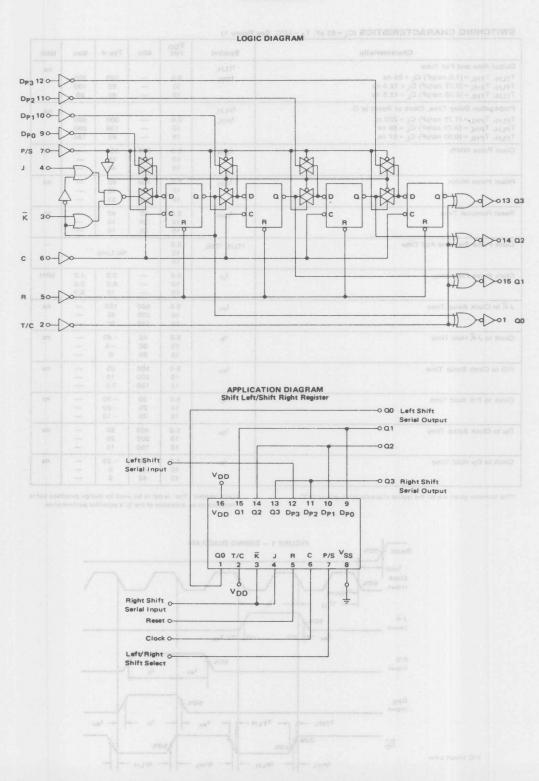
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



T/C Input Low

### MC14035B





#### TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Buffered Outputs
- Single-Phase Clocking
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B.

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
i <sub>in</sub> , l <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Piastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

# MC14038B

FOR COMPLETE DATA
SEE MC14032B

#### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

#### TRIPLE SERIAL ADDERS

Positive Logic - MC14032B Negative Logic - MC14038B

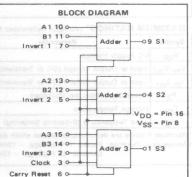


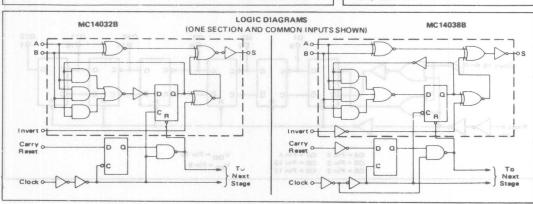
L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)







#### 12-BIT BINARY COUNTER

The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- Pin-for-Pin Replacement for CD4040B

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

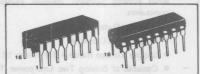
Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

#### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

12-BIT BINARY COUNTER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C

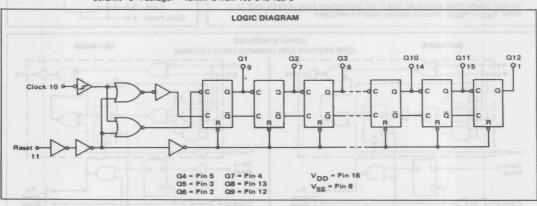
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
5	0	No Change
~	0	Advance to next state
X	1	All Outputs are low

X = Don't Care



ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

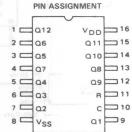
	0.550	VDD	Tio	w"		25°C		Thi		
Characteristic	Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0		0.05	-	0	0.05	MOTEL IN	0.05	Vdc
$V_{in} = V_{DD}$ or 0	-	10	1.8 - 1	0.05	- 1	0	0.05	3 (Sgush	0.05	HUTT
001 001	No.	15	21	0.05	-	0 40	0.05	(Plo <u>u</u> en al	0.05	HITT
"1" Level	VOH	5.0	4.95		4.95	5.0	18.67	4.95	(D) =_1 (1	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	011	10	9.95		9.95	10	-	9.95	mistTee	2000019
		15	14.95	4674)	14.95	15		14.95		A CONTRACTOR
Input Voltage "0" Level	VIL			1914		00.7		Henon 3		Vdc
$(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$		5.0	- 1	1.5		2.25	1.5	Totan 88.4	1.5	Tistule
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$		10	-	3.0	-	4.50	3.0	-	3.0	To Let
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	- 1	4.0	-	6.75	4.0	Agen 8.9	4.0	Theat
"1" Level	VIH								810	/ Steel C
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$		5.0	3.5		3.5	2.75	M2 - 101	3.5	- Tura)	Vdc
$(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$		10	7.0	_	7.0	5.50	- 8	7.0	- Target	1000
$(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$		15	11.0	-	11.0	8.25	ea = 100	11.0	- FLU?	
Output Drive Current (AL Device)	10Н	in the same of	-							mAdc
(VOH 2.5 Vdc) Source	0	5.0	-3.0	Jan	-2.4	-4.2	-	-1.7	Select Detail	Fropass
(VOH - 4.6 Vdc)		5.0	-0.64	_	-0.51	-0.88	_	-0.36	-20	town St
(VOH = 95 Vdc)		10	-1.6	-	-1.3	-2.25	01-201	-0.9	an Series	Inval
(V <sub>OH</sub> = 13.5 Vdc)	-	15	-4.2	-	-3.4	-8.8	en <del>a</del> si	-2.4	n Bi <del>n</del> ti -	1125
(VOL = 0.4 Vdc) Sink	OL	5.0	0.64	-	0.51	0.88	E2-841	0.36	an 2-3) =	mAdc
$(V_{OL} = 0.5 \text{ Vdc})$		10	1.6		1.3	2.25	_	0.9	_	
(VOL = 1.5 Vdc)	285	15	4.2	147/42	3.4	8.8	_	2.4	tibry opi	45000
Output Drive Current (CL/CP Device)	ГОН									mAdc
(VOH = 2.5 Vdc) Source	On	5.0	-2.5		-2.1	-4.2	_	-1.7	_	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	100	-0.44	-0.88	_	-0.36	provide from	Stoots I
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3		-1.1	-2.25	-	-0.9	-	
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	_	-2.4	_	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88		0.36	_	mAdc
(V <sub>OL</sub> = 0.5 Vdc)	02	10	1.3	HTTL:HU	1.1	2.25	_	0.9	FI Shu ne	2000
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8		2.4		
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1		± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	18 - 1	± 0.3	-	±0.00001	± 0.3	-	±1.0	μ:Adc
Input Capacitance	Cin	_			-	5.0	7.5		_	pF
(V <sub>in</sub> - 0)	OTE					0.0	7.5			P.
Quiescent Current (AL Device)	IDD	5.0	1 -	5.0	-	0.005	5.0	-	150	μAdc
(Par Package)	100	10	-	10	-	0.010	10	- 10	300	-
(Terrackage)	0.0	15	- 1	20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0		20		0.005	20		150	μAdc
(Per Package)	100	10		40	DOUR 16 VI	0.003	40	will not on	300	MAGE
		15		80	al Kid ana	0.015	80	(d s1,2011 s)	600	Digta Inde
Total Supply Current**†	IT	5.0		00	1 10	42 μA/kHz			000	μAdc
(Dynamic plus Quiescent,		10	1			.85 μA/kHz				MAGE
Per Package)		15				43 µA/kHz				
(C <sub>1</sub> 50 pF on all outputs, all						AS MAINIA				
buffers switching)	AUDIT									

 $<sup>^*</sup>T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I\_T is in  $\mu$ A (per package), C\_L in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or V<sub>DD</sub>). Unused outputs must be left open.



<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

SWITCHING CHARACTERISTICS (CL = 50 pF, TA = 25°C)

Characteristic	20	Symbol	V <sub>DD</sub> V <sub>dc</sub>	Min	Тур#	Max	Unit
Output Rise and Fall Time	22. 1. 19	tTLH.	BILLIAN TO BUILD	1100/11/1	1	211312373111411	ns
T <sub>TLH</sub> , T <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns		T DOMES	5.0	104	100	200	ALTERNATION CONTRACTOR
T <sub>TLH</sub> , T <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns		<sup>t</sup> THL	10		50	100	dea - man
		80.6			200		
$T_{TLH}$ , $T_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	35 1 60		15	YOR-	40	80	
		TOLU.	SE 8 1 0				O U P OF
Clock to Q1		tPHL t	GE 57 - 8				ns
tpHL, tpLH = (1.7 ns/pF) CL + 315 ns			5.0	IV	260	520	secilary te
tpHL, tpLH = (0.66 ns/pF) CL + 137 n	S	31 1	10	_	115	230	Sh - 010
tpHL, tpLH = (0.5 ns/pF) CL + 95 ns		0.5	15		80	160	D.8 - 04
		0.0	10			(00) 1 1 10	No 188
Clock to Q12				HIV.	13407 E		ns
tpHL, tpLH = (1.7 ns/pF) CL + 2415 n			5.0	-	1625	3250	NO - ON
tpHL, tpLH = (0.66 ns/pF) CL + 867 n	S		10	-	720	1440	0 1 - 0V9
$t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_{L} + 475 \text{ ns}$			15		500	1000	23 - OK)
Propagation Delay Time	5- LAS	tPHL		- 一相儿	1 1991	U ZA/ TALE U	ns
			0 0 0		- 60004		1200
tpHL = (1.7 ns/pF) C <sub>L</sub> + 485 ns			5.0		370	740	Ba JROAD
					Pania -		ER HIGHT
THE CONTRACTOR OF THE CONTRACT		all project or the second	10	1	155	310	EL HOAL
	60   12		15	E 1 207	115	230	NO - 10 VI
Clock Pulse Width			5.0	385	140	- 1309	ns
			10	150	55	1304	E. 1.20 Y
			15	115	38	IONJOI VIIINI	D SWING ROOM
Clock Pulse Frequency	0.1 152	fcl	5.0	2	2.1	1.5	MHz
25 - 1 - 0 - 1 - 1 - 25		'GI	10		7.0	3.5	Par - Labors
			15		10.0	4.5	DI THEN
			13		10.0	4.5	100
Clock Rise and Fall Time		tTLH, THL	5.0	The second			ns
			10		No Limit		E.F. 1000
		10.	15				200000000000
Reset Pulse Width	80.62	twH	5.0	960	320	Killer Carrier In	ns
		.vvr	10	360	120		
			15	270	80		HITTERS TO THE
Peast Demoisl Time	0.0	.02	- 0			Signed LAS resi	
Heset Hemoval Time		trem	5.0	130	65	-	ns
		os I	10	50	25	11 15 -	
		- Inches	15	30	15		

<sup>&</sup>quot;The formulas given are for the typical characteristics only at 25°C.

#### FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

# Pulse Generator Pulse Generator Pulse Generator Pulse Generator Pulse Generator Pulse Generator Pulse Generator Pulse Generator Pulse Generator Pulse Generator Pulse Generator

90% 50% 10%

50% Duty Cycle

Clock

# Pulse Generator Clock 20 ns Clock 20 ns Clock 20 ns Clock 20 ns Clock 20 ns Clock 20 ns Clock 20 ns Clock 20 ns

TTLH THL

FIGURE 2 - SWITCHING TIME TEST

CIRCUIT AND WAVEFORMS

VDD

6

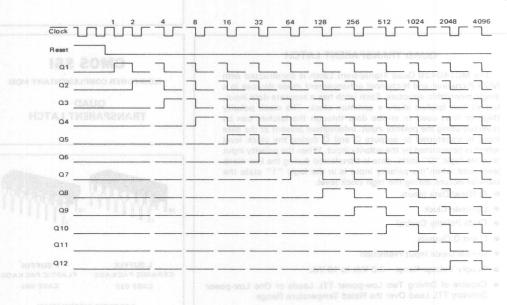
VDD

-Vss

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 3 - TIMING DIAGRAM



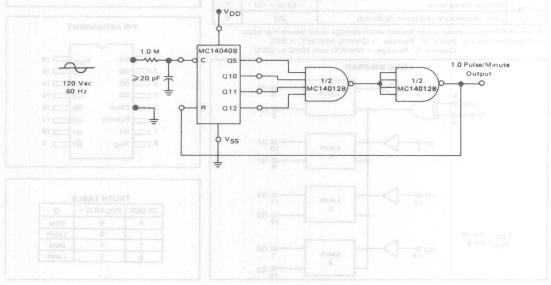


#### **APPLICATIONS INFORMATION**

#### TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by

3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



#### QUAD TRANSPARENT LATCH

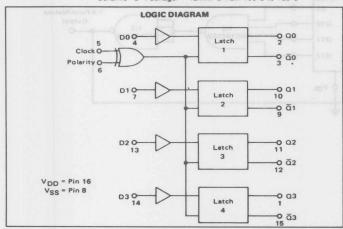
The MC14042B Quad Transparent Latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and  $\overline{\mathbf{Q}}$  during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

- Buffered Data Inputs
- Common Clock
- Clock Polarity Control
- Q and Q Outputs
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧-
In lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

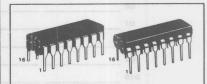
\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic: "P" Package: -12mW/°C from 65°C to 85°C
Ceramic: "L" Package: -12mW/°C from 100°C to 125°C



#### **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

QUAD TRANSPARENT LATCH

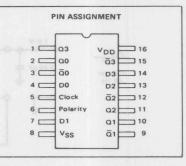


L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



CLOCK	POLARITY	Q
0	0	Data
1	0	Latch
1	1	Data
0	1	Latch

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

Brill xaM 6 get cité	raceV 1	VDD	Tio	w*		25°C		Thi	gh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	(Reine 8	0.05	Vdc
Vin VDD or 0	er	10	-	0.05	-	0	0.05	Photom and	0.05	i sa rri
08 00 -	ar i	15	-	0.05	-	0	0.05	Charlet Bar	0.05	10000
"1" Level	VOH	5.0	4.95	_	4.95	5.0	70	4.95	valo 0 cites	Vdc
Vin - 0 or VDD	9.8	10	9.95	-	9.95	10	10 A	9.95	- ( <u>Fig.</u>	No September
001 00 -	0.1	15	14.95	_	14.95	15		14.95	1919).	129
Input Voltage "0" Level	VIL			N. F. S.		-	80 4 10	Salan A.O		Vdc
(VO = 4.5 or 0.5 Vdc)		5.0	-	1.5	-	2.25	1.5	-	1.5	2.50
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	5.0	10	-	3.0	-	4.50	3.0	Farea, Old a. J. Sulpul	3.0	Bargo!
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	100	15		4.0	_	6.75	4.0	HIDIO 1. 1	4.0	114
"1" Level	VIH						30.7			-
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	- 101	5.0	3.5		3.5	2.75	oter ju.	3.5	766	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	_	7.0	5.50	_	7.0	dition -	1 2000
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	0.3	15	11.0	_	11.0	8.25	_	11.0	_	1
Output Drive Current (AL Device)	ІОН		1110		11.0	0.20		1		mAdo
(VOH = 2.5 Vdc) Source	·OH	5.0	-3.0	_	-2.4	-4.2	_	-1.7	_	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88	0.00	-0.36	pelB pau	H HaptC
(V <sub>OH</sub> = 9.5 Vdc)	0.0	10	-1.6	_	-1.3	-2.25	_	-0.9	_	
(V <sub>OH</sub> = 13.5 Vdc)	O.s.	15	-4.2	_	-3.4	-8.8	_	-2.4	_	
	1	5.0	0.64		0.51	0.88		0.36		mAdo
04 - 05 44-1	OL	10	1.6		1.3	2.25	_	0.30	_	MAGG
(V <sub>OL</sub> = 0.5 Vdc)	0.8	15	4.2		3.4	8.8	_	2.4	_	
(V <sub>OL</sub> = 1.5 Vdc)	the	15	4.2	-	3.4	0.0		2.4		-
Output Drive Current (CL/CP Device)	ЮН									mAdd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	ri marsi
(V <sub>OH</sub> = 4.6 Vdc)	0.8	5.0	-0.52	=	-0.44	-0.88	-	-0.36	_	
(V <sub>OH</sub> = 9.5 Vdc)	101	10	-1.3	-	-1.1	-2.25	-	-0.9	_	
(V <sub>OH</sub> = 13.5 Vdc)	386 - 13	15	-3.6	-	-3.0	-8.8		-2.4	-	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdd
(V <sub>OL</sub> = 0.5 Vdc)	- 431	10	1.3	-	1.1	2.25	10.40 Tel 7-09	0.9		Big is a
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8	No. Tender	2.4		de Later Co
Input Current (AL Device)	lin	15	-	± 0.1	-0.010	± 0.00001	± 0.1	to to mobile;	± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	± 1.0	μAdo
Input Capacitance (V <sub>in</sub> = 0)	Cin	-		-	-	5.0	7.5	-	-	pF
Quiescent Current (AL Device)	Ipp	5.0	-	1.0	-	0.002	1.0	-	30	μAdo
(Per Package)	-00	10	ero Trant	2.0	EN DISSE	0.004	2.0	เลยีเล	60	
distriction of	Periodo I Pe	15	110 100 1	4.0	DEIG HI	0.006	4.0	HEREIT A	120	
Quiescent Current (CL/CP Device)	IDD	5.0	-	4.0	1 -	0.002	4.0	<u> </u>	30	μAdo
(Per Package)	.00	10		8.0	_	0.002	8.0		60	, made
. C. Jonager		15	_	16		0.004	16	_	120	
Total Supply Current**†	IT	5.0			I= 1	1.0 µA/kHz)				μAdo
(Dynamic plus Quiescent,		10				2.0 $\mu$ A/kHz)				I MAGE
Per Package)		15				3.0 µA/kHz)				
(C <sub>1</sub> = 50 pF on all outputs, all	3	- Date	ateta .		1000	o. o portinital				
buffers switching)	pri lop-15	Just								

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

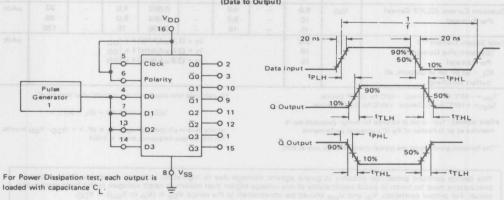
where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.004.

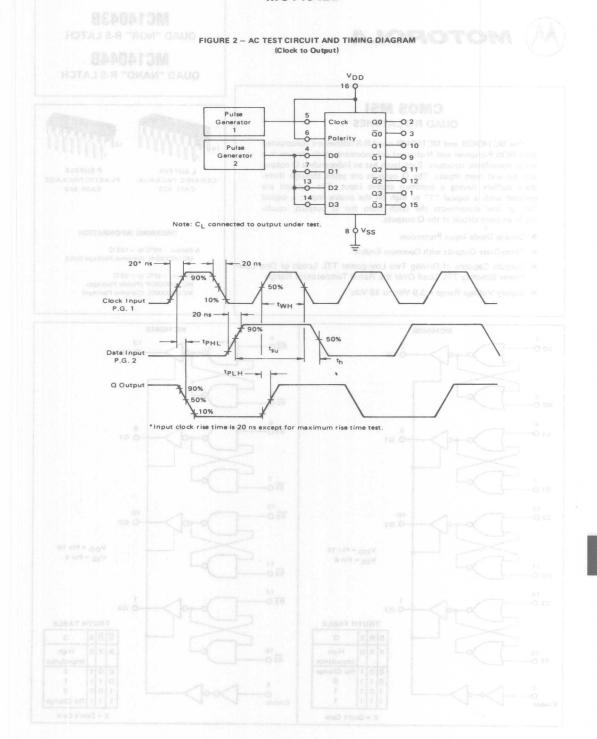
		Chara	acteristic				Symbol	VDD	Min	Тур#	Max	Unit
Output Rise and Fall	Time	4500	1 10 10 10	1000	21814	A September 1	tTLH.	the special state		or persons	0.0000	ns
tTLH, tTHL = (1.5	ns/pF) Ci	+ 25	ns				tTHL	5.0	1-04	100	200	Surprac Sec
tTLH, tTHL = (0.7							er 1	10		50	100	E-W
t <sub>TLH</sub> , t <sub>THL</sub> = (0.5							H et 1	15	-	40	80	
			.0 110	1 30 A	Description of the last of the	62.5	tPLH.	HOV	Here J.			ns
Propagation Delay Ti tpLH, tpHL = (1.			25 00					5.0	_	220	440	N W
tPLH, tPHL = (0.	ee sainEl	C + 12	55 ns				tPHL	10		90	180	
TPLH, TPHL - 10.	E == /= E \	C + 35	57 118				-	15	level 0	60	120	Nov tuen
tpLH, tpHL = (0.			-					13		00		
Propagation Delay T							tPLH,			130.4	2.0 90 6.1	ns
tPLH, tPHL = (1.	.7 ns/pF)	CL + 13	35 ns				\$PHL	5.0	-	220	440	OV
tPLH, tPHL = (0.	.66 ns/pF)	) CL + 5	57 ns				1-74-4	10	-	90	180	L. O.A.
tPLH, tPHL = (0.	5 ns/pF)	CL + 35	5 ns					25	Invitu	60	120	
Clock Pulse Width	0.5			6.0			HW³			THE U	THE PART OF	ns
							91	5.0	300	150	0.0 10 0.1	DAL.
							31	10	100	50	. 5 eg 13:	FOW)
								15	80	40	and w	rd number
Clock Pulse Rise an	d Fall Tim	ne	AR.O.				tTLH.		9314	114	TOV GE	μѕ
							tTHL	5.0	-	-	15	HOW
							95	10	i -	-	5.0	- INON
								15	_	- 19	4.0	HOVI
Hold Time	-		900	1100		700	th	301	1 3	100	75 Y F. O	ns
							1000	5.0	100	50	56V 2.0	10VI
							87	10	50	25	1.8 V.8:1	E DECKLE
								15	40	20	ense su	D tunnui
Setup Time	2777		5.77	1000	7	0.5-			1074	12	SAN	ns
							tsu	5.0	50	0	SEV BW	
							01	10	30	0	56V20	
							1 at 1	15	25	0	DV ALELO	HOVI
SBAM I	ar a T		100.0	76577		T VED		10.1		10	- BOX B O	C 121

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 — AC AND POWER DISSIPATION TEST CIRCUIT AND TIMING DIAGRAM (Data to Output)





QUAD "NOR" R-S LATCH

MC14044B

QUAD "NAND" R-S LATCH

# CMOS MSI

The MC14043B and MC14044B quad R-S latches are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three-state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- Double Diode Input Protection
- Three-State Outputs with Common Enable
- Outputs Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc





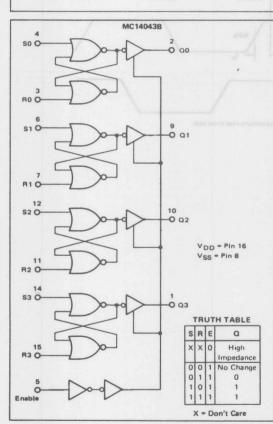
L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

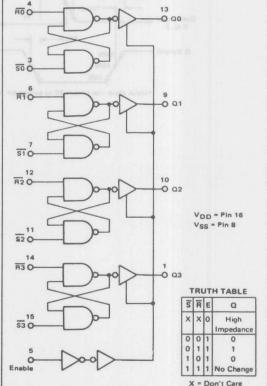
#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

MC14044B





# MC14043B•MC14044B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

diri of euh seumen tankus bish		Vpp	Tic	w		25°C	Paulot	Thi	igh "	GAMAB
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min Max		Unit
Output Voltage "0" Level	VOL	5.0		0.05	_	0	0.05	-	0.05	Vdc
TWO TY - STO INCIDENT SERVICE YE	·OL	10	t dgV o	0.05	(200	0	0.05	10dino	0.05	S 444x
ROUG BOUNDARHALINES FOR M. TORING		15	0.00	0.05	1841(274)	0	0.05	) healaid i	0.05	10 100
oper operation, Vin and Vous shor	1/-	5.0	4.95		4.95	5.0	on Target	4.95	100-3	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	VOH	10	9.95		9.95	10		9.95		1
A lu - o oi ADD		15	14.95		14.95	15	1010	14.95	s ganole)	883
		13	14.55	-	14.55	13	2100 613	14.55	0.000	Vdc
Input Voltage "0" Level	VIL				nonrealt	2.25	1.5	88-002-810i	1.5	Vac
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$		5.0	O'All of	15	214-9	4.50	3.0	direct Pres	3.0	agna?
$(V_0 = 9 \text{ or } 1.0 \text{ Vdc})$		10	125		DAWNER!		4.0	re3	4.0	
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15		4.0		6.75	4.0		4.0	-
"1" Level	VIH	1								1
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$		5.0	3.5	contract or	3.5	2.75	SITRIN	3.5	HEN DIVISE	Vdc
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$		10	7.0	(3.4R) v	7.0	5.50	7	7.0	-	-
(V <sub>O</sub> = 1 5 or 13.5 Vdc)	997	15	11.0	-	11.0	8.25	(test)	11.0	_	
Output Drive Current (AL Device)	ЮН								-	mAdc
(V <sub>OH</sub> = 2 5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	-1.7	peril Lastin	DEMO
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	in-2-25 +	-0.36	35.1	1.17
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	5 202ss	-0.9	00.01 - 1	177
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	_	-3.4	-8.8	HE_00 +	-2.4	03/0) - 7	1177
(VOI = 0.4 Vdc) Sink	IOL	50	0.64	-	0.51	0.88	-	0.36	Fatt Zitne	mAdo
(V <sub>OI</sub> = 0.5 Vdc)	ma	10	1.6	-	1.3	2.25	F 2025 THE	0.9	86.11 * 3	HT.
(VOL = 1.5 Vdc)	01	15	4.2	-	3.4	8.8	an_05 =	2.4	-00.01	P. A.S.
Output Drive Current (CL/CP Device)	ГОН		+	-			111 H.A. 1	No Chica	-	mAdo
(VOH = 2.5 Vdc) Source	HO	5.0	-2.5	_	-2.1	-4.2	_	-1.7	onleQ on h	(MODE)
(V <sub>OH</sub> = 4.6 Vdc)	0.8	5.0	-0.52		-0.44	-0.88	an GET 1	-0.36	100.00	200
(V <sub>OH</sub> = 9.5 Vdc)	62	10	-1.3		-1.1	-2.25	80 Ed 4	-0.9	36.01 -	1.192
(V <sub>OH</sub> = 13.5 Vdc)	18	15	-3.6		-3.0	-8.8	201 (4)	-2.4	- ( <u>0</u> .25.)	391
1. OH				-	0.44	-	90 981	0.36	FUSUV **	mAdd
(VOL = 0.4 Vdc) Sink (VOL = 0.5 Vdc)	IOL	5.0	0.52	1	1.1	0.88	on V2	0.36	02.0)	made
OL	87	10	1.3	-	3.0	8.8	47 ns.	2.4	- 0.26 -	Aug!
1.05		15	3.6	-				-		-
Input Current (Al. Device)	lin	15	-	± 0.1	-	±0 00001	±01	- 17.00	± 1.0	μAdc
Input Current (CL/CP Device)	1 <sub>in</sub>	15	-	± 0.3	-	+0.00001	± 0.3		± 1.0	μAdo
Input Capacitance	Cin			-	-	5.0	7.5	-	-	pF
$(V_{10} = 0)$	9.8	100						districtive on	Sulf terror	Same,
Quiescent Current (AL Device)	Ipp	50	-	1.0	-	0.002	1.0	-	30	μAdo
(Per Package)	.00	10		2.0		0.004	2.0	siosath.	60	Connet I
10 303 01	0.0	15	-	4.0	-	0.006	4.0	S STOREGY	120	Charlett's
Quiescent Current (CL/CP Device)	Inc	5.0	-	4.0	-	0.002	4.0	-	30	μAdo
(Per Package)	1DD	10	-	8.0		0.002	8.0	_	60	μΑσο
i ei i dekagei	-81	15		16		0.004	16		120	
Total Supply Current**†	1-	5.0	+	1 10			-		120	1 4
	IT		1			).58 µA/kHz				μAdd
(Dynamic plus Quiescent, Per Package)		10	1			.15 µA/kHz				M-1537, 1943 T
(CL = 50 pF on all outputs, all outputs		15	1 3 3 3 7		11 = (	.73 μA/kHz	1) f + 1D	D		
switching)					et list man	samp about	ser sentill	d bi lon si	dia pani	
Three-State Output Leakage Current	ITL	15	-	±0.1	- Takena	±0.0001	±0.1	in the British	±3.0	μAdd
(AL Device)										1
Three-State Output Leakage Current	ITL	15	1000	±1.0	_	±0.0001	±1.0	T -	±7.5	μAdo
(CL/CP Device)			1			1	14091313			

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

"The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: IT is in  $\mu A$  (per package), CL in pF, V = (VDD – VSS) in volts, f in kHz is input frequency, and k = 0.004.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin, lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

#### SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

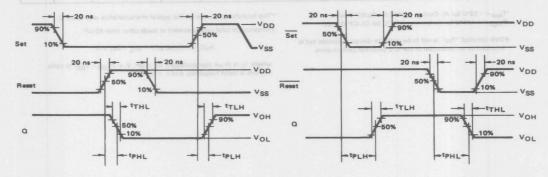
Charac	teristic				Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise Time	5,8-	D.S- 1		9.5-	tTLH		95%	9 5 11	BAS 24	ns
tTLH = (1.35 ns/pF) CL + 32.5 ns					0.8	5.0	-	100	200	KO VO
tTLH = (0.60 ns/pF) CL + 20 ns					01	10	-	50	100	HOA!
tTLH = (0.40 ns/pF) CL + 20 ns					37	15	-	40	80	HOVI
Output Fall Time	88.0	and to 1		1450	THL	101	1 1 1	ia f	20 Y 30 P	ns
tTHL = (1.35 ns/pF) CL + 32.5 ns					DE	5.0	-	100	200	30 VI
tTHL = (0.60 ns/pF) CL + 20 ns					0 1	10	-	50	100	100
tTHL = (0.40 ns/pF) CL + 20 ns						15	19th vall	40	80	1000
Propagation Delay Time	0.5	1.5-		2.5	tPLH		2000	18.	OVER	ns
tpLH = (0.90 ns/pF) CL + 130 ns					08-1	5.0	-	175	350	HOVE
tpLH = (0.36 ns/pF) CL + 57 ns					61	10	-	75	175	165/47
tpLH = (0.26 ns/pF) CL + 47 ns					av d	15	-	60	120	1000
tpHL = (0.90 ns/pF) CL + 130 ns					tPHL	5.0	- 4	175	350	ns
tpHL = (0.90 ns/pF) CL + 57 ns					tor a	10	-	75	175	10.93
tpHL = (0.26 ns/pF) CL + 47 ns					21	15	-	60	120	NOV
Set, Set Pulse Width	TENEN ST		1 1 1		tw	5.0	200	80	324 100	ns
						10	100	40	ALICE SHEET	102 mm
						15	70	30	0.000000	12 100
Reset, Reset Pulse Width					tw	5.0	200	80	- (6)	ns
						10	100	40	1000000	ment-in
						15	70	30	1 Townson	S 105)
Three-State Enable/Disable Delay	800.0		0.0		tPLZ,	5.0	-	150	300	ns
					tPHZ.	10	-1900	80	160	neares
					tPZL.	15		55	110	Fruit!
					tPZH	15		35	110	

\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

AC WAVEFORMS

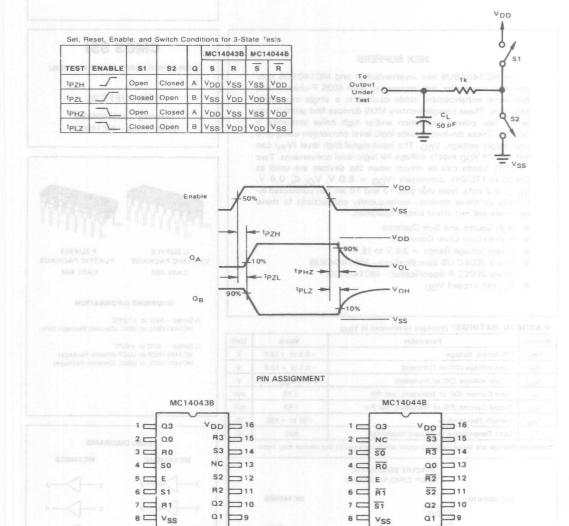




#### MC14043B•MC14044B

MC14049UB

# THREE-STATE ENABLE/DISABLE DELAYS



NC = No Connection

#### **HEX BUFFERS**

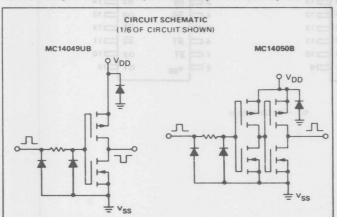
The MC14049UB hex inverter/buffer and MC14050B non-inverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, VpD. The input-signal high level (VIH) can exceed the VpD supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (VpD = 5.0 V, VoL  $\leqslant$  0.4 V, IoL  $\geqslant$  3.2 mA). Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- Meets JEDEC UB Specifications—MC14049UB Meets JEDEC B Specification—MC14050B
- V<sub>IN</sub> can exceed V<sub>DD</sub>

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin	Input Voltage (DC or Transient)	-0.5 to +18.0	٧
Vout	Output Voltage (DC or Transient)	0.5 to V <sub>DD</sub> +0.5	٧
lin	Input Current (DC or Transient), per Pin	±10	mA
lout	Output Current (DC or Transient), per Pin	+ 45	mA
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

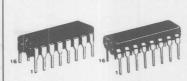


#### **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

#### HEX BUFFERS

Inverting - MC14049UB Noninverting - MC14050B



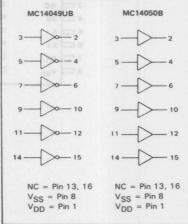
L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP or UBCP (Plastic Package) MC14XXXBCL or UBCL (Ceramic Package)

#### LOGIC DIAGRAMS



**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

					VDD	110	w*		25°C		l h	igh" .	
Cha	racterist	ic		Symbol	Vdc	Min	Max	Min	Тур #	Max	Min	Max	Unit
Output Voltage	Typ o	4105	"0" Level	VOL	5.0	-	0.05	- 1	0	0.05	- 1	0.05	Vdc
Vin = VDD or 0					10		0.05	-	0	0.05	-	0.05	
					15	-	0.05	_	0	0.05	-	0.05	10010
$V_{in} = 0 \text{ or } V_{DD}$			"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	or or the	Vdc
					10	9.95	-	9.95	10	in the s	9.95	19.0	11.173
100	-08		01		15	14.95	_	14.95	15	16. JE 4	14.95	o ( <del></del>	4071
Input Voltage MC140	49UB		"0" Level	VIL					179 1		7 (75) ad		Vdc
$(V_0 = 4.5 \text{ Vdc})$				neri I	5.0	-	1.0	-	2.25	1.0	-	1.0	Treats
$(V_0 = 9.0 \text{ Vdc})$					10	-	2.0	-	4.50	2.0	O They	2.0	BUTT
$(V_0 = 13.5 \text{ Vdc})$					15	-	2.5	-	6.75	2.5	0.1350	2.5	Lucyex
00			"1" Level	VIH							(D ( B o)		Vdc
(V <sub>O</sub> = 0.5 Vdc)				e sor 1	5.0	4.0	-	4.0	2.75	_	4.0	reduct T	
$(V_0 = 1.0 \text{ Vdc})$				- I	10	8.0	-	8.0	5.50	(18 v.)	8.0	(ske() r	10.00
(V <sub>O</sub> = 1.5 Vdc)	cis.		- No. 1		15	12.5	i	12.5	8.25	-	12.5	-	21.114
Input Voltage MC140	50B		"0" Level	VIL					(4)	3.85 +	3 (3eta)		Vdc
(V <sub>O</sub> = 0.5 Vdc)					5.0	-	1.5	-	2.25	1.5	-	1.5	1111
$(V_O = 1.0 \text{ Vdc})$				THAI	10	-	3.0	-	4.50	3.0	21-22-1	3.0	SERetro
$(V_0 = 1.5 \text{ Vdc})$					15	-	4.0	_	6.75	4.0	D (29/m)	4.0	Jimes I
			"1" Level	VIH							the Laborator		Vdc
$(V_0 = 4.5 \text{ Vdc})$					5.0	3.5	-	3.5	2.75		3.5		THAN
$(V_O = 9.0 \text{ Vdc})$				1 2 1	10	7.0	-	7.0	5.50	-	7.0	- 14	SERVICE D
$(V_0 = 13.5 \text{ Vdc})$				Land I	15	11	-	11	8.25	_	11	-	
Output Drive Current (	AL Devi	ce)	0.8	ІОН						an Etit o	O STORY	n V (3)	mAde
(VOH = 2.5 Vdc)			Source		5.0	-1.6	-	-1.25	-2.5	er Bare. Des To	-0.9	30 F	1171
$(V_{OH} = 9.5 \text{ Vdc})$				1	10	-1.6	-	-1.3	-2.6	100	-0.9	A C 5	8371
(VOH = 13.5 Vdc)					15	-4.7	-	-3.75	-10	-	-2.7	-	
(VOL = 0.4 Vdc)			Sink	IOL	5.0	3.75	-	3.2	6.0	-	2.2	MAIN T THE	mAdd
(VOL = 0.5 Vdc)					10	10	-	8.0	16	area .	5,6	12 <u>(1</u> 1	DH4.
(VOL = 1.5 Vdc)	91		100		15	30	-	24	40	JE 3	17.0	80 01	(P. 77)
Output Drive Current (	CL/CP D	evice)		ІОН						2	CA AND IN	4000	mAde
(VOH = 2.5 Vdc)			Source	ILIKE	5.0	-1.5	-	-1.25	-2.5	-	-1.0	med CL was	Saldy services
$(V_{OH} = 9.5 \text{ Vdc})$					10	-1.5	-	-1.3	-2.6	UDE-1	-1.0	ES 0	HUP
(VOH = 13.5 Vdc)					15	-4.5	-	-3.75	-10	AREA S	-3.0	81.0	F1.1K
(VOL = 0.4 Vdc)			Sink	IOL	5.0	3.6	-	3.2	6.0	1,57	2.6	900.L	mAdd
$(V_{OL} = 0.5 \text{ Vdc})$				miet L	10	9.6	-	8.0	16	-	6.6	eln( <del>e</del> n)(s	nighae
(V <sub>OL</sub> = 1.5 Vdc)	68		6,0		15	28	-	24	40	01.05.1	19	y (C <del>-4</del> ) -	28/37
Input Current (AL Dev	ice)			lin	15	-	± 0.1	-	± 0.00001	± 0.1	10. (Ta)	± 1.0	μAdd
Input Current (CL/CP [	Device)			lin	15	-	±0.3	-	± 0.00001	± 0.3	11.00	± 1.0	μAdo
Input Capacitance				Cin	-	-	w village	ete <del>l</del> ara	10 .	20		-	pF.
(V <sub>in</sub> = 0)								- HONOLA	a section to a result	Desir NO	10000		1 541
Quiescent Current (AL	Device)			IDD	5.0	-	1.0	-	0.002	1.0	-	30	μAdd
(Per Package)				00	10	-	2.0	-	0.004	2.0	-	60	12 THE PROPERTY OF THE PARTY OF
					15	-	4.0	-	0.006	4.0	-	120	
Quiescent Current (CL/	CP Device	ce)		IDD	5.0		4.0		0.002	4.0		30	μAdd
(Per Package)	Held Co.	Mark of The Co		.00	10	1833 TES	8.0	W270A	0.004	8.0	TARREST A	60	
					15	_	16	-	0.006	16	-	120	
Total Supply Current * *	†			IT	5.0		-	IT = (1	8 μA/kHz)		-		μAdo
		r Package	)	, ,	10				5 μA/kHz)1				mr.oc
(Dynamic plus Quiescent, Per Package) (C <sub>1</sub> 50 pF on all outputs, all buffers switching)			8 3 18	15				3 μA/kHz)					

 $<sup>^{\</sup>circ}$ T<sub>low</sub> =  $-55^{\circ}$ C for AL Device,  $-40^{\circ}$ C for CL/CP Device. Thigh =  $+125^{\circ}$ C for AL Device,  $+85^{\circ}$ C for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.002.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

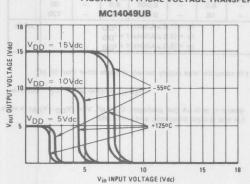
<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

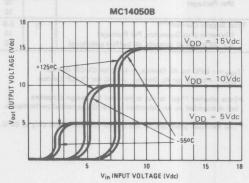
SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

								Lucality			
						DanyE.	VDD	34	shannan	2	
26V 800 - 200 C	haracteri	stic				Symbol	Vdc	Min	Тур #	Max	Unit
MC14049UB	0		0.08	100	at						N WHAT
Output Rise Time	0.8	4.05	1 -	69.5	1.0	TLH	99.3 "Y"			ony is	ns
tTLH = (0.8 ns/pF) C1 + 60 ns							5.0	-	100	160	
tTLH = (0.3 ns/pF) C1 + 35 ns							10	-	50	100	
tTLH = (0.27 ns/pF) CL + 26.5	ns					LV I	15	-	40	60	mov sug
Output Fall Time	25.5	100	7 0.1		9:0	THL				(5b) 6	ns
tTHL = (0.3 ns/pF) C1 + 25 ns							5.0	_	40	60	I'' OVI
tTHL = (0.12 ns/pF) C1 + 14 ns	. 27.5						10	_	20	40	FOVE
tTHL = (0.1 ns/pF) CL + 10 ns						let 4	15	-	15	30	
Propagation Delay Time	\$27 car	3 00		-0.6	1 0.5	tPLH				6×1057-15	ns
tpi H = (0.38 ns/pF) Ci + 61 ns	00.0					1.2	5.0	_	80	120	L'exi
tpl H = (0.20 ns/pF) C1 + 30 ns	03.5						10		40	65	Feyi
tpLH = (0.11 ns/pF) CL + 24.5	ns					74. 19	15	-	30	50	Wall tog
Propagation Delay Time	(50.3	17.	ns	1	101	tPHL				IKKO A	ns
tpHL = (0.38 ns/pF) CL + 11 ns	av n						5.0	-	30	60	1 × 650
tpHL = (0.12 ns/pF) CL + 9 ns							10	-	15	30	G.S.
tpHL = (0.11 ns/pF) CL + 4.5 n	is					HILL SIN	15	-	10	20	transfer and
MC14050B	Dê e	0.7		2.0	18.					fably 8.	8-691
Output Rise Time	45.0				1	tTLH				1009 03	ns
tTLH = (0.7 ns/pF) C1 + 65 ns						HOLY	5.0	_ (N)	100	160	mich zugen
tTLH = (0.25 ns/pF) CL + 37.5	ns					1	10	_	50	80	1110 97
tTLH = (0.2 ns/pF) C1 + 30 ns	0.2-						15	_	40	60	HGVI
Output Fall Time		1850	-	110	31	free	-		-	PAR 2 20	00
t <sub>THL</sub> = (0.2 ns/pF) C <sub>1</sub> + 30 ns						THL	5.0		40	60	ns
t <sub>THL</sub> = (0.06 ns/pF) C <sub>1</sub> +17 ns	107.4						10		20	40	1070
t <sub>THL</sub> = (0.04 ns/pF) C <sub>1</sub> + 13 n							15		15	30	= 40VI
Section 1	•	1		-		1	15	1	15	30	la man
Propagation Delay Time tp: H = (0.33 ns/pF) C: + 63.5	6.5					tPLH .	5.0		00	140	ns
tp[H = (0.33 ns/pF) C[ + 83.5 tp[H = (0.19 ns/pF) C] + 30.5							5.0	-	80	140	HOW
tp[H = (0.06 ns/pF) C[ + 30.5							10	-	1	80	HOW
	- 22	3.2	11/194	3.5	5.0	Jol 4	15	-	30	60	EL SONE
Propagation Delay Time						tPHL.				bby ED	ns
tpHL = (0.2 ns/pF) CL + 30 ns							5.0	-	40	80	TIOVI
tpHL = (0.1 ns/pF) CL + 15 ns						mit 1	10	-	20	40	mid awa
tpHL = (0.05 ns/pF) CL + 12.5	ns						15	-	15	30	THE REAL PROPERTY.

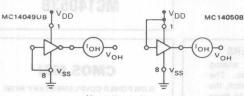
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

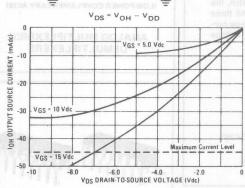
# FIGURE 1 - TYPICAL VOLTAGE TRANSFER CHARACTERISTICS Versus TEMPERATURE

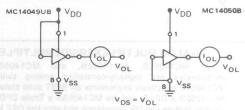




<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.







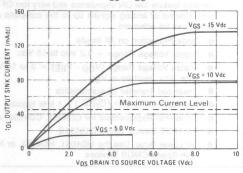


FIGURE 4 – AMBIENT TEMPERATURE

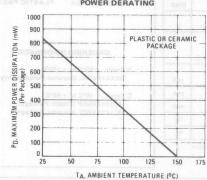
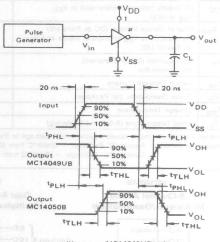


FIGURE 5 – SWITCHING TIME TEST CIRCUIT
AND WAVEFORMS



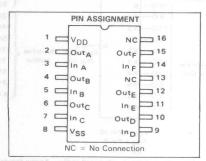
tect the inputs against damage due to high static voltages or electric fields **referenced to the Vss pin, only.** Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges Vss  $\leq$  Vin  $\leq$  18 V and Vss

This device contains circuitry to pro-

 V<sub>Out</sub> ≤ V<sub>DD</sub> are recommended.

 Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

#Invert on MC14049UB only



MC14052B MC14053B

#### ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally-controlled analog switches. The MC14051B effectively implements an SPBT solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (VDD VEE) = 3 to 18 V
   Note: VEE must be ≤ VSS
- Linearized Transfer Characteristics
- Low-Noise 12 nV/√Cycle, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch. See MC14551B
- For Lower RON, Use the HC4051, HC4052, or HC4053 High-Speed CMOS Devices

#### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage (Referenced to V <sub>EE</sub> , V <sub>SS</sub> ≥ VEE)	-0.5 to +18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient) (Referenced to V <sub>SS</sub> for Control Inputs and V <sub>EE</sub> for Switch I/O)	-0.5 to V <sub>DD</sub> +0.5	V
lin	Input Current (DC or Transient), per Control Pin	± 10	mA
Isw	Switch Through Current	± 25	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 55°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

#### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



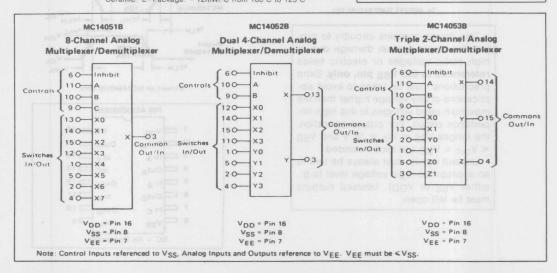
CASE 620
L SUFFIX
CERAMIC PACKAGE

P SUFFIX
PLASTIC PACKAGE

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



# MC14051B•MC14052B•MC14053B

The second second	303	CLIP'S		TI	ow*	-	25°C		Th	gh*	- 3
Characteristic	Symbol	VDD	Test Conditions	Min	Max	Min	Тур#	Max	Min	Max	Un
SUPPLY REQUIREMENT						()	etapel) o	mmit vis	and wis	tomam	q
Power Supply Voltage	T		V <sub>DD</sub> -3 ≥ V <sub>SS</sub> ≥ V <sub>EE</sub>	3	18	3	AND W	18	3	18	V
Range as as	V <sub>DD</sub>	2	VDD-3 = VSS = VEE	3	1.65 1	.013	ilan TLO	10	an int	10	Ľ
Quiescent Current Per	IDD	5	Control Inputs: Vin = VSS or VDD,	-	5	1219	0.005	5	1.55	150	μ/
Package (AL Device)		10	Switch I/O: VEE & VI/O & VDD,	- 1	10	lana	0.010	10	N +47	300	
607		15	and ∆V <sub>switch</sub> ≤ 500 mV**	_	20	_	0.015	20	6(2-1	600	
Quiescent Current Per	IDD	5	Control Inputs: Vin = VSS or VDD.	-	20	10710	0.005	20	MTG.	150	μ
Package (CL/CP Device)		10	Switch I/O: $V_{EE} \le V_{I/O} \le V_{DD}$ , and $\Delta V_{switch} \le 500 \text{ mV**}$	_	80	5710	0.010	40 80	01.ES	300 600	
Total Supply Current	ID(AV)	5	TA = 25°C only	- 68	3.61 +	10.13	(0.07 µA/	kHz)f +	lpp .		μ
(Dynamic Plus Quiescent,	5(11)	10	(The channel component,		- 1 5 Ту	pical	(0.20 µA/I				
Per Package)	11 1	15	(Vin - Vout)/Ron, is not			10.13	(0.36 µA/I	kHz)f +	IDD		
an			included.)	- 1	187 -	ssV.	00.01	(A) Togti	eChot I	etti oli	
CONTROL INPUTS — II	NHIBIT, A		100000000000000000000000000000000000000		35.4	costo	ent vigité es	1767 36	Market In	gradi	
Low-Level Input Voltage	V <sub>IL</sub> = 0	5	Ron = per spec,	-	1.5	- '	2.25	1.5	1000	1.5	1
	1	10	loff = per spec	-	3.0	-	4.50 6.75	3.0		3.0	
	- 0				4.0	_	-	4.0		4.0	-
High-Level Input Voltage	VIH	5	Ron = per spec,	3.5	-	3.5	2.75	- 80	3.5	-	1
	3	10	loff = per spec	7.0	_	7.0	5.50 8.25	-	7.0	-	
Annual State of Control of Control of Control	-			11.0	_	11.0	-		11.0		-
Input Leakage Current (AL Device)	lin	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	-	± 0.1	_	± 0.00001	± 0.1		± 1.0	μ
Input Leakage Current (CL/CP Device)	lin	15	$V_{in} = 0 \text{ or } V_{DD}$	3+-	± 0.3	4-01	± 0.00001	± 0.3	OFFICE BOBICS	±1.0	и
Input Capacitance	Cin	_		_	_	_	5.0	7.5	_		F
SWITCHES IN/OUT AND		NS OI	JT/IN - X, Y, Z (Voltages Refer	enced	to Vee						
		110 01		1	-		r	50	20013		L
Recommended Peak-to- Peak Voltage Into or	V <sub>1/O</sub>	_	Channel On or Off	0	VDD	0	_	VDD	0	VDD	V
Out of the Switch	0							3.0	869-10	0	
Recommended Static or	ΔV <sub>switch</sub>	-	Channel On	0	600	0	-	600	0	300	m
Dynamic Voltage Across					La co						
the Switch** (Figure 5)	6.1					W 5	. (20)(20)	teli oin	Marini S	MILIOE	
Output Offset Voltage	V00	_	Vin = 0 V, No load	-	_	-	10		-	3 -	μ
ON Resistance	Ron	5	ΔV <sub>switch</sub> ≤ 500 mV**,	-	800	_	250	1050	_	1300	5
(AL Device)		10	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control),	-	400	377 5	120	500	_	550	
		15	and Vin = 0 to VDD (Switch)	-	220	_	80	280	V-20	320	
ON Resistance	Ron	5	ΔV <sub>switch</sub> ≤ 500 mV**,	_	880	_	250	1050	_	1200	1
(CL/CP Device)		10	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control),	-	450	`	120	500		520	
- DE-	0:	15	and V <sub>in</sub> = 0 to V <sub>DD</sub> (Switch)	-(4	250	Hollin	80	280	1 1	300	
△ ON Resistance Between	ΔRon	5		_	70	1	25	70		135	2
Any Two Channels		10		_	50	-	10	50	-	95	
in the Same Package		15		_	45	_	10	45	(M) = A	65	
Off-Channel Leakage	loff	15	Vin = VIL or VIH (Control)	_	± 100	_	± 0.05	± 100	50-	± 1000	n
Current (AL Device) (Figure 10)	0.11		Channel to Channel or Any One Channel		Januar S		eyd) Sive .				
Off-Channel Leakage	loff	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control)	_	± 300		± 0.05	± 300		± 1000	n
Current (CL/CP Device) (Figure 10)	011		Channel to Channel or Any One Channel	60.0	ugiHy I		who Son is	igra toss	00.0	E VOICE	
Capacitance, Switch I/O	C				Sec. 1	of selled	251.0	18 JB	DA F	F (B)	-
THE PARTY OF THE P	C <sub>1/O</sub>		Inhibit = V <sub>DD</sub>		-	-	10	mi+	1,144,15	-	p
Capacitance, Common O/I	C <sub>O/I</sub>	-	Inhibit = V <sub>DD</sub> (MC14051B)	-	OI_HI		60	of each no	14 <u>2</u> - 4		p
			(MC14052B)	EDITALIES	print of		32		Daily		
			(MC14053B)				17	- Control of the Cont			$\perp$
Capacitance, Feedthrough	C1/O	-	Pins Not Adjacent	-	-		0.15	_		-	p
(Channel Off)	1	_	Pins Adjacent	1	0.5		0.47				1

<sup>\*</sup> T<sub>low</sub> = -55°C for AL Device, -40° for CL/CP Device.

T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device

<sup>#</sup> Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>For voltage drops across the switch ( $\Delta V_{switch}$ ) >600 mV (>300 mV at high temperature), excessive  $V_{DD}$  current may be drawn; i.e. the current out of the switch may contain both  $V_{DD}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

# 6

## MC14051B•MC14052B•MC14053B

ELECTRICAL CHARACTERISTICS\* ( $C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$ ) ( $V_{EE} \leq V_{SS}$  unless otherwise indicated)

Characteristic	Symbol	VDD-VEE	Typ #	Max	Unit
Propagation Delay Times (Figure 6)	tPLH, tPHL	Serokeli appuntovi	STREMES	MEGUN	ns
Switch Input to Switch Output (R <sub>L</sub> = 10 kΩ)					
MC14051	A SEA OF BEEN	1000	11/20/3	SIDEHOV SI	Midne to
tpLH, tpHL = (0.17 ns/pF) CL + 26.5 ns		5.0	35	90	990
tpLH, tpHL - (0.08 ns/pF) CL + 11 ns	e y shahil kranisti	10	15	40	i mada
tpLH, tpHL = (0.06 ns/pF) CL + 9.0 ns	r mingy Out dames	15	12	30	подвиз
MC14052	North all general Williams	181			ns
tpLH, tpHL = (0.17 ns/pF) CL + 21.5 ns	The state of the s	5.0	30	75	
tPLH, tPHL = (0.08 ns/pF) CL + 8.0 ns	Service Children	10	12	30	ancor
tPLH, tPHL = (0.06 ns/pF) CL + 7.0 ns		15	10	25	and the same
MC14053	Carlotte A. Carlotte		-		ns
tpLH, tpHL = (0.17 ns/pF) CL + 16.5 ns	Albert District of Wall	5.0	25	65	riggine.
tpLH, tpHL = (0.08 ns/pF) CL + 4.0 ns	gange learning effici	10	8.0	20	DIME
tpLH, tpHL = (0.06 ns/pF) CL + 3.0 ns	- na Petruny - seld	15	6.0	15	PROME
Inhibit to Output ( $R_L = 10 \text{ k}\Omega$ , $V_{EE} = V_{SS}$ )	tour tour				ns
Output "1" or "0" to High Impedance, or	tPHZ, tPLZ,	SIT, A. B. C	MU1 01	LESSEL AN	RIM
High Impedance to "1" or "0" Level	tPZH, tPZL		250	700	ious
MC14051B	Tomas and a second	5.0	350 170	700 340	
		10	140	280	
		15	-	-	-
MC14052B	. High min = ngR	5.0	300	600	ns
	Charles and a beat	10	155	310	
		15	125	250	-
MC14053B	and to 0 = aV	5.0	275	550	ns
		10	1.10	280	LOWS J
		15	110	220	
Control Input to Output (R <sub>L</sub> = 10 k $\Omega$ , V <sub>EE</sub> = V <sub>SS</sub> )	tPLH, tPHL	100	360	700	ns
MC14051B		5.0	160	720 320	10000
		10	120	240	HUAC I
type of the second of the seco	OF JE SHINE	and the second second	-		HOTE.
MC14052B		5.0	325	650	ns
	THE THE STATE SHOWING THE	10	90	250 180	THE PERSONS
					1000
MC14053B		5.0	300	600 240	ns
	no whosto:	10	120 80	160	nammo
				160	-
Second Harmonic Distortion $(R_L = 10K\Omega, f = 1kHz) V_{in} = 5 V_{PP}$		10	0.07	mug(H) he	%
	DIAL	10	17	- COLUMN TO	MH
Bandwidth (Figure 7)	BW	10	17	-	MH
$(R_L = 1 k\Omega, V_{in} = 1/2 (V_{DD} V_{EE}) p-p, C_L = 50pF$	D. V. S. V. S.	1 00			Line
$20 \text{ Log} \frac{\text{Vout}}{\text{Vin}} = -3 \text{ dB})$	V O O or and think	at the		1 13	1
vin			-		
	Manual Publishing	ng ngA		5.04	STEW DE
Off Channel Feedthrough Attenuation (Figure 7)		10	- 50	-	dB
R <sub>L</sub> = 1KΩ, V <sub>in</sub> = 1/2 (V <sub>DD</sub> - V <sub>EE</sub> ) p-p	1 2 2 2 2 2	- The same of the same of			
fin = 4.5 MHz — MC14051B		2090	And And And	anuo See	STREET ST
fin = 30 MHz — MC14052B		De	I To the last	diaminant	OWY W
fin = 55 MHz — MC14053B		62	1 1 1 1 1 1	PEXABIL BU	al sett
Channel Separation (Figure 8)	0 4 V 10 0 F 4 4 F	10	-50	opa <del>ta</del> du.	dB
$(R_L = 1 k\Omega, V_{in} = 1/2 (V_{DD} - V_{EE}) p-p,$	Complete of County			parveG x	1000
f <sub>in</sub> = 3.0 MHz	ANY CHIEF CARDOO			100	SHOW
Mint and a second secon					
	A STATE OF THE STA	100		LUMBER DE	
Crosstalk, Control Input to Common O/I (Figure 9)	and an analysis of	10	75	00 200	mV
$(R_1 = 1 k\Omega, R_L = 10 k\Omega)$	THE RESERVE THE PARTY OF THE PA			1	- Straige
Control t <sub>TLH</sub> = t <sub>THL</sub> = 20 ns, Inhibit = V <sub>SS</sub> )	The state of the s		1	A CONTRACTOR	1

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

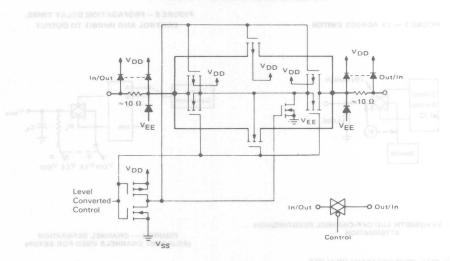
#Data labelled "Typ" is not to be used for design purposes but is
intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} = (V_{in} \text{ or } V_{out}) \le V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS, VEE, or VDD). Unused outputs must be left open.

# MC14051B•MC14052B•MC14053B

FIGURE 1 - SWITCH CIRCUIT SCHEMATIC



TRUTH TABLE

Contre	ol Ir	pu	ts	-							
	Select			ON Switches							
Inhibit	C*	В	A	MC14051B	MC140	052B	MC	1405	3B		
0	0	0	0	X0	YO	×ο	ZO	YO	XO		
0	0	0	1	X1	Y 1	×1	ZO	YO	X1		
0	0	1	0	X2	Y2	X2	ZO	Y1	X0		
0	0	1	1	X3	Y3	ХЗ	ZO	Y1	X1		
0	1	0	0	X4		1200	Z1	YO	XO		
0	1	0	1	X5			Z1	YO	X 1		
0	1	1	0	X6			Z1	Y1	XO		
0	1	1	1	X7		8	Z1	Y1	X 1		
1	×	×	×	None None No			None				

\*Not applicable for MC14052

FIGURE 3 - MC14052B FUNCTIONAL DIAGRAM

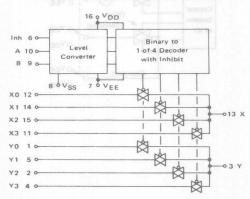


FIGURE 2 - MC14051B FUNCTIONAL DIAGRAM

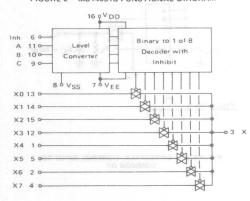
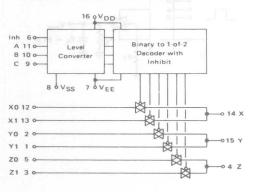


FIGURE 4 - MC14053B FUNCTIONAL DIAGRAM



x = Don't Care

FIGURE 5 - AV ACROSS SWITCH

FIGURE 6 - PROPAGATION DELAY TIMES,
CONTROL AND INHIBIT TO OUTPUT

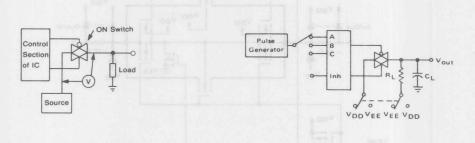


FIGURE 7 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

A, B, and C inputs used to turn ON or OFF the switch under test.

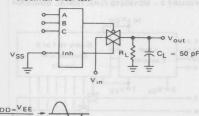


FIGURE 9 — CROSSTALK, CONTROL INPUT TO COMMON O/I

FIGURE 8 — CHANNEL SEPARATION (ADJACENT CHANNELS USED FOR SETUP)

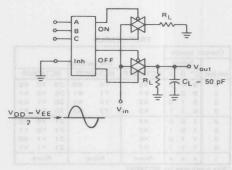
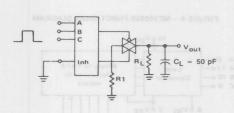
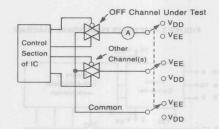


FIGURE 10 - OFF CHANNEL LEAKAGE

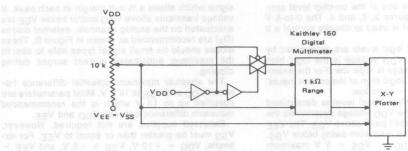


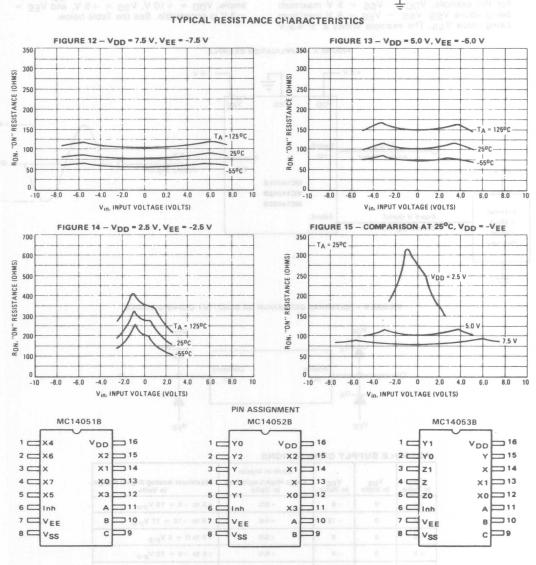


# 0

#### MC14051B•MC14052B•MC14053B

FIGURE 11 - CHANNEL RESISTANCE (RON) TEST CIRCUIT





#### MC14051B • MC14052B • MC14053B

#### APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figures 2, 3, and 4. The 0-to-5 V Digital Control signal is used to directly control a 9 Vp-p analog signal.

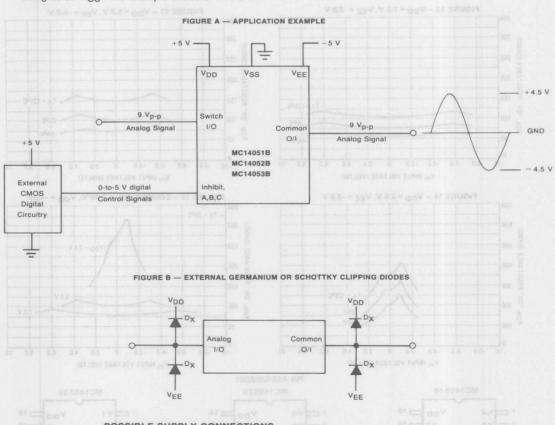
The digital control logic levels are determined by VDD and VSS. The VDD voltage is the logic high voltage; the VSS voltage is logic low. For the example, VDD = +5 V = logic high at the control inputs; VSS = GND = 0 V = logic low.

The maximum analog signal level is determined by VDD and VEE. The VDD voltage determines the maximum recommended peak above VSS. The VEE voltage determines the maximum swing below VSS. For the example,  $V_{DD}-V_{SS}=5\ V$  maximum swing above  $V_{SS}$ ;  $V_{SS}-V_{EE}=5\ V$  maximum swing below VSS. The example shows a ± 4.5 V

signal which allows a 1/2 volt margin at each peak. If voltage transients above VDD and/or below VEE are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between VDD and VEE is 18.0 V. Most parameters are specified up to 15 V which is the recommended maximum difference between VDD and VEE.

Balanced supplies are not required. However, Vss must be greater than or equal to VFF. For example,  $V_{DD} = +10 \text{ V}$ ,  $V_{SS} = +5 \text{ V}$ , and  $V_{EE} =$ -3 V is acceptable. See the Table below.



### POSSIBLE SUPPLY CONNECTIONS

V <sub>DD</sub> In Volts	V <sub>SS</sub> In Volts	V <sub>EE</sub> In Volts	Control Inputs  Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+8	0	-8	+ 8/0	$+8 \text{ to } -8 = 16 \text{ V}_{p-p}$
+ 5	0	- 12 01	+5/0	+5 to -12 = 17 V <sub>p-p</sub>
+ 5	0	0	+ 5/0	$+ 5 \text{ to } 0 = 5 \text{ V}_{p-p}$
+ 5	0	- 5	+ 5/0	$+5 \text{ to } -5 = 10 \text{ V}_{p-p}$
+10	+ 5	-5	+ 10/ + 5	+10 to -5 = 15 V <sub>p-p</sub>



# MC14060B

#### 14-BIT BINARY COUNTER AND OSCILLATOR

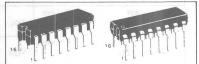
The MC14060B is a 14-stage binary ripple counter with an on-chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on Clock will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

- Fully static operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from Stages 4 Through 10 and 12 Through 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4060B

#### **CMOS MSI**

(LOW POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER AND OSCILLATOR



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

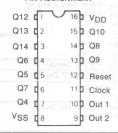
C Series: - 40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

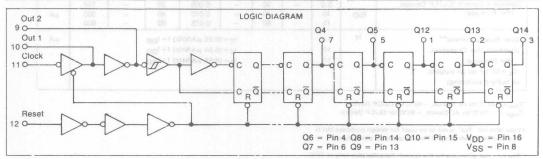
#### TRUTH TABLE

Clock	RESET	Output State
5	La	No Change
1	L	Advance to next state
×	н	All Outputs are low

X = Don't Care

#### PIN ASSIGNMENT





Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

rnis device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub>  $\leq$  (V<sub>in</sub> or V<sub>out</sub>)  $\leq$  V<sub>DD</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

		VDD	DD Tlow*			25°C		This	ah°	11-14
Characteristic	Symbol	V	Min	Max	Min	Typ#	Max	Min	Max	Unit
Output Voltage "O" Level Vin = VDD or 0	VOL	5.0 10 15		0.05 0.05 0.05	-	0 0	0.05 0.05 0.05	80a 00a	0.05 0.05 0.05	V
$V_{ID} = 0$ or $V_{DD}$	Voн	5.0 10 15	4.95 9.95 14.95	-	4.95 9.95 14.95	5.0 10 15	- els F o <u>E</u> V 0	4.95 9.95 14.95	no ±eto A s <u>⊊</u> etio	V
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 V) (V <sub>O</sub> = 9.0 or 1.0 V) (V <sub>O</sub> = 13.5 or 1.5 V)	VIL	5.0 10 15		1.5 3.0 4.0	U Norab Bangka Igh-ko a	2.25 4.50 6.75	1.5 3.0 4.0	d Uwer the control of	1.5 3.0 4.0	٧
(V <sub>O</sub> = 0.5 or 4.5 V) (V <sub>O</sub> = 1.0 or 9.0 V) (V <sub>O</sub> = 1.5 or 13.5 V)	VIH	5.0 10 15	3.5 7.0 11.0	-	3.5 7.0 11.0	2.75 5.50 8.25	en@co	3.5 7.0 11.0	J News R. I Space nit	V
Output Drive Current (AL Device)  (VOH = 2.5 V) (Except Source (VOH = 4.6 V) Pins 9 and 10)  (VOH = 9.5 V)  (VOH = 13.5 V)	loн	5.0 5.0 10	-3.0 -0.64 -1.6 -4.2	1 1 1	-2.4 -0.51 -1.3 -3.4	-4.2 -0.88 -2.25 -8.8		-1.7. -0.36 -0.9 -2.4	-	mA
(V <sub>OL</sub> = 0.4 V) Sink (V <sub>OL</sub> = 0.5 V) (V <sub>OL</sub> = 1.5 V)	lOL	5.0 10 15	0.64 1.6 4.2	-	0.51 1.3 3.4	0.88 2.25 8.8	-	0.36 0.9 2.4	_	mA
Output Drive Current (CL/CP Device) (VOH = 2.5 V) (Except Source (VOH = 4.6 V) Pins 9 and 10) (VOH = 9.5 V) (VOH = 13.5 V)	ЮН	5.0 5.0 10	-2.5 -0.52 -1.3 -3.6	-	-2.1 -0.44 -1.1 -3.0	-4.2 -0.88 -2.25 -8.8	r webst	- 1.7 - 0.36 - 0.9 - 2.4	=	mA
(V <sub>OL</sub> = 0.4 V) Sink (V <sub>OL</sub> = 0.5 V) (V <sub>OL</sub> = 1.5 V)	lOL	5.0 10 15	0.52 1.3 3.6	-	0.44 1.1 3.0	0.88 2.25 8.8	-	0.36 0.9 2.4		mA
Input Current (AL Device)	lin	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μΑ
Input Current (CL/CP Device)	lin	15	-	±0.3	dom to	±0.00001	±0.3	-	±1.0	μΑ
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	_ 901	1905_008	5.0	7.5	21	-	pF
Quiescent Current (AL Device) (Per Package)	lDD	5.0 10 15		5.0 10 20	-	0.005 0.010 0.015	5.0 10 20	-	150 300 600	μΑ
Quiescent Current (CL/CP Device) (Per Package)	IDD	5.0 10 15	- ATAJA;	20 40 80	103-	0.005 0.010 0.015	20 40 80	-	150 300 600	μА
Total Supply Current** (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	T O	5.0 10 15	0 0		I <sub>T</sub> =	(0.25 μA/kH: (0.54 μA/kH: (0.85 μA/kH:	z) f+IDD		H	μА

 $<sup>^{\</sup>circ}T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C1 = 50 pF, TA = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise Time (Counter Outputs)	<sup>†</sup> TLH	5.0 10 15	-	40 25 20	200 100 80	ns
Output Fall Time (Counter Outputs)	tTHL	5.0 10 15	no are	50 30 20	200 100 80	ns
Propagation Delay Time Clock to Q4	tPLH tPHL	5.0 10 15		415 175 125	740 300 200	ns
Clock to Q14  A RA YOMBUGBB ROTALIJSBO DR — # 3RUDIT	RO ROTALLE	5.0 10 15	1389YT 1881-2 801	1.5 0.7 0.4	2.7 1.3 1.0	μS
Clock Pulse Width	twH	5.0 10 15	100 40 30	65 30 20	-	ns
Clock Pulse Frequency	fφ	5.0 10 15	V AL-199V.	5 14 17	3.5 8 12	MHz
Clock Rise and Fall Time	tTLH tTHL	5.0 10 15		No Limit		ns
Reset Pulse Width	t <sub>W</sub>	5.0 10 15	120 60 40	40 15 10		ns
Propagation Delay Time Reset to Qn	tPHL .	5.0 10 15	1-1-1-100 F	170 80 60	360 160 100	ns

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the !C's potential performance.

FIGURE 1 — POWER DISSIPATION TEST CIRCUIT

AND WAVEFORM

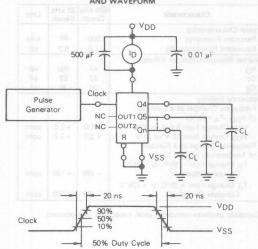
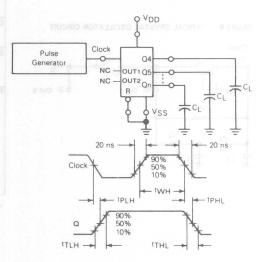
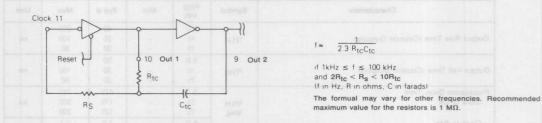


FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



# MC14060B

FIGURE 3 - OSCILLATOR CIRCUIT USING RC CONFIGURATION



#### TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 - RC OSCILLATOR STABILITY

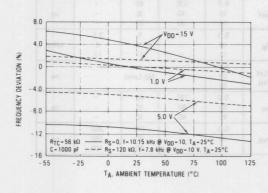


FIGURE 5 — RC OSCILLATOR FREQUENCY AS A FUNCTION OF RTC AND C

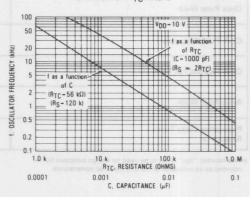


FIGURE 6 - TYPICAL CRYSTAL OSCILLATOR CIRCUIT

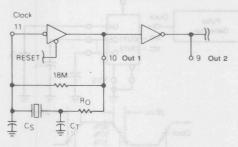


FIGURE 7 - TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

Characteristic	500 kHz Circuit	32 kHz Circuit	Unit	
Crystal Characteristics				
Resonant Frequency	500	32	kHz	
Equivalent Resistance, RS	1.0	6.2	kΩ	
External Resistor/Capacitor Values	P. MY			
RO	47	750	kΩ	
CT	82	82	pF	
CS	20	20	pF	
Frequency Stability	1000	- 4	photo:	
Frequency Changes as a Function	1-0-1	1993		
of VDD (TA = 25°C)	DIA -			
VDD Change from 5.0 V to 10 V	+60	+2.0	ppm	
VDD Change from 10 V to 15 V	+20	+ 2.0	ppm	
Frequency Change as a Function				
of Temperature (VDD = 10 V)	-			
TA Change from -55°C to +25°C				
Complete Oscillator*	+ 100	+ 120	ppm	
TA Change from + 25°C to + 125°C				
Complete Oscillator*	- 160	- 560	ppm	

<sup>\*</sup>Complete oscillator includes crystal, capacitors, and resistors



# MOTOROLA

MC14066B

#### **QUAD ANALOG SWITCH/QUAD MULTIPLEXER**

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

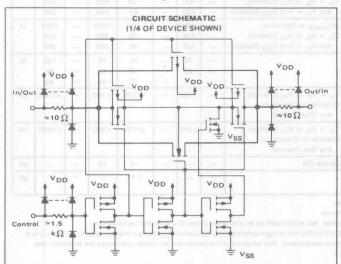
The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise 12 nV/√ Cycle, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016, CD4066, MC14016B
- For Lower RON, Use The HC4066 High-Speed CMOS Device

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In	Input Current (DC or Transient), per Control Pin	± 10	mA
Isw	Switch Through Current	± 25	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TI	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C



#### CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH



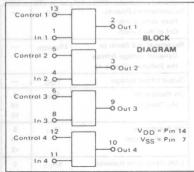


L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX PLASTIC PACKAGE CASE 646

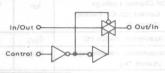
#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)







1	Control	Switch	Lo
1	0 = V <sub>SS</sub>	OFF	U JA
1	1 = V <sub>DD</sub>	ON	50%

Logic Diagram Restrictions

VSS ≤V<sub>in</sub> ≤V<sub>DD</sub>

VSS ≤V<sub>out</sub> ≤V<sub>DD</sub>

					T <sub>low</sub> *		25°C		Thigh*		
Characteristic	Symbol	VDD	Test Conditions	Min	Max	Min	Тур#	Max	Min	Max	Uni
SUPPLY REQUIREMEN	NTS (Voltage	s Refe	renced to V <sub>SS</sub> )								
Power Supply Voltage Range	V <sub>DD</sub>	-		3	18	3	-	18	3	18	٧
Quiescent Current Per Package (AL Device)	IDD	5 10 15	Control Inputs: $V_{in} = V_{SS}$ or $V_{DD}$ , Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$ , and $\Delta V_{switch} \le 500 \text{ mV**}$		0.25 0.50 1.00	121	0.005 0.010 0.015	0.25 0.50 1.00	CAN	7.5 15 30	μА
Quiescent Current Per Package (CL/CP Device)	1 <sub>DD</sub>	5 10 15	Control Inputs: $V_{in} = V_{SS}$ or $V_{DD}$ , Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$ , and $\Delta V_{switch} \le 500 \text{ mV**}$		1.0 2.0 4.0	g <del>-t</del> ur gmad	0.005 0.010 0.015	1.0 2.0 4.0	0 <del>10</del> 16 0 - 10	7.5 15 30	μА
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D</sub> (AV)	5 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>On</sub> , is not included.)	SOME	Ту		(0.07 μA/ (0.20 μA/ (0.36 μA/	kHz)f +	IDD	The life in the li	μА
CONTROL INPUTS (Vo	Itages Refere	nced to	V <sub>SS</sub> )			Stud	ni IIA no	noiros	in Prot	bold #	
Low-Level Input Voltage	VIL	5 10	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	7446	1.5	ip¥ 0	2.25 4.50	1.5	2 /L-4/8 26/27/0	1.5	٧
High-Level Input Voltage	VIH	15 5 10	R <sub>on</sub> = per spec, l <sub>off</sub> = per spec	3.5	4.0	3.5	6.75 2.75 5.50	4.0	3.5	4.0	V
	RONO	15	sowed 80M3 bas	11.0	M_Dat	11.0	8.25	NOR	11.0	10 <u>3</u> X	
Input Leakage Current (AL Device)	lin	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μA
Input Leakage Current (CL/CP Device)	lin	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	lagiv	±0.3	1,07530	± 0.00001	±0.3	UTAI	± 1.0	μA
Input Capacitance	Cin	_		-	-	-	5.0	7.5	-		pF
SWITCHES IN AND O	UT (Voltages	Refere	enced to VSS)		Arouts		or Party service			Daniel C	T
Recommended Peak-to- Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	mu 5	Channel On or Off	0	V <sub>DD</sub>	0	relation of the	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>p</sub> .
Recommended Static or Dynamic Voltage Across the Switch** (Figure 1)	ΔV <sub>switch</sub>	Cons	Channel On	0	600	0	encourie	600	0	300	m\
Output Offset Voltage	V00	-	V <sub>in</sub> = 0 V, No load	01-	10-10	id <del>-</del> h	10	ng. <del>mi</del> Orl	9-3	entr <del>al</del> m	μ\
ON Resistance (AL Device)	R <sub>on</sub>	5 10 15	$\Delta V_{switch} \le 500 \text{ mV**},$ $V_{in} = V_{IL} \text{ or } V_{IH} \text{ (Control)},$ and $V_{in} = 0 \text{ to } V_{DD} \text{ (Switch)}$	1 0 1	800 400 220	100	250 120 80	1050 500 280		1300 550 320	Ω
ON Resistance (CL/CP Device)	Ron	5 10 15	ΔV <sub>Switch</sub> ≤ 500 mV**, V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> = 0 to V <sub>DD</sub> (Switch)	UTTER 	880 450 250	1- 10- 10-	250 120 80	1050 500 280	-	1200 520 300	Ω
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5 10 15	, ouv	_	70 50 45	=	25 10 10	70 50 45	5	135 95 65	Ω
Off-Channel Leakage Current (AL Device) (Figure 6)	loff	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	J	± 100	-	± 0.05	± 100	-	±1000	n.A
Off-Channel Leakage Current (CL/CP Device) (Figure 6)	loff	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	I.	± 300	-	± 0.05	± 300	-	± 1000	n.A
Capacitance, Switch I/O	C <sub>1/O</sub>	_	Switch Off	_	_	_	10	15			pf
	110										Pi

<sup>\*</sup> Tlow = -55°C for AL Device, -40° for CL/CP Device.

Capacitance, Feedthrough

(Switch Off)

C1/0

0.47

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

<sup>#</sup> Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>For voltage drops across the switch ( $\Delta V_{switch}$ ) >600 mV (>300 mV at high temperature), excessive  $V_{DD}$  current may be drawn; i.e. the current out of the switch may contain both  $V_{DD}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

#### MC14066B

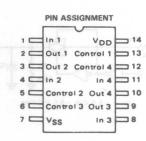
ELECTRICAL CHARACTERISTICS\* (C1 = 50 pF, TA = 25°C unless otherwise noted.)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Propagation Delay Times $V_{SS} = 0 \text{ Vdc}$ Input to Output $(R_L = 10 \text{ k}\Omega)$	tplH, tpHL	98	nwe seos	10.0 VA	380,00	ns
<sup>t</sup> PLH, tpHL = (0.17 ns/pF) C <sub>L</sub> + 15.5 ns	1 211 1112	5.0	l -	20	40	
<sup>t</sup> PLH, tpHI = (0.08 ns/pF) C <sub>I</sub> + 6.0 ns		10	_	10	20	
<sup>t</sup> PLH, tpHI = (0.06 ns/pF) C <sub>I</sub> + 4.0 ns		15	Lio 1	7.0	15	
Control to Output ( $R_L = 1 \text{ k}\Omega$ ) (Figure 2)			1000			
Output "1" to High Impedance	tPHZ	5.0	_	40	80	ns
		10	-	35	70	100
		15	-	30	60	
Output "0" to High Impedance	tPLZ	5.0		40	80	ns
	1	10	1 4	35	70	
		15	4 ( <u>v</u> )-	30	60	
High Impedance to Output "1"	tpzH	5.0	_	60	120	ns
a let a la	TZn	10	_	20	40	
		15	_	15	30	
High Impedance to Output "0"	tPZL	5.0		60	120	ns
	1721	10	_	20	40	
		15	A HOTOLOGIC	15	30	
Second Harmonic Distortion V <sub>SS</sub> = -5 Vdc	_	5.0	TAUMETT	0.1	G133	%
(Vin = 1.77 Vdc, RMS Centered @ 0.0 Vdc,						
$R_L = 10 \text{ k}\Omega$ , $f = 1.0 \text{ kHz}$ )				part mass	North Stendar	
Bandwidth (Switch ON) (Figure 3) V <sub>SS</sub> = -5 Vdc	_	5.0	_	65	-	MHz
					200	
V V V				language and	L	
$(R_L = 1 \text{ k}\Omega, 20 \text{ Log} \frac{V_{\text{out}}}{V_{\text{in}}} = -3 \text{ dB}, C_L = 50 \text{ pF}, V_{\text{in}} = 5 \text{ V}_{\text{p-p}})$			1 -		1	
Feedthrough Attenuation (Switch OFF) V <sub>SS</sub> = -5 Vdc	_ ruo N	5.0	1-8	-50		dB
$(V_{in} = 5 V_{p-p}, R_L = 1 k\Omega, f_{in} = 1.0 MHz)$ (Figure 3)		0.0	1	33		45
Channel Separation (Figure 4) VSS = -5 Vdc	_	5.0	8- 6-	- 50		dB
$(V_{in} = 5 V_{p-p}, R_L = 1 k\Omega, f_{in} = 8.0 \text{ MHz})$ (Switch A ON, Switch B OFF)					0 0	
Crosstalk, Control Input to Signal Output (Figure 5)					Sty dea	
V <sub>SS</sub> = -5 Vdc	-	5.0	_	300	-	mV <sub>p-l</sub>
$(R_1 = 1 k\Omega, R_L = 10 k\Omega, Control t_{TLH} = t_{THL} = 20 ns)$					1 1	

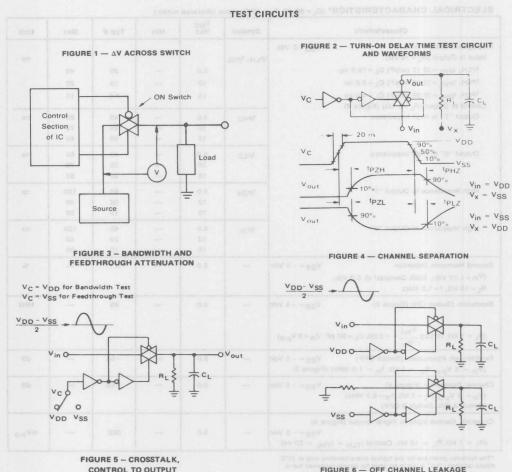
\*The formulas given are for the typical characteristics only at 25°C. #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

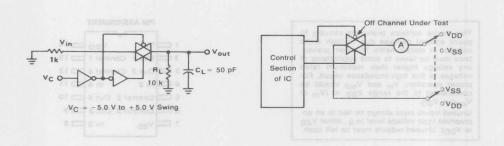


#### MC14066B



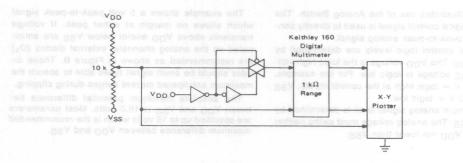
CONTROL TO OUTPUT

FIGURE 6 - OFF CHANNEL LEAKAGE

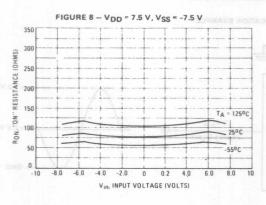


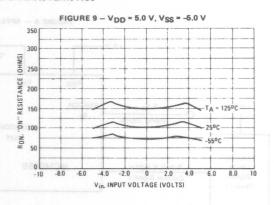
#### MC14066B

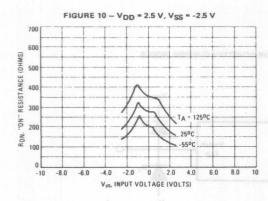
FIGURE 7 - CHANNEL RESISTANCE (RON) TEST CIRCUIT



#### TYPICAL RESISTANCE CHARACTERISTICS







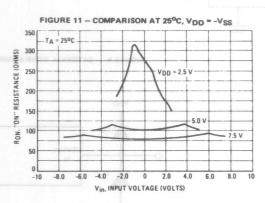


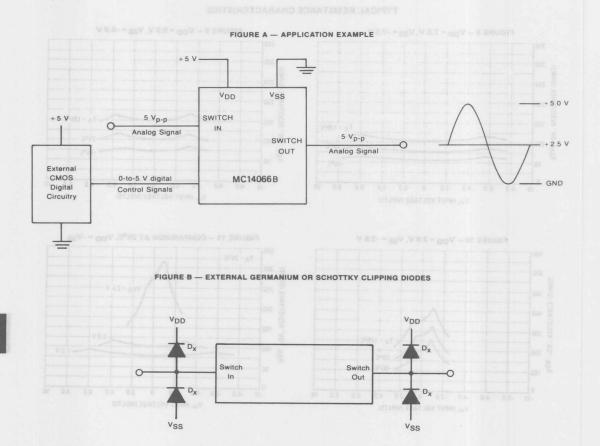
Figure A illustrates use of the Analog Switch. The 0-to-5 volt digital control signal is used to directly control a 5 volt peak-to-peak analog signal.

The digital control logic levels are determined by  $V_{DD}$  and  $V_{SS}$ . The  $V_{DD}$  voltage is the logic high voltage; the  $V_{SS}$  voltage is logic low. For the example,  $V_{DD} = +5 \text{ V} = \text{logic high at the control inputs; } V_{SS} = \text{GND} = 0 \text{ V} = \text{logic low.}$ 

The maximum analog signal level is determined by VDD and VSS. The analog voltage must swing neither higher than VDD nor lower than VSS.

The example shows a 5 volt peak-to-peak signal which allows no margin at either peak. If voltage transients above  $V_{DD}$  and/or below  $V_{SS}$  are anticipated on the analog channels, external diodes  $(D_X)$  are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between VDD and VSS is 18.0 volts. Most parameters are specified up to 15 volts which is the recommended maximum difference between VDD and VSS.





## ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14067 and MC14097 multiplexers/demultiplexers are digitally controlled analog switches featuring low ON resistance and very low leakage current. These devices can be used in either digital or analog applications.

The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1-of-16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

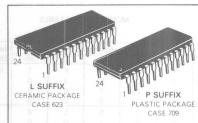
The MC14097 is a differential 8-channel multiplexer/demultiplexer with an inhibit and three binary control inputs A, B, and C. These control inputs select 1 of 8 pairs of channels by turning ON the appropriate analog switches (see MC14097 truth table).

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B and CD4097B

# **CMOS**

(LOW-POWER COMPLEMENTARY MOS)

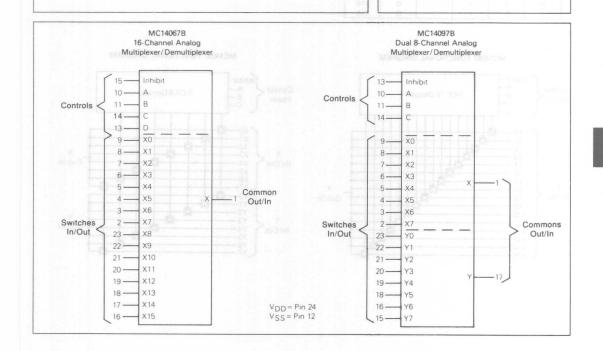
## ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



## ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin	Input Current (DC or Transient), per Control Pin	± 10	mA
Isw	Switch Through Current	± 25	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

### MC14067 TRUTH TABLE

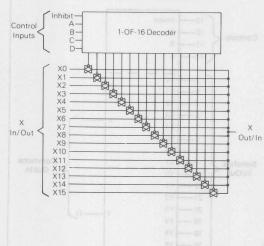
	Co	ntrol Inpu	ıts		Selected
Α	В	С	D	Inh	Channel
×	X	X	X	. 1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	tea Le	0	0	0	X2
1	1	0	0	0	X3
0	0	- 1	0	0	X4
1	NO O	OHIN OU	0	0	X5
0	1	1	0	0	X6
1 /4	Possilius Con	1	0	0	X7
0	0	0	1	0	X8
1	0 09	0 00	1 Intrad	0	X9
0	(0.]80(0.0)	01-01-19	per 1x in	0	X10
1	10 paper	0	CHECK PARKS	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

## MC14097 TRUTH TABLE

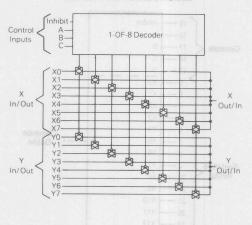
	Control	Inputs		Selected
Α	В	C	Inh	Channels
X	×	X	1	None
0	0	0	0	X0 Y0
1	0	0	0	X1 Y1
0	1	0	0	X2 Y2
1	1 (90	0	0	X3 Y3
0	0	den testo	0	X4 Y4
1	0		0	X5 Y5
0	1	1	0	X6 Y6
1	1	1	0	X7 Y7

X = Don't Care

### MC14067 FUNCTIONAL DIAGRAM



### MC14097 FUNCTIONAL DIAGRAM



FIECTD	CAL	CHAD	ACTED	POLICE

	N. a	4 1	table Indexed		ow"	private	25°C			igh"	
Characteristic			Min	Max	Min	Typ#	Max	Min	Max	Un	
SUPPLY REQUIREMEN	NTS (Voltag	es Refe	renced to VSS)								
Power Supply Voltage Range	V <sub>DD</sub>	-	1Figure 3) 5.0	3	18	3	-	18	3	18	V
Quiescent Current Per Package (AL Device)	I <sub>DD</sub>	5 10 15	Control Inputs: $V_{in} = V_{SS}$ or $V_{DD}$ , Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$ ,	_	5 10 20	_	0.005 0.010 0.015	5 10	O COBA	150 300 600	μ.
Quiescent Current Per Package (CL/CP Device)	loo T	5 10 15	and ΔV <sub>Switch</sub> ≤ 500 mV**  Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> ,  Switch I/O: V <sub>EE</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> ,  and ΔV <sub>Switch</sub> ≤ 500 mV**	_	20 40 80	tu <del>ur</del> uk	0.005 0.010 0.015	20 40 80	lorand	150 300 600	д
Total Supply Current (Dynamic Plus Quiescent, Per Package)	ID(AV)	5 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>In</sub> -V <sub>out</sub> )/R <sub>on</sub> , is not included.)			pical	(0.07 μΑ/) (0.20 μΑ/) (0.36 μΑ/)	(Hz)f +	IDD	000	μ.
CONTROL INPUTS -	INHIBIT,	A, B,	C, D (Voltages Referenced to VS	S)							
Low-Level Input Voltage	VIL	5 10 15	R <sub>On</sub> = per spec, l <sub>off</sub> = per spec	_	1.5 3.0 4.0	© or s	2.25 4.50 6.75	1 5 3.0 4.0	HS VA	1.5 3.0 4.0	V
High-Level Input Voltage	VIH as	5 10 15	R <sub>on</sub> = per spec, l <sub>off</sub> = per spec	3.5 7.0 11.0	- -	3.5 7.0 11.0	2.75 5.50 8.25		3.5 7.0 11.0	<del>-</del>	V
Input Leakage Current (AL Device)	lin 08	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	-	± 0.1	-	± 0.00001	± 0.1	-	± 1.0	μ
Input Leakage Current (CL/CP Device)	lin	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	-	± 0.3	in <u>ii</u> ni	± 0.00001	± 0.3	H tino:	± 1.0	μ
Input Capacitance	Cin			-	-	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	5.0	7.5	enner of	77	р
SWITCHES IN/OUT AN	D COMM	ONS C	OUT/IN - X, Y (Voltages Refere	nced 1	o Ves	ev-la	(V) EVI -	W. Dist	F - 3	1	
Recommended Peak-to- Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>		Channel On or Off	0	V <sub>DD</sub>	0	Ant-	V <sub>DD</sub>	(20 0 to	V <sub>DD</sub>	Vp
Recommended Static or Dynamic Voltage Across the Switch** (Figure 1)	ΔV <sub>switch</sub>		Channel On (6 Aug 4)	0	600	0.9	JVI 3-1 -	600	0	300	m
Output Offset Voltage	V00		Vin = 0 V, No load	(Hitter)	_	N-20	10	N-to	haran.		μ
ON Resistance (AL Device)	Ron	5 10 15	$\Delta V_{Switch} \le 500 \text{ mV**},$ $V_{in} = V_{IL} \text{ or } V_{IH} \text{ (Control)},$ and $V_{in} = 0 \text{ to } V_{DD} \text{ (Switch)}$	=	800 400 220	/ш/ (0 <del>25</del> 0)	250 120 80	1050 500 280	Gladens	1300 550 320	Ω
ON Resistance (CL/CP Device)	Ron	5 10 15	$ \Delta V_{\text{Switch}} \leq 500 \text{ mV**}, $ $ V_{\text{in}} = V_{\text{IL}} \text{ or } V_{\text{IH}} \text{ (Control)}, $ $ \text{and } V_{\text{in}} = 0 \text{ to } V_{\text{DD}} \text{ (Switch)} $	ntyleab	880 450 250	ar ed	250 120 80	1050 500 280	edor s	1200 520 300	Ω
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5 10 15		=	70 50 45	_	25 10 10	70 50 45	_	135 95 65	Ω
Off-Channel Leakage Current (AL Device) (Figure 2)	ioff	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	-	± 100	-	± 0.05	± 100	_	±1000	n
Off-Channel Leakage Current (CL/CP Device) (Figure 2)	loff	15	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	-	± 300	_	± 0.05	± 300		±1000	n
Capacitance, Switch I/O	C <sub>1/O</sub>	-	Inhibit = V <sub>DD</sub>	-	-	-	10	-	_	-	р
Capacitance, Common O/I	CO/I		Inhibit = V <sub>DD</sub> (MC14067B) (MC14097B)	-	-		100 60	_	_	-	р
	1										

<sup>\*</sup>  $T_{low} = -55$ °C for AL Device, -40° for CL/CP Device.

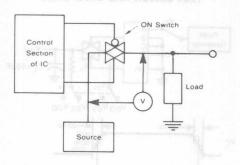
high = +125°C for AL Device, +85°C for CL/CP Device.

<sup>#</sup> Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>For voltage drops across the switch ( $\Delta V_{switch}$ ) >600 mV (>300 mV at high temperature), excessive  $V_{DD}$  current may be drawn; i.e. the current out of the switch may contain both  $V_{DD}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See second page of this data sheet.)

Characteristic	Symbol	V <sub>DD</sub> -V <sub>SS</sub>	Тур#	Max	Unit	
Propagation Delay Times Channel Input-to-Channel Output (R <sub>L</sub> = 200kΩ)	tPLH, tPHL	V of imposes of	an anganaka	STREME	ns	991
MC14067B				1		
	(Figure 3)	5.0	35	90	Office or a large	1
		10	15	40		1971
	O Fact of a World	15	12	30	and meaning	1
MC14097B	Yeard Virtin	Titl vitariouslift	se I		ns	60090
		5.0	25	65		
	VIII (2006 > 10)00 W	10	10	25		-
	The self they be	15	7	18	Cultant Per	1900
Control Input to Channel Output		District LC	04	100	ns	Charle
Control Input-to-Channel Output Channel Turn-On Time (R <sub>I</sub> = 10 k $\Omega$ )	tPZH, tPZL	No. of the last			115	
MC14067B/097B	(Figure 4)	Company of the Company				-
MC 14007B/097B	(Figure 4)	5.0	240	600	internal gi	Song
	tise compared led	10	115	290	smutt au Co	- Minu
	Acres de La Maria	15	75	190		100
Channel Turn-Off Time (R <sub>L</sub> =300 kΩ) MC14067B/097B	tPHZ, tPLZ	pietouron -			ns	
	(Figure 4)	5.0	250	625	LISTEL JOS	ENC
	1	10	120	300	-	
	LONGE	15	75	190	dostiny teans	Print.
Any Pair of Address Inputs to Output MC14067B	tpLH, tpHL	1943 - 1163	at the		ns	
es les les les les les les les les les l	750116	5.0	280	700	Cathely trained	1
		10	115	290	STATE OF THE OWNER, OWNER, OWNER, OWNER, OWNER, OWNER, OWNER, OWNER, OWNER, OWNER, OWNER, OWNER, OWNER, OWNER,	
	2000	15	85	215		
MC14097B					ns	
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	(Figure 10)	5.0	250	625	Tomatical Press	ded t
	(rigule 10)	10	100	250		A ST
		15	75	190		
Second Harmonic Distortion	CILITY CILITY				-	9507
(R <sub>L</sub> = 10 k $\Omega$ , f = 1 kHz, V <sub>in</sub> = 5 V <sub>p-p</sub> )		10	0.3		%	990
ON Channel Bandwidth	BW				MHz	801
$[R_L = 1 k\Omega, V_{in} = 1/2 (V_{DD} - V_{SS})_{D-p}(sine-wave)]$	angestov) V (J	CUTUM .		DOMATI	OWI BEN	TIN
		The state of the s		7		
$20 \text{ Log}_{10} \frac{\text{Vout}}{\text{Vin}} = -3 \text{ dB} \qquad \qquad \text{MC14067}$		10	15		ON NEIGHT BED	THE RE
Vin MC14097	В	10	25	-	10 0111 8021	W 86
Off Channel Feedthrough Attenuation	_	10	-40	-	dB	10.0
[R <sub>L</sub> = 1 k $\Omega$ , V <sub>in</sub> = 1/2 (V <sub>DD</sub> - V <sub>SS</sub> ) p-p(sine-wave)]		I Intervention		100	o press behi	Torra
f <sub>in</sub> = 20 MHz - MC14067E f <sub>in</sub> = 12 MHz - MC14097E	(Figure 5)			Mat	voltage Ace	SHEET
Channel Separation		10	-40		40	188
	1980) AC	10	-40		dB	O VI
[ $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{SS})_{p-p} (\text{sine-wave})$ ] $f_{in} = 20 \text{ MHz}$	(Figure 6)	100				
IIN - 20 MITZ	(Figure 6)	Lean and Park	8		9.50	a mor
Crosstalk, Control Inputs-to-Common O/I (R1 = 1kΩ, R <sub>L</sub> = 10 kΩ,	W VACORITION	10	30	-	mV	HING .
Control t <sub>f</sub> = t <sub>f</sub> = 20 ns, Inhibit = V <sub>SS</sub> )	(Figure 7)			-	-	

FIGURE 1 - AV ACROSS SWITCH



MC14067B PIN ASSIGNMENT

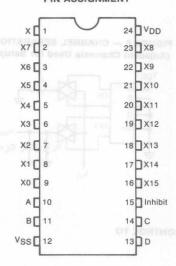
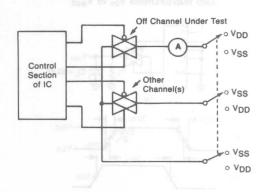


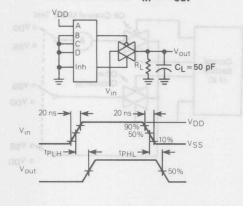
FIGURE 2 — OFF CHANNEL LEAKAGE



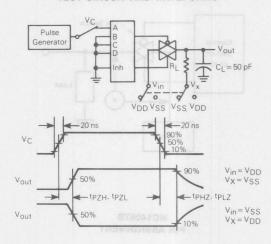
MC14097B PIN ASSIGNMENT



# FIGURE 3 — PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS Vin to Vout



# FIGURE 4 — TURN-ON AND DELAY TURN-OFF TEST CIRCUIT AND WAVEFORMS



# FIGURE 5 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

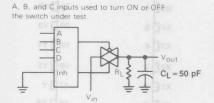


FIGURE 6 — CHANNEL SEPARATION (Adjacent Channels Used for Setup)

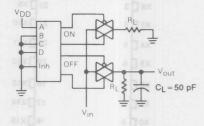


FIGURE 7 — CROSSTALK, CONTROL TO COMMON O/I

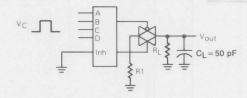
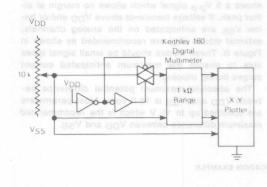
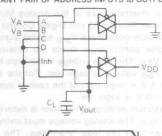
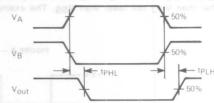


FIGURE 9 — CHANNEL RESISTANCE (RON) TEST CIRCUIT THE SHOULD FIGURE 10 — PROPAGATION DELAY,

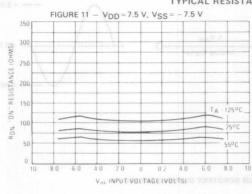


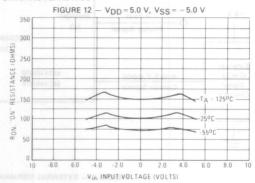
ANY PAIR OF ADDRESS INPUTS to OUTPUT

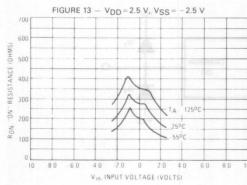




## TYPICAL RESISTANCE CHARACTERISTICS







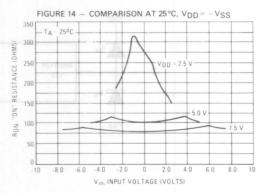


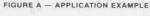
Figure A illustrates use of the Analog Multiplexer/ Demultiplexer. The 0-to-5 volt Digital Control signal is used to directly control a 5  $V_{D-D}$  analog signal.

The digital control logic levels are determined by  $V_{DD}$  and  $V_{SS}$ . The  $V_{DD}$  voltage is the logic high voltage; the  $V_{SS}$  voltage is logic low. For the example,  $V_{DD} = +5$  V = logic high at the control inputs;  $V_{SS} = GND = 0$  V = logic low.

The maximum analog signal level is determined by  $V_{DD}$  and  $V_{SS}$ . The analog voltage must swing neither higher than  $V_{DD}$  nor lower than  $V_{SS}$ . The example

shows a 5  $V_{p-p}$  signal which allows no margin at either peak. If voltage transients above  $V_{DD}$  and/or below  $V_{SS}$  are anticipated on the analog channels, external diodes  $(D_x)$  are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V<sub>DD</sub> and V<sub>SS</sub> is 18.0 volts. Most parameters are specified up to 15 V which is the recommended maximum difference between V<sub>DD</sub> and V<sub>SS</sub>.



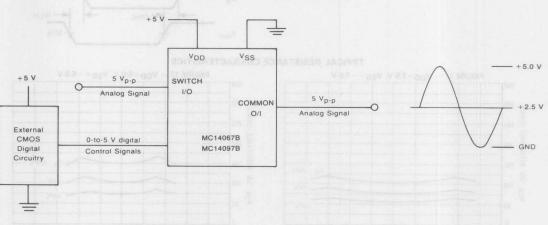
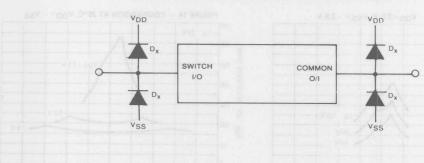
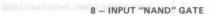


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES









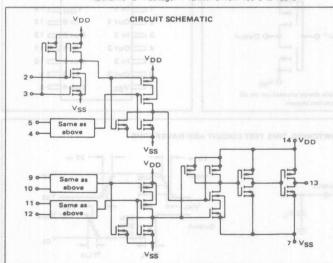
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

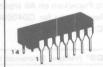
\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/"C from 50°C to 85°C Ceramic "L" Package: - 12mW/"C from 100°C to 125°C



## **CMOS SSI**

(LOW POWER COMPLEMENTARY MOS)
8-INPUT "NAND" GATE

FOR COMPLETE DATA SEE MC14001B





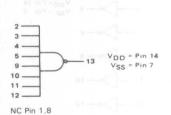
CERAMIC PACKAGE CASE 632 P SUFFIX PLASTIC PACKAGE CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### LOGIC DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



# MC14069UB

# CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

**HEX INVERTER** 

### HEX INVERTER

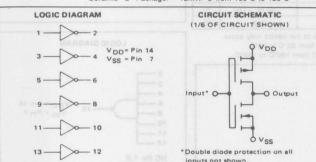
The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications

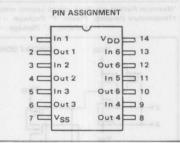
MAXIMUM RATINGS\* (Voltages Referenced to VSS)

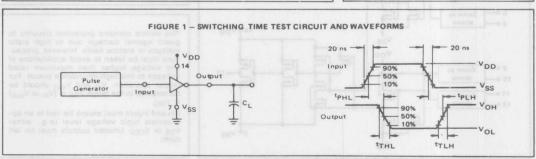
Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C









**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

		VDD	Tic	ow*		25°C		Thi	gh °	1
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
$V_{in} = V_{DD}$	0.	10	-	0.05	-	0	0.05	-	0.05	
D EXCLUSIVE "NOR" GATE	aug i	15	-	0.05		0	0.05	-	0.05	
"1" Level	Vон	5.0	4.95	_	4.95	5.0	_	4.95	10 mg = 17	Vdc
V <sub>in</sub> = 0	OH	10	9.95	BTAD	9.95	10	PEVE	9.95	DALKO	
		15	14.95	na maria	14.95	15		14.95		
nput Voltage "0" Level	VIL				511 -10					Vdc
(VO = 4.5 Vdc)	12	5.0	1000 1000	1.0	DM right	2.25	1.0	1000	1.0	DILLE .
(V <sub>O</sub> = 9.0 Vdc)	Hillian I	10	Dettillions	2.0	5 (6)	4.50	2.0	emeaner	2.0	Night.
(V <sub>O</sub> = 13.5 Vdc)		15	sen Ause	2.5	ester of	6.75	2.5	divida as	2.5	SMALE
"1" Level	VIH			10.71	1000	1000	TO BE THE OWNER.	9195 97 10	M 60 ft 10 ft 1	7201405
(V <sub>O</sub> = 0.5 Vdc)		5.0	4.0	11	4.0	2.75	0.0 - 0	4.0	to V_y/qq	Vdc
(V <sub>O</sub> = 1.0 Vdc)		10	8.0	_	8.0	5.50		8.0	surpuo 0	A D
(V <sub>O</sub> = 1.5 Vdc)		15	12.5	pn0 10	12.5	8.25	leng Low	12.5	to weep	10 e
Output Drive Current (AL Device)	ТОН		12.0	INSISH S	USE TRUIT	PI DOINE	SHI THYE	Deed A	T VEHICLE	mAd
(V <sub>OH</sub> = 2.5 Vdc) Source	HO	5.0	-3.0		-2.4	-4.2	NO DOUBLE	-1.7	900 with	0 0
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	senagh	-0.51	-0.88		-0.36	SOTTE -	100
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	AND AND MAKE	-1.3	-2.25	Midningut	-0.9	an sure to	100
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	_	-3.4	-8.8	d toposis	-2.4	EXTONE	W. W.
The state of the s	EA.		0.64		0.51	0.88		0.36		mAc
	IOL	5.0				2.25		0.36		
(V <sub>OL</sub> = 0.5 Vdc)		15	1.6		1.3	8.8	North Nie	2.4	NE FAMILIE	NURSELY.
(V <sub>OL</sub> = 1.5 Vdc)	60 11	.15	4.2	OJ -	3.4	0.0	SHIPS TO SE	2.4		1
Output Drive Current (CL/CP Device)	ОН	1 v 1	O. Store	180-				amedali		mAd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	-	-1.7	Addition A	14
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	/ of 2.0	-0.44	-0.88	10-1741 11	-0.36	SO SE-TURS	F Heny
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	ne CO in	-0.9	NO YOU THE	Figure 1
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4		
(VOL = 0.4 Vdc) Sink	OL	5.0	0.52	-	0.44	0.88	_	0.36		mAd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3	700	1.1	2.25		0.9	el spans	2 01
(V <sub>OL</sub> = 1.5 Vdc)	200	15	3.6	-	3.0	8.8	Serting (	2.4	greet Trans	
Input Current (AL Device)	lin	15	lugate yad	±0.1	or eas	± 0.00001	± 0.1	they book	± 1.0	μAdo
Input Current (CL/CP Device)	lin	15	01	±0.3	mera_DA	±0.00001	±0.3	Plastic	±1.0	μAdo
nput Capacitance	Cin	-	- United	EL 12.00	160 II 20 PM	50	7.5	PATE TO S	-	pF
(V <sub>10</sub> 0)	1-1	parline.	-	-		-				1
Quiescent Current (AL Device)	IDD	5.0	MATORIS	0.25	100000	0.0005	0.25	HEIME	7.5	μAdo
(Per Package)	טטי	10		0.50		0.0010	0.50	_	15	-
A		15		1.00	-	0.0015	1.00		30	
Quiescent Current (CL/CP Device)	1	5.0		1.0	-		1.0		7.5	
(Per Package)	IDD	10	-	2.0	300	0.0005	2.0		15	μAdd
(rer rackage)		15	18	4.0	1 1	0.0010	4.0		30	
T 10 10 T 10	1	THE PERSON		4.0	1 - 10			0	30	
Total Supply Current**†	IT	5.0	-			0.3 µA/kHz				μАс
(Dynamic plus Quiescent, Per Gate)		10	1	BURN CH		0.6 μA/kHz				- S
(C <sub>L</sub> = 50 pF)		15			17 - 11	0.9 µA/kHz	I T IDDI	0		
85 M3 + 00 V					T	T		四水	A	
Output Rise and Fall Times **	tTLH,				1 19			who I		ns
(C <sub>L</sub> = 50 pF)	tTHL					100	000			
TLH, THL = (1.35 ns/pF) CL + 33 ns		5.0	-	-	ylon	100	200	basulyn15	-	1 2 1
TLH, THL = (0.60 ns/pF) CL + 20 ns		10	-	-	1	50	100	-		-
TLH, THL = (0.40 ns/pF) CL + 20 ns		15	-	_		40	80		-	
Propagation Delay Times** (C <sub>L</sub> = 50 pF)	tPLH, tPHL	2,000,0	27 113 W ASSE	1316A 1316	Anto th	Calena Di		- 5 380	017	n
tpLH,tpHL = (0.90 ns/pF) CL + 20 ns		5.0	-		an de	65	125	-	-	1
tpLH,tpHL = (0.36 ns/pF) CL + 22 ns		10	_	11	-	40	75	407	-	1
tpLH.tpHL = (0.26 ns/pF) CL + 17 ns		15	The second second second	726-1	The state of the s	30	55			1

<sup>&</sup>quot;T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ V1k}$$

to the range  $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>&</sup>quot;The formulas given are for the typical characteristics only at 25°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.002.



## **CMOS SSI**

### QUAD EXCLUSIVE "OR" AND "NOR" GATES

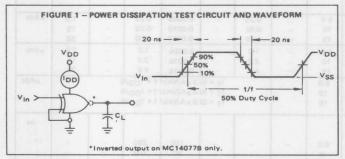
The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14070B Replacement for CD4030B and CD4070B Types
- MC14077B Replacement for CD4077B Type

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

"Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW"C from 55°C to 85°C Ceramic "L" Package: -12mW"C from 100°C to 125°C



# MC14070B

QUAD EXCLUSIVE "OR" GATE

# MC14077B

QUAD EXCLUSIVE "NOR" GATE





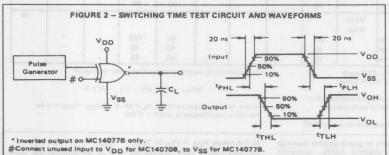
CASE 632
L SUFFIX
CERAMIC PACKAGE

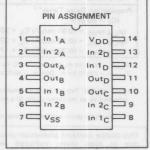
CASE 646
P SUFFIX
PLASTIC PACKAGE

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)





## MC14070B•MC14077B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tie	ow*		25°C		Thi	igh °	1
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	-	10		0.05		0	0.05		0.05	
		15	-	0.05	-	0	0.05	- 1	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95	-	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>		10	9.95	-	9.95	10	-	9.95		1000
		15	14.95	-	14.95	15	-	14.95	-	
Input Voltage "0" Level	VIL			223	AD Y	3 184	11-5 ()	UD		Vdc
(VO - 4.5 or 0.5 Vdc)		5.0	-	1.5		2.25	1.5	-	1.5	
(VO 9.0 or 1.0 Vdc)	Jan 1987	10	in Samuel	3.0	estato t	4.50	3.0	min-si S	3.0	Section
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	BILL IS	4.0	unolenio	6.75	4.0	on sion	4.0	Evah
"1" Level	VIH	61	Saummi	palon do	I selbri	nousbide	DOMNE G	nero ton	List Is v	1907
(VO - 0.5 or 4.5 Vdc)		5.0	3.5		3.5	2.75	-	3.5	00	Vdc
(VO: 1.0 or 9.0 Vdc)	Sign I	10	7.0	-	7.0	5.50	-	7.0	_	
(VO = 1 5 or 13.5 Vdc)		15	11.0		11.0	8.25	-	11.0		
Output Drive Current (AL Device)	ГОН				1907	F of old W	3.8 × 30	RFI SOST	oV visca	mAdc
(VOH - 2.5 Vdc) Source	·OH	5.0	-3.0		-2.4	-4.2		-1.7		
IV A C V/d-V	- 1	5.0	-0.64		-0.51	-0.88	_ 3	-0.36	diament 8	1
(V <sub>OH</sub> = 9.5 Vdc)	S. E. H.	10	-1.6	nO-10 e	-1.3	-2.25	TWO-LOW)	-0.9	e suisce	0.6
(V <sub>OH</sub> = 13.5 Vdc)	W 90 - 1	15	-4.2	ness au	-3.4	-8.8	ill =svO	-2.4	T Indiana is	
		5.0	0.64	1.12113.8116	0.51	0.88		0.36		mAdc
(VOL = 0.4 Vdc) Sink	OL		-		1.3	2.25	us Folta	0.36	O fildeb	MAGC
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6		3.4	The second second second second	Not lines	2.4	699-201-rs	2 4
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	THE PRINCE	2.4		
Output Drive Current (CL/CP Device)	ІОН									mAdc
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	100	-1.7	7.41	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 0 4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	H BATH	mAdc
(VOL = 0.5 Vdc)		10	1.3		1.1	2.25	adding.	0.9	HUD W	THE PARTY NA
(VOL = 1.5 Vdc)		15	3.6	- 1	3.0	8.8	Blomata!	2.4		10 Sett
Input Carrent (AL Device)	lin	15	11-15	±01	-	± 0.00001	±0.1	voiming!	±1.0	μAdc
Input Current (CL/CP Device)	lin	15	-	±03	-	±0 00001	± 0.3	-	±1.0	μAdc
Input Capacitance	Cin	-	-	-	-	5.0	7.5	uni Tuntu		pF
(V <sub>in</sub> = 0)	oin				150 360	THE REAL PROPERTY.		such tuning	D 18 beart	100 9
Quiescent Current (AL Device)	las	5.0	_ 1000	0.25	-	0.0005	0.25	- Harrier II	7.5	μAdc
(Per Package)	IDD	10	021 bit	0.50		0.0010	0.50		15	MAGC
(rei i ackage)	1 1 1	15	_	1.00		0.0015	1.00		30	200
0 0 10:100.0				-	-	0.0005		-	111111111111111111111111111111111111111	-
Quiescent Current (CL/CP Device)	IDD	5.0	poo (cm:	1.0	of again	M 2003 300 3 mil	1.0	ov ostiti	7.5	μAdc
(Per Package)		10	3784	2.0	108 July	0.0010	2.0	ministra in	15	uteneun
		15	1000	4.0	NOT W	0.0015	4.0	LOS BOLL	30	-
Total Supply Current**†	IT	5.0				$0.3  \mu A/kHz)$				μAdc
(Dynamic plus Quiescent,		10				0.6 µA/kHz)				
Per Package)	1, 101	15			1T = (	0.9 µA/kHz)	f + IDD			
(C <sub>L</sub> = 50 pF on all outputs, all	-									
buffers switching)	E1031						tank.			
Output Rise and Fall Times**	TLH.		00	10 41						ns
(C <sub>L</sub> = 50 pF)	THL						Thomas		The state of	1000
TLH, THL = (1.35 ns/pF) CL + 33 ns	Vris .	5.0	-	-	-	100	200	-	-	
TLH, THL = (0.60 ns/pF) CL + 20 ns	eliov - 1	10	- 1	-	-	50	100	-		2.5
TLH, THL = (0.40 ns/pF) CL + 20 ns	gold	15	-	-	Towns 61	40	80	-	-	
Propagation Delay Times**	TPLH.		orace	10 100						ns
(C <sub>L</sub> = 50 pF)	tPHL			Service .	-	I had				
tPLH. tPHL = (0.90 ns/pF) CL + 130 ns	tunus T.	5.0	_	LL.U	PER COL	175	350	1		
tPLH, tPHL = (0.36 ns/pF) CL + 57 ns	1	10	_			75	150			
<sup>t</sup> PLH, <sup>t</sup> PHL = (0.26 ns/pF) C <sub>L</sub> + 37 ns	1000	15		-		55	110	1		
	THE PARTY OF THE P			The state of		00	110			1

 $<sup>^{\</sup>star}T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \le (V_{in} \text{ or } V_{Out}) \le V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

<sup>†</sup>To calculate total supply current at loads other than 50 pF

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = {V\_DD-V\_SS} in volts, f in kHz is input frequency, and k = 0.002.



# MC14071B

## QUAD 2-INPUT "OR" GATE

The MC14071B is constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). The primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4071B

## **CMOS SSI**

QUAD 2-INPUT "OR" GATE
FOR COMPLETE DATA
SEE MC14001B





CERAMIC PACKAGE CASE 632 P SUFFIX
PLASTIC PACKAGE
CASE 646

### ORDERING INFORMATION

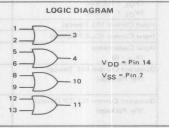
A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

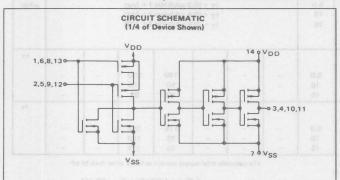
C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter 8.8	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW"C from 55°C to 85°C Ceramic "L" Package: -12mW"C from 100°C to 125°C





This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



### **DUAL 4 INPUT "OR" GATE**

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

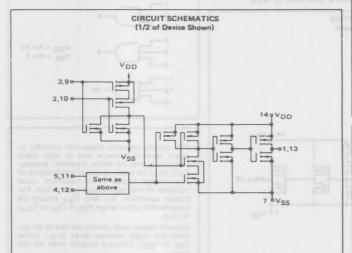
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4072B

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin, lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

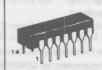
Ceramic "L" Package: -12mW/°C from 100°C to 125°C



## **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)
DUAL 4-INPUT "OR" GATE

FOR COMPLETE DATA SEE MC14001B





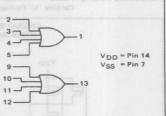
L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX PLASTIC PACKAGE CASE 646

## ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### LOGIC DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

# MC14073B



## TRIPLE 3-INPUT "AND" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

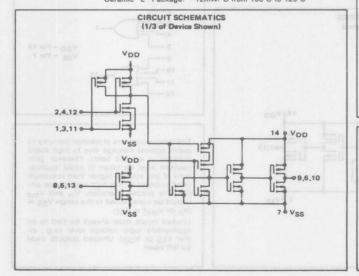
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4073B

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. Iout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C



## **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "AND" GATE

FOR COMPLETE DATA
SEE MC14001B



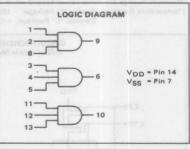


L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX PLASTIC PACKAGE CASE 646

### ORDERING INFORMATION

A Series: -55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.





## TRIPLE 3-INPUT "OR" GATE

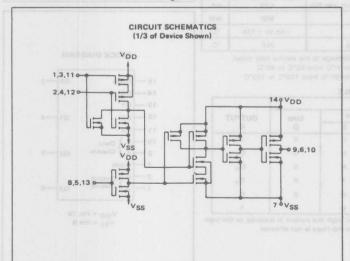
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4075B

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: – 12mW/"C from 55°C to 85°C Ceramic "L" Package: – 12mW/"C from 100°C to 125°C

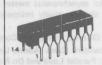


## **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "OR" GATE

FOR COMPLETE DATA
SEE MC14001B



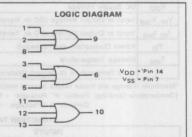


L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX PLASTIC PACKAGE CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

# MC14076B



## 4-BIT D-TYPE REGISTER with THREE-STATE OUTPUTS

The MC14076B 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated outputdisable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- Four Bus Buffer Registers
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range Schottky TTL Load Over the Rated Temper

### MAXIMUM RATINGS\* (Voltages Referenced to Voc)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

### **FUNCTION TABLE**

	1	NPUTS			
		Data Disable		Data	OUTPUT
Reset	Clock	A	В	D	Q
1	×	×	×	X	0
0	0	A X bas	×	×	an
0	5	1	×	×	Qn
0	5	×	1	×	an
0	5	0	0	0	0
0 0 0	above out a	0	0	40000	1

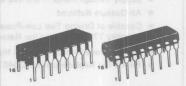
When either output disable A or B (or both) is (are) high the output is disabled to the highimpedance state; however sequential operation of the flip-flops is not affected.

X = Don't Care.

# **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

QUAD D-TYPE REGISTER with THREE STATE OUTPUTS



CERAMIC PACKAGE PLASTIC PACKAGE CASE 648

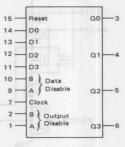
# CASE 620

ORDERING INFORMATION A Series: -55°C to +125°C MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: -40°C to +85°C

MC14XXXBCP or UBCP (Plastic Package) MC14XXXBCL or UBCL (Ceramic Package)

### **BLOCK DIAGRAM**



VDD = Pin 16 VSS = Pin 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

			VDD	Tic	w		25°C		Thi	gh	
Characterist	ic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Uni
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vde
V <sub>in</sub> = V <sub>DD</sub> or 0	5 052	111111	10	1	0.05	-	0	0.05	mita_	0.05	
00			15	1	0.05	-	0	0.05	ST IN D	0.05	luC
	"1" Level	VOH	5.0	4.95	-	4.95	5.0	# 10 B	4.95	JHP IN	Vde
Vin = 0 or VDD	02	TOH	10	9.95	_	9.95	10	13489m	9.95		
AIU - O OL ADD			15	14.95		14.95	15	RH8m	14.95		10
Input Voltage	"0" Level	VIL		750	10000		1				Vde
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		1.2	5.0	38	1.5	11-1	2.25	1.5	Out. Att	1.5	No.
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	666		10		3.0		4.50	3.0		3.0	
(V <sub>O</sub> = 13.5 or 1.5 Vdc			15		4.0	_	6.75	4.0	- 11	4.0	
110 1010 01110 101	"1" Level	VIH	31		7.0		20 30 -	O (Selan	EDI = TO		
(VO = 0.5 or 4.5 Vdc)		·In	5.0	3.5		3.5	2.75	W. V. ARIGH	3.5	STATES OF	Vdo
(VO = 1.0 or 9.0 Vdc)	300		10	7.0	_	7.0	5.50	O (⇔g\an	7.0	at all the	
(VO = 1.5 or 13.5 Vdc			15	11.0	_	11.0	8.25	nd to-bes d	11.0	01 -14-3197 01 -15T 100	
Output Drive Current (AL		Lavi	10 111	.11.0		11.0	0.23	Ch fillion	11.0	W 191 191	mAd
(VOH = 2.5 Vdc)	Source	ІОН	5.0	-3.0	and the same	-2.4	-4.2		-1.7		Acres 100
(V <sub>OH</sub> = 4.6 Vdc)			5.0	-0.64	TENS, SE	-0.51	-0.88	nutryO.	-0.36	special fills	18-6
(V <sub>OH</sub> = 9.5 Vdc)	80		10	-1.6		-1.3	-2.25		-0.9	great Total	1
	85		15	-4.2		-3.4	-8.8		-2.4		
(V <sub>OH</sub> = 13.5 Vdc)	_ por		-	-	an maga	-	200000000000000000000000000000000000000	THE PERSON .	-	2000 T 1 80	1100
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	OL	5.0	0.64	1074	0.51	0.88	-	0.36	7110	mAd
$(V_{OL} = 0.5 \text{ Vdc})$	69	4	10	1.6	7.11	1.3	2.25	-	0.9		
(V <sub>OL</sub> = 1.5 Vdc)			15	4.2		3.4	8.8	-	2.4		
Output Drive Current (CL	/CP Device)	1ОН			77 177				100		mAd
(V <sub>OH</sub> = 2.5 Vdc)	Source	1000	5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	
(V <sub>OH</sub> = 4.6 Vdc)		- 08	5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(V <sub>OH</sub> = 9.5 Vdc)	987	000	10	-1.3	HVA	-1.1	-2.25	-	-0.9	Porto-Mad	Spine Fil
(V <sub>OH</sub> = 13.5 Vdc)	87	687	15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	_	0.36	-	mAd
(VOL = 0.5 Vdc)	80	06	10	1.3	-	1.1	2.25	-	0.9	VI. 1 To-107	STEEL ST
(VOL = 1.5 Vdc)	2 1	ar i	15	3.6	AM	3.0	8.8	- '	2.4	-	-
Input Current (AL Device	)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μAd
Input Current (CL/CP De	vice)	lin	15		± 0.3	1 -	±0.00001	± 0.3	-	±1.0	μAde
Input Capacitance	GE .	Cin	- 57		_	-	5.0	7.5	-	_	pF
(V <sub>in</sub> = 0)	200	oin					3.0	7.5			PI
Quiescent Current (AL De	avice)	las	5.0		5.0		0.005	5.0		150	μAde
(Per Package)		IDD	10	]	10		0.005	10	smil pal	150 300	MAG
, or ruckuger	08	0.0	15		20		0.010	20		600	1
0 101.101	10 1	08					-				
Quiescent Current (CL/CF	Device)	IDD	5.0	7.09	20	-	0.005	20	tall ber	150	μAd
(Per Package)		4.14	10	-	40	100	0.010	40	-	300	
			15	-	80	1 -	0.015	80	-	600	-
Total Supply Current**†	65	IT	5.0	1			1.75 µA/kH2				μAd
(Dynamic plus Quiesco	ent,	es FAM	10				.50 μA/kH2				CSFISE C
Per Package)	21		15			IT = (2	2.25 µA/kH2	) f + DD	)		
(CL = 50 pF on all ou	puts, all			-							
buffers switching)					100	7 to 1000 a	All Printers and the	The last of the			
Three-State Leakage Curr (AL Device)	ent	ITL	15	-	± 0.1	no seeds	±0.00001	± 0.1	the the sea	±3.0	μAd
Three-State Leakage Curr	ent	ITL	15	-	±1.0	AND MA	±0.00001	±1.0	ne <u>U</u> sani	±7.5	μAd

 $<sup>^{\</sup>circ}$ T<sub>low</sub> =  $-55^{\circ}$ C for AL Device,  $-40^{\circ}$ C for CL/CP Device. T<sub>high</sub> =  $+125^{\circ}$ C for AL Device,  $+85^{\circ}$ C for CL/CP Device.

<sup>\*</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (VDD – VSS) in volts, f in kHz is input frequency, and k = 0.002.

	a Launt Lau		Indan's		aminto costs	
Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH- tTHL	13.2				ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns		5.0	14-1	100	200	
tTLH, tTHL = (0.75 ns/pF) CL + 12.5 ns	8 - 1 8	10	-	50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	4 - 69	15	-	40	80	
Propagation Delay Time Clock to Q	tPLH, tPHL	1 00	E-11V	Pos.3 **0	56V 60 10 8	ns
tpLH, tpHL = (1.7 ns/pF) CL + 215 ns	0.6	5.0	-	300	600	
tpLH, tpHL = (0.66 ns/pF) CL + 92 ns	1.03	10	-	125	250	
tpLH, tpHL = (0.5 ns/pF) CL + 65 ns Reset to Q		15	927	90	180	
tpLH, tpHL = (1.7 ns/pF) CL + 215 ns	- 1 0	5.0	-	300	600	
tpLH, tpHL = (0.66 ns/pF) CL + 92 ns		10	-	125	250	
tpLH, tpHL = (0.5 ns/pF) CL + 65 ns		15	100	90	180	
3-State Propagation Delay, Output "1" or "0"	tPHZ, tPLZ	5.0	-	150	300	ns
to High Impedance	1	10	- 3	60	120	
- 182-10	1 - 1 9	15	- 1	45	90	
3-State Propagation Delay, High Impedance	tPZH, tPZL	5.0	-	200	400	ns
to "1" or "0" Level		10	301	80	160	
acc acc		15	-	60	120	
Clock Pulse Width	twH	5.0	260	130		ns
		10	110	55	-	
		15	80	40	- A	
Reset Pulse Width	twH	5.0	370	185	1-732	ns
	1	10	150	75	to-1 8.53	
		1500	110	55	17.7 63	
Data Setup Time	t <sub>su</sub>	5.0	30	15	(E) V (E)	ns
2.4		10	10	5	(E) A (E)	
	101	15	4	2	civaC=14, n	
Data Hold Time	th	5.0	130	65	DO SELECTIV	ns
		10	60	30	-0.000	
		15	50	25	-	
Data Disable Setup Time	t <sub>su</sub>	5.0	220	110	G JALIMA	ns
005 - DI 646.0 -	- Su	10	80	40	- 100	
	8 1	15	50	25	-	
Clock Pulse Rise and Fall Time	TLH, THL	5.0	991	- Name	15	μs
100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 10	10	-	_	5	1991
		15	-	-	4	
Clock Pulse Frequency	fcl	5.0		3.6	1.8	MHz
COLLEGE AND THE PROPERTY OF THE PARTY OF THE		10	_	9.0	4.5	TOWN DATE OF
		15		12	6.0	

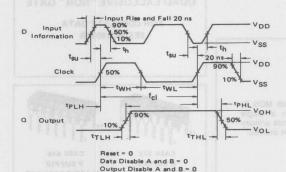
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

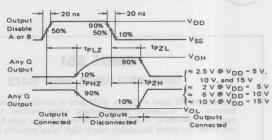
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

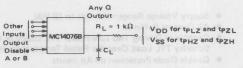
<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### FIGURE 1 - TIMING DIAGRAM

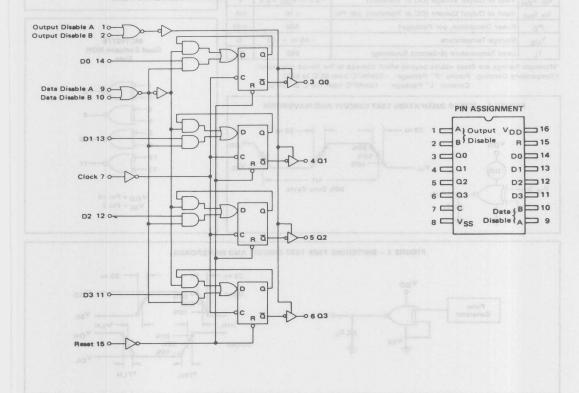


# FIGURE 2 - THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT





### **FUNCTIONAL BLOCK DIAGRAM**



# MC14077B

QUAD EXCLUSIVE "NOR" GATE

FOR COMPLETE DATA SEE MC14070B

## **CMOS SSI**

## QUAD EXCLUSIVE "NOR"GATE

The MC14077B quad exclusive NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolothic structure. This complementary MOS logic gate finds primary use where low power dissipation and/or high noise immunity is desired.

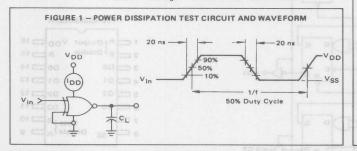
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14077B Replacement for CD4077B Type

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> . I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C





CASE 632

L SUFFIX

CERAMIC PACKAGE

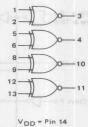
CASE 646
P SUFFIX
PLASTIC PACKAGE

### ORDERING INFORMATION

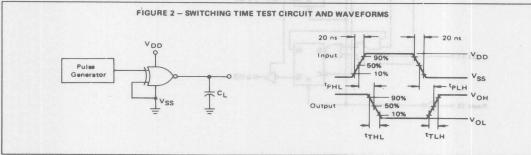
A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

> MC14077B Quad Exclusive NOR Gate



V<sub>DD</sub> = Pin 14 V<sub>SS</sub> = Pin 7



# 8 - INPUT "NOR" GATE

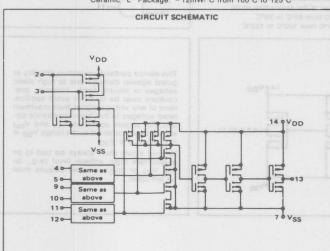
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> . I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C



## **CMOS SSI**

(LOW POWER COMPLEMENTARY MOS)

8-INPUT "NOR" GATE FOR COMPLETE DATA SEE MC14001B



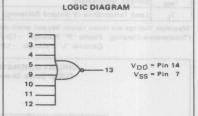


CERAMIC PACKAGE CASE 632 P SUFFIX
PLASTIC PACKAGE
CASE 646

## ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



N.C. pins 1, 6, and 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



# MC14081B



## QUAD 2-INPUT "AND" GATE

The MC14081B is constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). The primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4081B

## **CMOS SSI**

QUAD 2-INPUT "AND" GATE
FOR COMPLETE DATA
SEE MC14001B





CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

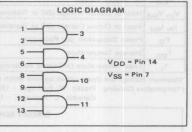
MAXIMUM RATINGS\* (Voltages Referenced to VSS)

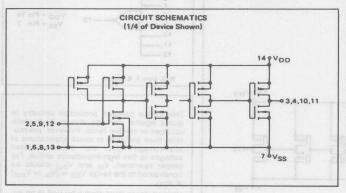
Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C





This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \le (V_{in} \text{ or } V_{OU}) \le V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

## DUAL 4-INPUT "AND" GATE

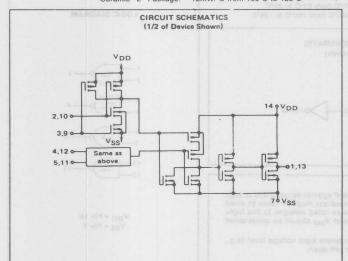
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4082B

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> . I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW"C from 55°C to 85°C Ceramic "L" Package: -12mW"C from 100°C to 125°C



## **CMOS SSI**

(LOW POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "AND" GATE
FOR COMPLETE DATA
SEE MC14001B





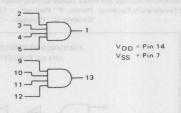
L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX PLASTIC PACKAGE CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### LOGIC DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



# MC14093B



## QUAD 2-INPUT "NAND" SCHMITT TRIGGER

The MC14093B Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B

MAXIMUM RATINGS\* (Voltages Referenced to Voc)

Symbol	Parameter //	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

#### EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

## CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" SCHMITT TRIGGER





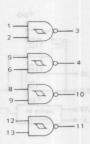
L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX PLASTIC PACKAGE CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: - 40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

## LOGIC DIAGRAM



V<sub>DD</sub> = Pin 14 V<sub>SS</sub> = Pin 7

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

			VDD	T <sub>low</sub> *		25°C			Thigh*		
Characteristic		Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage	"O" Level	VOL	5.0	- 19	0.05	-	0	0.05	2160	0.05	Vdc
Vin = VDD or 0		0.	10	-	0.05	-	0	0.05	_	0.05	(Surject
ear		10	15	-	0.05	_	0	0.05	-	0.05	
00	"1" Level	VOH	5.0	4.95		4.95	5.0		4.95	-	Vdc
Vin = 0 or VDD	007	VOH	10	9.95	977-	9.95	10	-	9.95	100	Vac
300			15	14.95	PRINCE S	14.95	15		14.95	The state of the s	DOTED :
Output Drive Current (AL D		lau	10 101	14.55		14.00	13		14.33		mAdo
	Source	ІОН	5.0	-3.0		-2.4	-4.2	-	-1.7	April 18 Comments	IIIAUC
(V <sub>OH</sub> 4.6 Vdc)	oduce	-	5.0	-0.64	HIGH	-0.51	-0.88		-0.36	SINCE COUR	Francis
(V <sub>OH</sub> = 9.5 Vdc)		-	10	-1.6		-1.3	-2.25		-0.36		1
(V <sub>OH</sub> = 13.5 Vdc)			15	-4.2		-3.4	-8.8		-2.4		
	Jestonian a			-	In a log	-	-	male od o	-	gil" beloc	
OL	Sink	IOL	5.0	0.64	1111 4 1110	0.51	0.88		0.36	Total	mAdd
(V <sub>OL</sub> = 0.5 Vdc)			10	1.6	-	1.3	2.25	-	0.9	-	H
(V <sub>OL</sub> = 1.5 Vdc)			15	4.2		3.4	8.8	-	2.4	-	
Dutput Drive Current (CL/C		10н									mAdo
OII	Source	A BUAGE	5.0	-2.5	SMET SH	-2.1	7.2	181-	-1.7	-	
(V <sub>OH</sub> = 4.6 Vdc)			5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(V <sub>OH</sub> = 9.5 Vdc)			10	-1.3	-	-1.1	-2.25	-	-0.9	-	15 15
(V <sub>OH</sub> = 13.5 Vdc)			15	-3.6		-3.0	8.8	010-2/	-2.4	-	
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	6-	0.36	-	mAdd
(VOL = 0.5 Vdc)		00 mg	10	1.3	-	1.1	2.25	1 =	0.9	-	
(VOL = 1.5 Vdc)		P 1	15	3.6	- 1	3.0	8.8	-	2.4	-	
Input Current (AL Device)		lin	15	-	± 0 1	0	±0.00001	± 0.1	- 1	±1.0	μAdc
Input Current (CL/CP Device)		lin	15	-	± 0.3	-	±0.00001	± 0.3		±1.0	μAdc
Input Capacitance (Vin = 0)	#92 ·	Cin	TURNUT		-	- 6	5.0	7.5	-		pF
Quiescent Current (AL Devi	cel	Ipp	5.0	-	0.25	-	0.0005	0.25	-	7.5	μAdc
(Per Package)		'DD	10		0.50		0.0000	0.50		15	AAGC
Tref rockager			15		1.00		0.0015	1.00		30	
Quiescent Current (CL/CP E	D	1	5.0		1.0	-	0.0005	1.0	-	7.5	-
(Per Package)	Jevice)	IDD	10	late min	2.0	NO.	0.0005	2.0		15	μAdo
(rer rackage)		ROLLYSIN	15	127 E F 14	4.0	TENT -	0.0010	4.0	-	30	May 13
- 12 12 12		+		-	1 4.0	-				30	
Total Supply Current**†		IT	5.0	1000			1.2 µA/kHz				μAdc
(Dynamic plus Quiescen	t,		10				2.4 µA/kHz				
Per Package)			15	Vome		IT = (	3.6 µA/kHz	f + IDD			1 19 White
ICL 50 pF, on all outpo	uts, all										
buffers switching)						0	1		1		-
Hysteresis Voltage		VH	5.0	0.20	0.62	0.17	0.26	0.6	0.13	0.6	Vdc
(Pins 1, 5, 8 and 12 he		The references	10	0.29	0.85	0.25	0.38	0.8	0.20	0.8	
or Pins 2, 6, 9 and 13	held high)	incremi mi	15	0.39	1.20	0.33	0.50	0.9	0.27	1.1	
Threshold Voltage		- Company	-				V more	market and a		Transfer of the last	100
(Pins 2, 5, 9, 12 held hig		VT+	5.0	1.90	4.15	1.80	2.70	4.05	1.70	4.05	Vdc
Pins 1, 6, 8, 13 held hig	h)	- mf 25	10	3.05	6.75	2.95	4.43	6.65	2.85	6.65	1
Positive-Going		my lim in	15	4.12	9.15	4.02	6.03	9.05	3.92	9.05	7 01
Negative-Going		V <sub>T</sub> -	5.0	1.63	3.76	1.63	2.44	3.66	1.53	3.66	Vdc
agV mandaman		-	10	2.70	6.18	2.70	4.05	6.08	2.60	8.08	1
		A	15	3.59	8.40	3.69	5.53	8.30	3.70	8.30	

 $<sup>^*</sup>T_{low} = -55^\circ\text{C}$  for AL Device,  $-40^\circ\text{C}$  for CL/CP Device.  $T_{high} = +125^\circ\text{C}$  for AL Device,  $+85^\circ\text{C}$  for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.004.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

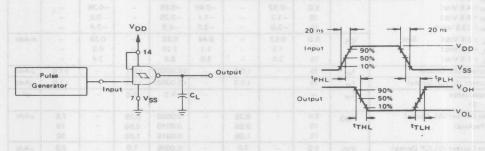
<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (CL = 50 pF, TA = 25°C)

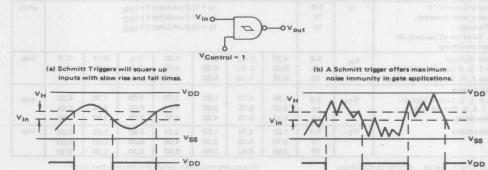
	Ch	aracteristic		nist	Symbol	V <sub>DD</sub> Vdc	Min	Typ #	Max	Unit
Output Rise Time	Wb I	80.0	0		ttlH	5.0	1	100 50	200 100	ns
4V - 1	1.05	1 1	6.0	1-88.6	1 32 7	15	1 454	40	80	
Output Fall Time				9.08	tTHL	5.0	-	100	200	ns
				推制		10	- 1	50	100	
mAm						15	L. NEL E	40	80	tpur Driv
Propagation Delay	Time	1. 6.1	23-		tPLH, tPHL	5.0	- 1	125	250	ns
						10	- 1	50	100	260 A1
				1.5		15	1 - 1	40	80	HOM

#Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## FIGURE 1 - SWITCHING TIME TEST CIRCUIT AND WAVE FORMS



## FIGURE 2 - TYPICAL SCHMITT TRIGGER APPLICATIONS

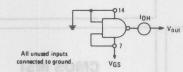


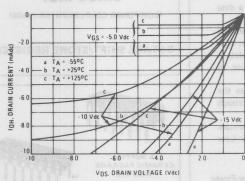
6

Vout

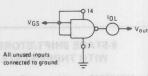
## MC14093B

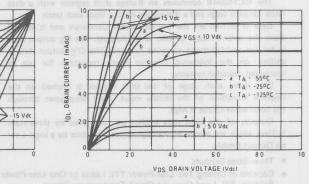
### FIGURE 3 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT



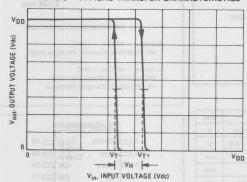


### FIGURE 4 - TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT





## FIGURE 5 - TYPICAL TRANSFER CHARACTERISTICS





# MC14094B

# 8-STAGE SHIFT/STORE REGISTER WITH THREE-STATE OUTPUTS

The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Qs output data is for use in high-speed cascaded systems. The Q's output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Pin-for-Pin Compatible with CD4094B

### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	±10 goV	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

Output				Parallel	Outputs	Serial (	Outputs
Clock	Enable	Strobe	Data	Q1	QN	QS*	Q'S
5	0	X	X	Z	Z	Q7	No Chg.
7	0	X	X	Z	Z	No Chg.	Q7
5	1	0	X	No Chg.	No Chg.	Q7	No Chg.
5	1	1	0	0	Q <sub>N</sub> -1	Q7	No Chg.
5	1	1	1	1	Q <sub>N</sub> -1	Q7	No Chg.
1	1	1	1	No Chg.	No Chg.	No Chg.	Q7

Z = High Impedance

X = Don't Care

\*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q8.

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

8-STAGE SHIFT/STORE REGISTER



L SUFFIX CERAMIC PACKAGE CASE 620

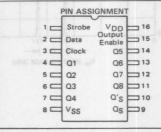


PSUFFIX
PLASTIC PACKAGE
CASE 648

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	T <sub>low</sub> *		25°C			Thigh*		
Characteristic	Symbol	Vdc	Min Max		Min	Typ #	Max	Min	Max	Uni
Output Voltage "0" Level	VOL	5.0	1 0	0.05	-	0	0.05	2002 000	0.05	Vdd
V <sub>in</sub> = V <sub>DD</sub> or 0	100	10	1	0.05	-	0	0.05	EASTER!	0.05	-F2
*In = *DD of o		15		0.05		0	0.05	Stin BLB7	0.05	T
0.0			4.05	0.00	4.05	-		4.05		144
"1" Level	VOH	5.0	4.95	100	4.95	5.0	-	4.95	the residence	Vdd
V <sub>in</sub> = 0 or V <sub>DD</sub>		10	9.95	1.119	9.95	10		9.95	double on the	100
and the same of th		15	14.95	1897-	14.95	15		14.95	NURC OF N	
Input Voltage "0" Level	VIL							Did total		Vde
(VO 4.5 or 0.5 Vdc)		5.0	-	1.5	1	2.25	1.5	00000	1.5	
(VO = 9.0 or 1.0 Vdc)	7 - 4	10		3.0	-	4.50	3.0	and a	3.0	
(Vo. 135 or 15 Vdc)		15	1	40		6.75	4.0	S 10 700 S	4.0	100
"1" Level	VIH	100				201 52000	2000	(III)	1997 AND 1997	
(Vo = 0.5 or 4.5 Vdc)	- IH	5.0	3.5		3.5	2.75	D ( Storen	3.5	197 119	Vdc
(VO : 1.0 or 9.0 Vdc)	-	100		1		- CT - CT - CT - CT - CT - CT - CT - CT	O THESE	THE RESERVED TO		1 400
		10	7.0	-	7.0	5.50	7	7.0	star Para	5010
(V <sub>O</sub> = 1 5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	S. Charles	11.0	-	
Output Drive Current (AL Device)	ІОН	To be				20 127 0	O Roles	8E 01 -		mAd
(VOH = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	- Frederick	-1.7		
(VOH = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	-	-0.36	rack Establish	1-8
(VOH = 9.5 Vdc)		10	-1.6		-1.3	-2.25		-0.9	401 01 000	100
111 1251111		15	-4.2	-	-3.4	-8.8	AL LABOUR	-2.4	Hat 73173	
	-	5.0	0.64		0.51	0.88		0.36	77 17	mAd
(VOL = 0.4 Vdc) Sink	IOL			-		450000	(i) Hugan	State of the second	Hat 1471	MAG
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1 3	2.25	- 29	0.9	BIRT AG	90
(V <sub>OL</sub> = 1.5 Vdc)	-	15	4.2	-	3.4	8.8	(3 Higher	2.4	ENIZT TER	
Output Drive Current (CL/CP Device)	ІОН	- OF		Total I		- 60 ES E	S THOM	SE OF -		mAd
(VOH = 2.5 Vdc) Source		5.0	-2.5	- 1	-2.1	-4.2	2 Dalar	-1.7	991 -5 HB	1
(VOH = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	di Garan	-0.36	- n	
(VOH = 9.5 Vdc)		10	-1.3		-1.1	-2.25	O How	-0.9	20172	
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	1	-3.0	-8.8	2 4 4	-2.4	- Carrier	
	1.	5.0	0.52	-	0.44	0.88	CONTRACTOR OF THE PARTY OF THE	0.36	200	mAd
OL .	OL	(80.00)	100000000000000000000000000000000000000	100	1			0.36		1000000
(V <sub>OL</sub> = 0.5 Vdc)	(15.5) (15.5)	10	1.3	1 1	1.1	2.25		7.12	NED AT HER	10
(V <sub>OL</sub> = 1.5 Vdc)	99	15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)	lin	15	-	±01		± 0.00001	±01	-	± 1.0	μAdı
Input Current (CL/CP Device)	1 <sub>in</sub>	15		±03		±0 00001	±03	-	± 1.0	μAd
Input Capacitance	Cin	- 46		-	-	50	7.5	-	and place	pF
(V <sub>10</sub> 0)	100	1.6		Land.						
Quiescent Current (AL Device)	las	5.0		50	-	0.005	5.0	1201	150	μAd
(Per Package)	IDD	10		10		0.010	10		300	J Artu
(rei rackage)	- 88 - 1	15	- 1	20		0.015	20			1 1
				+					600	-
Quiescent Current (CL/CP Device)	1DD	5.0		20	-	0.005	20	- OUTE NA	150	μAd
(Per Package)		10		40		0.010	40	-	300	
		15	-	80		0.015	80	-	600	-
Total Supply Current * †	1 <sub>T</sub>	5.0		197	1- = 1/	1.1 µA/kHz	) f + In-	Variety	port is subject	μAd
(Dynamic plus Quiescent,		10				14 μA/kHz				
Per Package)	1	15				140 µA/kHz				
(C <sub>1</sub> = 50 pF on all outputs, all	000	13	1		1T = (	HO MAIKINZ				- Constant
buffers switching)	255									The same
			-			_				-
3-State Output Leakage	ITL	15	-	± 0.1		± 0.0001	± 0.1	and the same	± 3.0	μΑ
Current (AL Device)					THE DESIGNATION	SECURITION OF	no tomeyr	aris vell grid		101 6-17
3-State Output Leakage	ITL	15		± 1.0			± 1.0		± 7.5	μА
Correct (CL/CR Review)	I L	10		-1.0	total news	design reprised	- 1.0	Contract of the	-1.0	I pun

 $<sup>^*</sup>T_{low} = -55^\circ\text{C}$  for AL Device,  $-40^\circ\text{C}$  for CL/CP Device.  $T_{high} = +125^\circ\text{C}$  for AL Device,  $+85^\circ\text{C}$  for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.001 .

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

## MC14094B

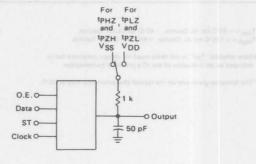
## SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

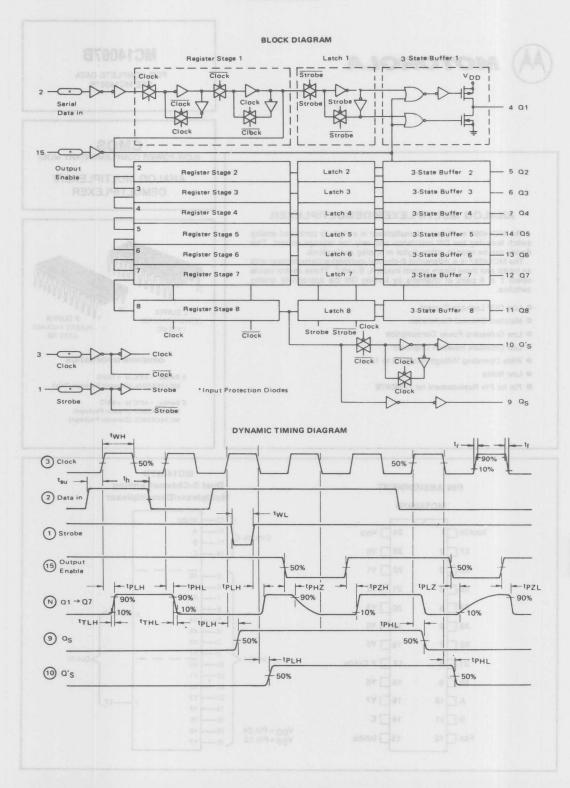
Chara	ecteristic		Symbol	V <sub>DD</sub> Vdc	Min	Typ#	Max	Unit
Output Rise and Fall Time			tTLH,			-		ns
tTLH, tTHL = (1.35 ns/	nE) C. + 33 ne		THL	5.0	10Y	100	200	by suding
tTLH, tTHL = (0.6 ns/p			BO STHL	10		50	100	A-EIA
tTLH, tTHL = (0.4 ns/p			180 Q 1	15		40	80	
	IF I CL + 20 hs	200		10		40	00	
Propagation Delay Time			tPLH.		R. I. Land		DON NO	ns
Clock to Serial out QS	15		tPHL	ATT SEE		050	000	L LIE
tPLH, tPHL = (0.90				5.0	TO THE PERSON NAMED IN	350	600	sleV rue
tpLH, tpHL = (0.36			100	10	-	125	250	(30)
tpLH, tpHL = (0.26	ns/pF) C <sub>L</sub> + 82 ns		For I	15	-	95	190	0.99
Clock to Serial out Q'S			0.0				ALC: TANKER	
tpLH, tpHL = (0.90	ns/pF) CL + 350 ns			5.0	1	230	460	93/3
tpLH, tpHL = (0.36	ns/pF) CL + 149 ns			10	ME	110	220	V - AND
tpLH, tpHL = (0.26	ns/pF) C1 + 62 ns			15	- 1	75	150	ON
Clock to Parallel out	00.0		1 9				₩ 2 E M G	QV)
tpLH, tpHL = (0.90	ns/pF) C <sub>1</sub> + 375 ns			5.0		420	840	- 0 A)
tpLH, tpHL = (0.35				10	HE!	195	390	utput Dri
tpLH, tpHL = (0.26			- 10	15	_ 1	135	270	HOVE
Strobe to Parallel out	700		96	0-1 02			- CEVER	HQ(9)
tpl H, tpH1 = (0.90	00/0E) C. + 245 00		- 0	5.0		290	580	ROVI-
tp_H, tpHL = (0.36			- 1 0	10		145	290	HOVI
			The state of	15		100	200	JOV)
tpLH, tpHL = (0.26				15	100	100	200	
Output Enable to Output			1 1	5.0		140	200	30 VI
tpHZ, tpZL = (0.90			tPHZ.	5.0		140	280	TOA
tpHZ, tpZL = (0.36			tPZL	10	1110	75	150	NO HUNDLY
tPHZ, tPZL = (0.26	ns/pF) CL + 42 ns		4	15	- 1	55	110	HOW
tpLZ, tpZH = (0.90 )			tpLZ.	5.0	-	225	450	HOY
tpLZ, tpZH = (0.36	ns/pF) CL + 77 ns		tPZH	10		95	190	HOY
tpLZ, tpZH = (0.26	ns/pF) CL + 57 ns		1 8	15	- 1	70	140	MD 97
Setup Time	88.0	86.0	t <sub>su</sub>	0 0 0 0	light 1	pigness	(58W 94.0)	ns
Data in to Clock			30	5.0	125	60	1.TV 8.0	JOVI
				10	55	30	1.5 % == 1	Was
			10-1	15	35	20	mail Takes	mail Chem
Hold Time	2.6 × 170000 n=1		co th	5.0	0	-40	110-13	ns
Clock to Data			'h	10	20	- 10	PA 1977 P. D. 181	115
Siden to Data				15	20	0	sonetici	eqs:7 ruq
Cleak Bules Wideh Uist		-	*****	5.0	200	100		ns
Clock Pulse Width, High			tWH		100	50	J. JAr Jugosu	
			1 01	10	83		Lupasi	
	00 L 860 B		85	15	. 63	40		
Clock Rise and Fall Time			t <sub>r(cl)</sub>	5	000	Technol P	15	μѕ
			t <sub>f</sub> (cl)	10	-	-	5.0	
nou l	on mon		00	15	-	-	4.0	
Clock Pulse Frequency			fcl	5.0	- 1	2.5	1.25	MHz
				10		5.0	2.5	
				15	- 1	6.0	3.0	
Strobe Pulse Width	CONTRACTOR OF THE	10.7	1	5.0	200	100		
Strobe Pulse Wiath			tWL		No. of Contract,		10 III - 10 6	ns
				10	80	40	CONTRACTORS	
				15	70	35	_	

\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## 3-STATE TEST CIRCUIT







# MC14097B

FOR COMPLETE DATA SEE MC14067B

## CMOS

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXER/

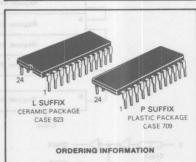
## ANALOG MULTIPLEXER/DEMULTIPLEXER

The MC14097 multiplexer/demultiplexer is a digitally controlled analog switch featuring low ON resistance and very low leakage current. This device can be used in either digital or analog applications.

The MC14097 is a differential 8-channel multiplexer/demultiplexer with

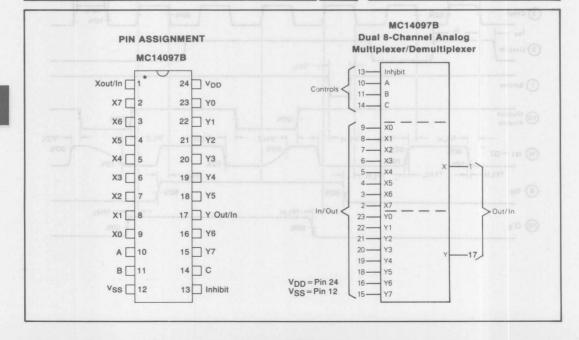
The MC14097 is a differential 8-channel multiplexer/demultiplexer with an inhibit and three binary control inputs A, B and C. These control inputs select 1 of 8 pairs of channels by turning ON the appropriate analog switches.

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4097B



A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



### 8-BIT ADDRESSABLE LATCHES

The MC14099B and MC14599B are 8-bit addressable latches. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. For the MC14599B the data pin is a bidirectional data port and for the MC14099B the input is a unidirectional write only port. The Write/ Read line controls this port in the MC14599B.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.

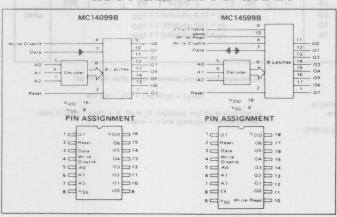
A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B

### MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter Parameter	Value	Unit
VDD	DC Supply Voltage	0 5 to + 18 0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	0 5 to V <sub>DD</sub> + 0 5	V
Im- lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Packaget	500	mW
Istg	Storage Temperature	65 to - 150	C
TL	Lead Temperature (8-Second Soldering)	260	C

\*Maximum Ratings are those values beyond which damage to the device may occur †Temperature Derating Plastic "P Package - 12mW °C from 65°C to 85°C Ceramic "L" Package 12mW °C from 100°C to 125°C



## CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT ADDRESSABLE LATCH

MC14599B WITH BIDIRECTIONAL PORT



CERAMIC PACKAGE CASE 620

PLASTIC PACKAGE CASE 648



L SUFFIX CERAMIC PACKAGE

PLASTIC PACKAGE CASE 726 CASE 707

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range VSS ≤ (Vin or  $V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

			VDD	Tio	w°		25°C		Thi	gh "	1
Characteristic	Syr	mbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Uni
Output Voltage "0"	Level V	OL	5.0	-	0.05	-	0	0.05	-	0.05	Vdd
Vin = VDD or 0		0.	10	-	0.05	-	0	0.05	-	0.05	
			15	-	0.05	-	0	0.05	-	0.05	
"1"	Level V	он	5.0	4.95	ZIN	4.95	5.0	menz	4.95	_	Vde
Vin = 0 or VDD		OH	10	9.95	_	9.95	10		9.95		
All A ON ADD			15	14.95	_	14.95	15		14.95	_	
Input Voltage "0"	11 1	,	10	14.50	ALC: STORY	14.55	10	AL III.	14.00	01.3301.00	Vdd
	Level V	'IL		orazo datas	al dalah	ID POOTO	0.05	feath wi	grille in s	S sent a cons	Voc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		- 1	5.0	mits won!	1.5	olymerhi	2.25	1.5	DA and	1.5	TENT.
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	TIBE		10	fr 103	3.0	GA curre	4.50	3.0	sel Terre	3.0	n-vin
(V <sub>O</sub> = 13.5 or 1.5 Vdc)			15	-	4.0	-	6.75	4.0	-	4.0	1014
	Level V	/IH		ST SSE D		Study Here	CL207 LINE		B11.20.10		1
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	SOURCE PARK		5.0	3.5	1407	3.5	2.75	DR- 6 7	3.5	E 17000	ROW
(V <sub>O</sub> = 1.0 or 9.0 Vdc)			10	7.0	-	7.0	5.50	Enemon	7.0	mes-ind	Regit
(V <sub>O</sub> = 1.5 or 13.5 Vdc)			15	11.0	by Tunt	11.0	8.25	o-bat	11.0		1
Output Drive Current (AL Device)	10	ОН		TO SERVICE OF	U alder	T accepts	1	water but	who are the	designation a	mAd
(VOH = 2.5 Vdc) Sou			5.0	-3.0		-2.4	-4.2	-	-1.7	_	1
(VOH = 4.6 Vdc)	Figures		5.0	-0.64		-0.51	-0.88	_	-0.36	eura y	13.10
(VOH = 9.5 Vdc)			10	-1.6	_1/10	-1.3	-2.25	AL WITTE	-0.9	H DELVEN	A
(VOH = 13.5 Vdc)			15	-4.2	_	-3.4	-8.8	_	-2.4		12 8
(VOI = 0.4 Vdc) Sin	k le	OL	5.0	0.64	_	0.51	0.88	_	0.36	_	
(VOL = 0.5 Vdc)	" "	OL	10	1.6	1, 2, 1	1.3	2.25		0.9	attel Out	S =
(VOL = 1.5 Vdc)			15	4.2		3.4	8.8	_	2.4		100
	:> 1-		-10	7.2		0.4	0.0			CHARLE DON	mAd
Output Drive Current (CL/CP Dev		ОН		-2.5		-2.1	-4.2		-1.7		mAd
(V <sub>OH</sub> = 2.5 Vdc) Sou	irce	- 11	5.0		1.5.4		1	_			
(V <sub>OH</sub> = 4.6 Vdc)			5.0	-0.52	0.00	-0.44	-0.88	40.TOW	-0.36	वि शायावय	0 0
(V <sub>OH</sub> = 9.5 Vdc)			10	-1.3	post at	-1.1	-2.25 -8.8	ed) Jevo	-2.4	I VALUE	18
(V <sub>OH</sub> = 13.5 Vdc)		-	15	-3.6	_	-3.0	-	-		-	
(VOL = 0.4 Vdc) Sin	k 10	OL	5.0	0.52	-	0.44	0.88	-	0.36	-	
(V <sub>OL</sub> = 0.5 Vdc)	\$ 5 P S 6		10	1.3	-	1.1	2.25	-	0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)	MARIE		15	3.6	_	3.0	8.8	_	2.4	_	
Input Current (AL Device)		In 1	15	-	±0.1	- /	±0.00001	±0.1	W) 48 0	±1.0	μAd
Input Current (CL/CP Device)	1	lin	15	- 10	±0.3	-	±0.00001	±0.3	-	±1.0	μAd
Input Capacitance	C	Cin	_	-	_	-	5.0	7.5	-		pF
(V <sub>in</sub> = 0)	HUR J	""							111111111111111111111111111111111111111		
Input Capacitance	0	Cin	_	-		_	15.0	22.5	_		pF
MC145998 - Data (pin 3)	33A	-in				nH 1916	10.0	10 NO 10	100000		la luch
(V <sub>in</sub> = 0)											
Quiescent Current (AL Device)	1.		EO		E 0		0.006	5.0		150	
(Per Package)	10	DD	5.0	(5)	5.0	-	0.005	10	81,/17/100	300	μAd
(rei rackage)				-	20		0.010	20	M) 90,700	600	
10.10	-	-	15	-		-	0.015		-		-
Quiescent Current (CL/CP Device)	10	DD	5.0	-	20	-	0.005	20	-	150	μAd
(Per Package)			10	-	40	-	0.010	40	-	300	
17 18 4 18 2 10k	Europi, I.		15	-	80	-	0.015	80	-	600	
Total Supply Current**†	1	IT	5.0		manant	IT = (1.	5 μA/kHz)	f + IDD	Hedricks	182	μAd
Dynamic plus Quiescent,			10	The same			0 μA/kHz)				
Per Package)	4 4 4		15				5 µA/kHz)				
(CL = 50 pF on all outputs,	- 7					-	ALT WORK	Wangel.			
all buffers switching)				127							1110

 $^{\circ}T_{low}$  =  $-55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high}$  =  $+125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

"The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_{\overline{I}}$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (VDD – VSS) in volts, f in kHz is input frequency, and k=0.004.

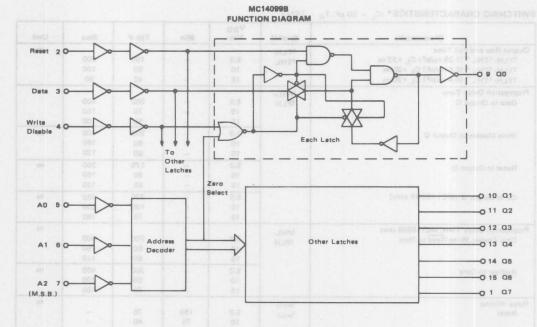
SWITCHING CHARACTERISTICS\* (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise and Fall Time  tTLH.tTHL = (1.35 ns/pF) Ct +32 ns	tTLH, tTHL	5.0		100	200	ns
tTLH, tTHL = (0.6 ns/pF) CL + 20 ns tTLH, tTHL = (0.4 ns/pF) CL + 20 ns		10	1	50 40	100	
Propagation Delay Time	tPHL,		1.0	- lest	No.	ns
Data to Output Q	tPLH.	5.0	_	200	400	
77	7	10	_	75	150	
AS	and a	15	_	50	100	61193
Write Disable to Output Q	all lands	5.0	-	200	400	ns
		10	11 + 1	80	160	
the same and the same and the same and the		15	- 197	60	120	
Reset to Output Q		5.0	-	175	350	ns
	SOUTH STATE	10	-	80	160	
The same of the sa		15	-	65	130	
CE to Output Q (MC14599B only)		5.0	7	225	450	ns
10 11 games and 11 00		10		100	200	e GA
		15	1 +	75	150	
Propagation Delay Time, MC14599B only	tPHL.	1.0			400	ns
Chip Enable, Write/Read to Data	tPLH	5.0	-	200	160	a ra
		10 15	1 1	80 65	130	
Address to Data		5.0		200	400	
Address to Data		10	I	90	180	ns
10 10		15	- I	75	150	1 - SA
Pulse Widths	tw(H)					ns
Reset	tw(L)	5.0	150	75	_	
	-W(L)	10	75	40	_	
		15	50	25	ortifice-	
Write Disable		5.0	320	160	-	ns
With Disable stopping and delta state of the	OMUAD	10	160	80	- Treesite	ship
and the address loude A.S. At and A.S.		15	120	60		-
Set Up Time	t <sub>su</sub>					ns
Data to Write Disable		5.0	100	50	-	1 8
		10	50	25		
		15	35	20		
Hold Time	th				rigate to sales	ns
Write Disable to Data	1 1/2 2	5.0	150	75	0701	C IS OF N
		10 15	75 50	40 25		1 5 6
810	NORTH AND	DECLEME				
Set Up Time	tsu	5.0	100	45	-	ns
Address to Write Disable	many to	10 15	80 40	30	-	-
		/	-		1-1	
Removal Time Write Disable to Address	trem t	5.0	0	-80	400-5	ns
Willia Disable to Address	BEY -	10	0	- 40 - 40	1	
		15	U	- 40		1

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the İC's potential performance.

## MC14099B•MC14599B

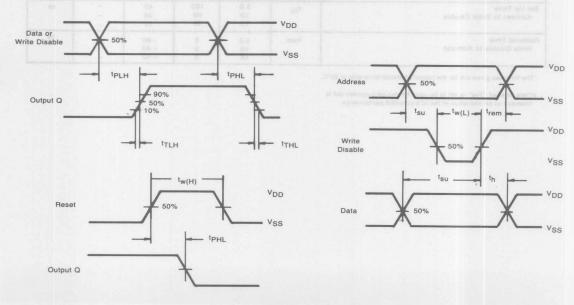


T	m	 19	4.4	-	A	13	-

Write Disable	Reset	Addressed Letch	Unaddressed Latches
0	0	Data	Q <sub>n</sub> °
0	1	Data	Reset
1	0	Q <sub>n</sub> °	Qn*
1	1 -	Reset	Reset

CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

#### SWITCHING WAVEFORMS

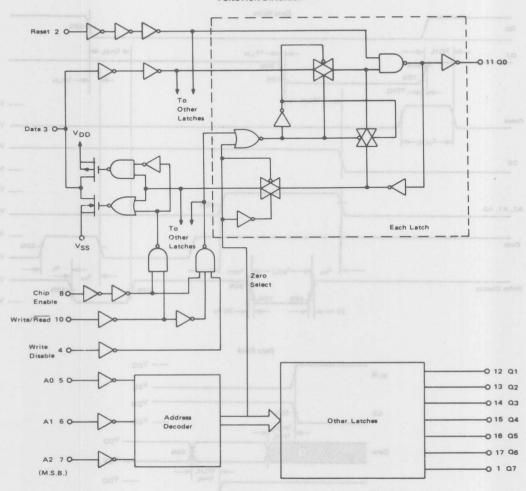


<sup>\*</sup> Qn is previous state of latch.

<sup>†</sup> Reset to zero state.

## MC14099B•MC14599B

MC14599B FUNCTION DIAGRAM



TRUTH TABLE

Chip Enable	Write/Read	Write Disable	Reset	Addressed Latch	Other Latches	Data Pin
0	×	х	0	•	•	Z
- 1	1	0	0	Data	•	Input
1	1	1	0	•	•	Z
1	0	X	0			Qn
Х	X	х	1	0	0	Z/0

X = Don't care.

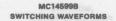
CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

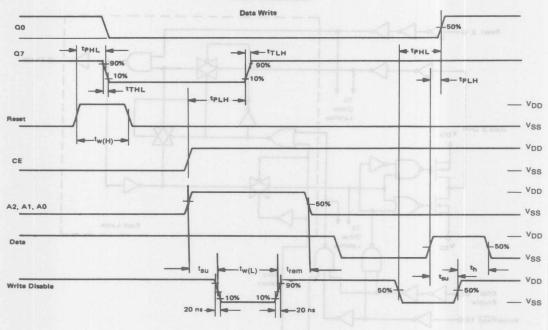
<sup>\* =</sup> No change in state of latch.

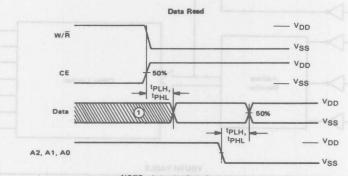
Z = High impedance.

Qn = State of addressed latch.

# MC14099B•MC14599B







NOTE: 1. Invalid Data Output 2. Reset in LOW State

MC14106B

## **Advance Information**

#### HEX SCHMITT TRIGGER

The MC14106B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14106B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

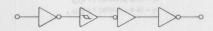
- Increased Hysteresis Voltage Over the MC14584B
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace the MC14584B or MC14069UB

MAXIMUM RATINGS\* (Voltages Referenced to Voc

MAVIM	OM HATINGS (Voltages Referenced to VSS)		
Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TI	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C
Ceramic "L" Package: -12mW/°C from 100°C to 125°C

#### EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$  Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

## **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

HEX SCHMITT TRIGGER





L SUFFIX
CERAMIC PACKAGE
CASE 632

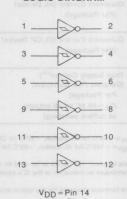
P SUFFIX
PLASTIC PACKAGE
CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### LOGIC DIAGRAM



VSS = Pin 7

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

 $<sup>^{\</sup>circ}$ Tlow =  $-55^{\circ}$ C for AL Device,  $-40^{\circ}$ C for CL/CP Device. Thigh =  $+125^{\circ}$ C for AL Device,  $+85^{\circ}$ C for CL/CP Device.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intendedas an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.001.

 $<sup>{}^{\</sup>dagger}V_H{}^{}=V_T{}_+{}^{}-V_T{}_-$  (But maximum variation of  $V_H$  is specified as less than  $V_T{}_+{}^{}$  max  ${}^-V_T{}^-$  min).

SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise Time	tTLH	5.0	_	100	200	ns
		10	-	50	100	
		15	_	40	80	
Output Fall Time	tTHL	5.0		100	200	ns
		10		50	100	
		15	-	40	80	
Propagation Delay Time	tPLH, tPHL	5.0		125	250	ns
		10	- Fileson Labor	50	100	
		15	10-0	40	80	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

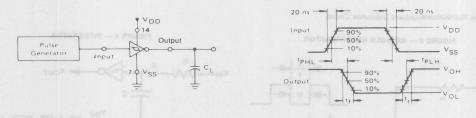
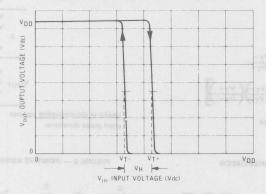


FIGURE 2 - TYPICAL TRANSFER CHARACTERISTICS



### APPLICATIONS

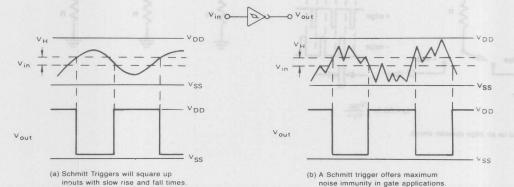


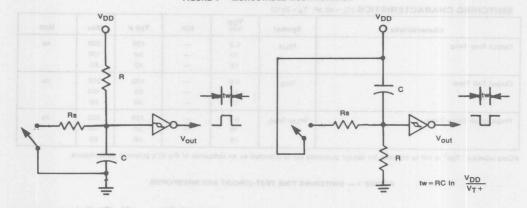
FIGURE 3

noise immunity in gate applications.

6-191

# MC14106B

#### FIGURE 4 - MONOSTABLE MULTIVIBRATOR



Useful as Pushbutton/Keyboard Debounce Circuit.

FIGURE 5 - ASTABLE MULTIVIBRATOR

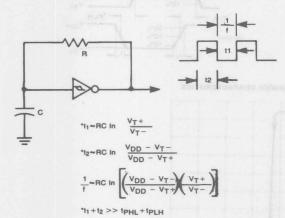
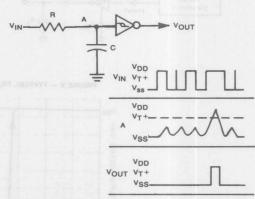


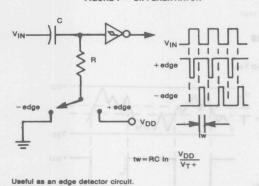
FIGURE 6 - INTEGRATOR

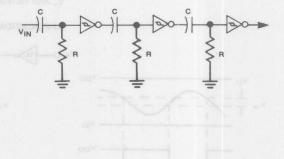


Useful in discriminating against short pulse durations.

FIGURE 7 - DIFFERENTIATOR

FIGURE 8 — POSITIVE EDGE TIME DELAY CIRCUIT





### **CMOS MSI**

MA180B thru MC14163B

# SYNCHRONOUS PRESETTABLE 4-BIT COUNTERS

The MC14160B – MC14163B are synchronous programmable counters constructed with complementary MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160 – 74163 TTL counters.

Two are synchronous programmable BCD counters with asynchronous and synchronous clear inputs respectively (MC14160B, MC14162B). The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (MC14161B, MC14163B).

- Internal Look-Ahead for Fast Counting
- Carry Output for N-Bit Cascading
- Synchronously Programmable
- Synchronous Counting
- Load Control Line
- Synchronous or Asynchronous Clear
- Positive Edge Clocked

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin, lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$  Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ . Unused outputs must be left open.

# MC14160B

BCD COUNTER
with Asynchronous Clear

## MC14161B

4-BIT BINARY COUNTER with Asynchronous Clear

## MC14162B

BCD COUNTER with Synchronous Clear

## MC14163B

4-BIT BINARY COUNTER with Synchronous Clear





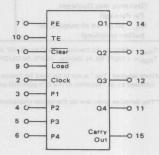
PLASTIC PACKAGE CASE 648 L SUFFIX CERAMIC PACKAGE CASE 620

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### BLOCK DIAGRAM



V<sub>DD</sub> = Pin 16 V<sub>SS</sub> = Pin 8

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

のとなりまとつ形式		VDD	Tie	ow*		25°C		Thi	gh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0		0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0	00	10	-	0.05	-	0	0.05		0.05	-
"" 55		15	-	0.05	-	0	0.05		0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	4 (2.7)	4.95		Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	· OH	10	9.95	_	9.95	10		9.95	-	1
BOD COUNTER		15	14.95	-	14.95	15		14.95	-	
Input Voltage "0" Level	VIL			710-4	W 189.67	TERRITO	SHORE	HOME	18	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	.12	5.0		1.5		2.25	1.5	_	1.5	1
(V <sub>O</sub> =9.0 or 1.0 Vdc)		10		3.0		4.50	3.0	- 1	3.0	
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15		40	1 1	6.75	4.0	_	4.0	
ASTRUOD Y BA "1" Level	VIH		SAMUNIA.	note tu	nonnan	12 STB 751	ACTA LO	- 8581	PERMIT	1
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	-114	5.0	3.5	S P.Ch	3.5	2.75	D Littley	3.5	noc_ 218	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	alone and	7.0	5.50	abien to	7.0	ng kanno	K3:14
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	berts - 11 3	11.0	8.25	COLUMN TWO	11.0	These s	GOVERN
Output Drive Current (AL Device)	1		111.0		1.0	0.20		a Hitmon	177 0	mAdo
- Inches	ІОН	5.0	-3.0		-2.4	-4.2		-1.7		IIIAGE
(V <sub>OH</sub> = 2.5 Vdc) Source (V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	N THE ST	-0.51	-0.88	TIB TOOLS	-0.36	11/0 SOLL 0	
(V <sub>OH</sub> = 9.5 Vdc)	(Dotton	10	-1.6	THE REAL PROPERTY.	-1.3	-2.25	non-	-0.9	DISCHARGE OF STREET	and s
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	THOUSE YOU	-3.4	-8.8	an elnav	-2.4	DOMESTIC OF	DI MONTO
	100		-	139314	-	-			(81818)	mAdo
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36		MAGG
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.25	-	2.4		13.49
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2		3.4	8.8	-	2.4		-
Output Drive Current (CL/CP Device)	ЮН						0 118-14	ni nemi		mAdd
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	A PLANT	-1.7		100
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52		-0.44	-0.88		-0.36		
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	Entur	-0.9	NO bear it	
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	- 0	-2.4	The second of	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	mitznys/	0.36	THOUSE	mAdd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3	1	1.1	2.25	Biosti	0.9	entitiet.	
(V <sub>OL</sub> = 1.5 Vdc)	10	15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)	lin	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 1.0	μAdd
Input Current (CL/CP Device)	lin	15	-	±03	-	±0.00001	± 0.3	-	± 1.0	μAdd
Input Capacitance	Cin	the same			-	5.0	7.5	-		pF
(Vin - 0) where the source of										
Quiescent Current (AL Device)	IDD	5.0	-	5.0	(The W	0.005	5.0		150	μAdd
(Per Package)	'00',	10		10	the o	0.010	10	THE REAL PROPERTY.	300	
		15	646	20		0.015	20	19	600	l ion
O	les	5.0	5 58 6	-	+	0.005	20	nonto	-	1.01
Quiescent Current (CL/CP Device)	1DD	10	-	20		0.000	40		150	μAdd
(Per Package)		15	- U = 00	40	-	0.010	80	The state of the s	300	1 180
				80	- CO 180				600	+
Total Supply Current**†	IT	5.0				.56 µA/kHz				μAdd
(Dynamic plus Quiescent,		10	-			.1 µA/kHz				
Per Package)		15	1001 -		1T = (1	.9 μA/kHz	1 + IDD			73
(C <sub>1</sub> = 50 pF on all outputs, all			1 0							dill.

 $^{\circ}T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

high - Fizz o for AL Device, Fig. o to o for our or

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.001.

\*\*The formulas given are for the typical characteristics only at 25°C.

1 Clear V<sub>DD</sub> 16
2 Clock Carry Out 15
3 P1 Q1 14
4 P2 Q2 13
5 P3 Q3 12
6 P4 Q4 11
7 PE TE 10

Load 9

Z

8 - VSS

SWITCHING	CHARACTERISTICS	(C) = 50 pF TA = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise Time	tTLH	Ratero	H ,BGent	EDM) NO		ns
		5.0	_	100	200	
		10		50	100	
en - 251 005 0.8 pp.d		15	_	40	80	2003
Output Fall Time	†THL					ns
		5.0	-	100	200	
		10	_	50	100	. 0:019. X
		15	-	40	80	
Propagation Delay Time	tPLH.					ns
SHM 03 08 - 08 - 10	†PHL			VO.		astun X
Clock to Q		5.0		250	700	1 2 to F
tpLH, tpHL = (0.90 ns/pF) C <sub>L</sub> + 305 ns		5.0		350 150	700 300	
tpLH, tpHL = (0.36 ns/pF) C <sub>L</sub> + 132 ns	TOTAL NOVEMBER	15		100	200	- Inner
tpLH, tpHL = (0.26 ns/pF) C <sub>L</sub> + 87 ns Clock to Carry Out		15	100-	100	200	
tpLH, tpHL = (0.90 ns/pF) CL + 395 ns	Company of the Compan	5.0	to and the part	440	880	Selected
tpLH, tpHL = (0.36 ns/pF) CL + 167 ns	10000	10	manife and	185	370	A SEE CHE
tpLH, tpHL = (0.26 ns/pF) C <sub>L</sub> + 112 ns		15	_	125	250	
TE to Carry Out						
tpLH, tpHL = (0.90 ns/pF) CL + 225 ns		5.0	_	300	600	
tpLH, tpHL = (0.36 ns/pF) CL + 112 ns		10	-	130	260	
t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 77 ns		15	_	90	180	
Clear to Q (MC14106B, MC14161B only)						11111
t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 110 ns		5.0	-	350	700	
$t_{PLH}$ , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 37 \text{ ns}$		10	_	150	300	1.18.27
t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 22 ns		15	-	100	200	
Setup Times						-,1
Data to Clock	tsu	5.0	320	160	-	ns
		10	130	65	-	
		15	90	45	-	
Load to Clock		5.0	600	300	-	
		10	260	130	-	
		15	180	90	-	
Enable to Clock (PE or TE)		5.0	420	210	_	
		10	170	85	-	
		15	120	60	_	
Clear to Clock (MC14162B, MC14163B only)		5.0	310	155	_	
		10	70	55 35		
		13	10	33		
Hold Times Clock to Data		5.0	40	-00		
Clock to Data	th	5.0	-10	-60		ns
		15	-5 0	- 25 - 15		
		15	0	- 15		
Clock to Load	- 1 7	5.0	-40	- 195	_	
		10	-10	-80	_	
		15	-5	-50	_	
	M. D. C.			14-17		
Clock to PE		5.0	-40	- 175	_	
		10	-10	- 70	-	
		15	0	-40	-	
Clock to TE		5.0	450	000	10.00	
Olock to TE		5.0	-150 -30	- 280 - 130		
		15	-30	- 130		
		13	20	00		
Clock to Clear (MC14162B, MC14163B only)		5.0	80	40	_	
		10	30	15	_	
		15	- 10	-70	_	
Clear Removal Time (MC14160B, MC14161B only)	1	5.0	90	30	_	ns
and instruction (morations, morations only)	trem	10	65	20		ns

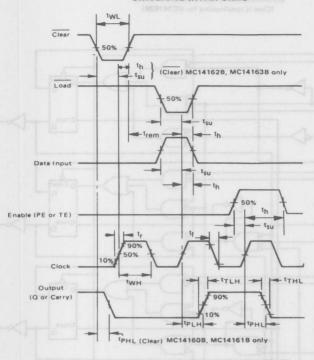
SWITCHING CHARACTERISTICS (C1 = 50 pF, TA = 25°C) (Continued)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Clear Pulse Width, Low (MC14160B, MC14161B only)	twL	5.0	200	100	THE ST	ns
		10	90	45	-	171.0
		15	60	30	_	
Clock Pulse Width, High	twH	5.0	250	125	_	ns
		10	100	50	- 1000	Boll Not
000 001 - 002		15	70	35	-	
Clock Rise and Fall Time	t <sub>r</sub> ,	5	_ =	-	15	μS
	tf	10	_	-	5	
m number		15	_	- 60	- 4	moltegage
Clock Pulse Frequency	fcl	5.0	-	2.0	1.0	MHz
		10	_	5.0	2.5	C) (a) should
		15	800 <u>-</u> JC	8.0	4.0	el migi - legge

\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

#### SWITCHING WAVEFORMS



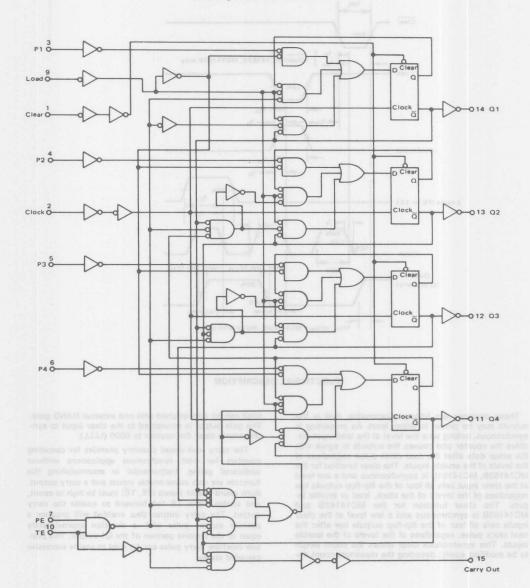
#### **FUNCTIONAL DESCRIPTION**

These counters are fully programmable; that is the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the MC14160B, MC14161B is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs. The clear function for the MC14162B and MC14163B is synchronous and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily; decoding the maximum count de-

sired can be acomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (PE, TE) must be high to count, and enable input TE fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages.

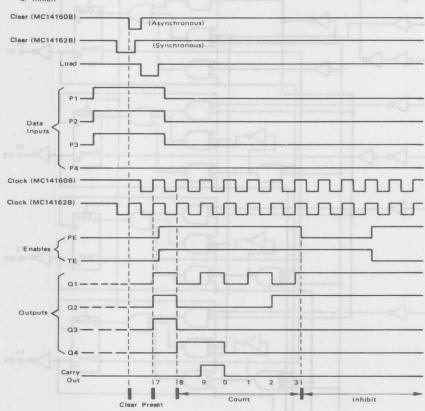
MC14160B, MC14162B LOGIC DIAGRAM (Clear is synchronous for MC14162B)



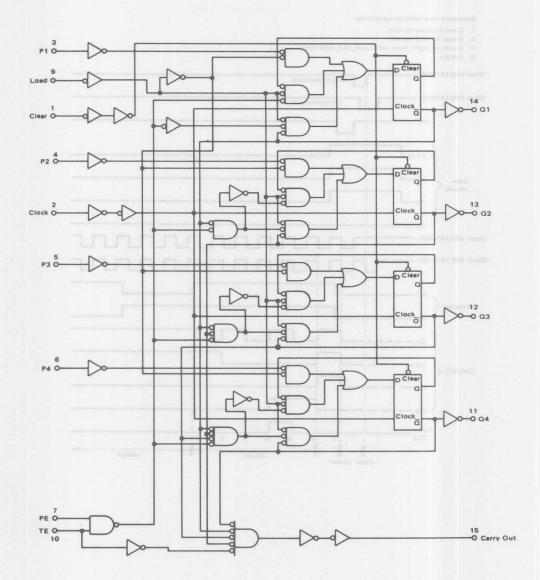
#### MC14160B, MC14162B TIMING DIAGRAM

Sequence illustrated in waveforms:

- 1. Clear outputs to zero.
- Preset to BCD seven.
   Count to eight, nine, zero, one, two, and three.
- 4. Inhibit



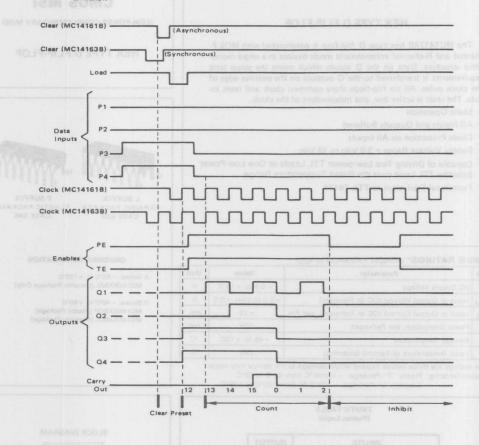
MC14161B, MC14163B LOGIC DIAGRAM (Clear is Synchronous for MC14163B)



MC14161B, MC14163B TIMING DIAGRAM



- 1. Clear outputs to zero.
- 2. Preset to binary twelve.
- 3. Count to thirteen, fourteen, fifteen, zero, one, and two,
- 4. Inhibit



## MC14174B

#### HEX TYPE D FLIP-FLOP

The MC14174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- Functional Equivalent to TTL 74174

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

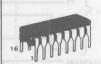
\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Pastic "P" Package: - 12mW/"C from 65°C to 85°C Ceramic "L" Package: - 12mW/"C from 100°C to 125°C

# esq.

# CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

HEX TYPE D FLIP-FLOP





L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

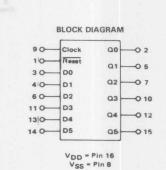
#### TRUTH TABLE (Postive Logic)

	OUTPUT		INPUTS	
1	Q	Reset	Data	Clock
]	0	1	0	
	1	1	1	_
No	Q	1	X	7
Chang	0	0	Х	X

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either Vss or VDD). Unused outputs must be left open.



	MOYT DA		VDD	Tie	ow*		25°C		Th	igh °	1
Characteristic	8 00	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage	"O" Level	VOL	5.0	-	0.05	-	0	0.05	The said	0.05	Vdc
Vin = VDD or 0	100	0.	10		0.05	-	0	0.05	Albert Unit	0.05	NESOUN !
55	100	1 . 5 .	15	-	0.05	_	0	0.05	10 ar ar	0.05	122
	"1" Level	VOH	5.0	4.95	-	4.95	5.0	1 38 7.46	4 95	SHE IK	Vdc
Vin = 0 or VDD	. Leve.	TOH	10	9.95	_	9.95	10	1019	9.95	JRT B.	171
III BO		-	15	14.95	Lings	14.95	15	or FootO	14.95	and war	Proces
Input Voltage	"O" Level	VIL	- 6		39392		are dil	F 4 19 45	nian Exti	F JUNET W	Vdc
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$	84	-11	5.0		1.5		2.25	1.5	Ten (T. 6)	1.5	1
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$			10		3.0		4.50	3.0	Len Do. Sti	3.0	162
$(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$	20		15		4.0	1112	6.75	4.0	Em 19.57	4.0	191
140 - 15.5 51 1.5 4467	"1" Level	VIH	10		1		0.70	9771940	- 1879 5 1	NOU NO IS	14014
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$	Level	AIH	5.0	3.5	-	3.5	2.75	64 E00 I	3.5	E.W - 1	Vdc
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$	001		10	7.0		7.0	5.50	- 2t -	7.0	200.02	
$(V_0 = 1.5 \text{ or } 13.5 \text{ Vdc})$	200		15	11.0		11.0	8.25	10 To 10 To 10	11.0		191
			15	11.0		. 11.0	0.25	10.20 +	11.0	W. W 1	mAdc
Output Drive Current (AL I		ЮН		-3.0	11365	-2.4	-4.2	3.0	-1.7	thing and a	MAGC
011	Source	00	5.0		-				-0.36		
$(V_{OH} = 4.6 \text{ Vdc})$	80	20	5.0	-0.64	-	-0.51	-0.88		-0.36	-	
(V <sub>OH</sub> = 9.5 Vdc)	test	200	10	-1.6	Jup	-1.3 -3.4	-2.25 -8.8		-2.4	daller achies	Testar!
$(V_{OH} = 13.5 \text{ Vdc})$	250		15	-4.2	-		-		-		
OL	Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
(V <sub>OL</sub> = 0.5 Vdc)		100	10	1.6	-	1.3	2.25	- '	0.9	-	
(VOL = 1.5 Vdc)	0.3		15	4.2	17	3.4	8.8	-	2.4	par Fredu's	Cieck
Output Drive Current (CL/0	CP Device)	IOH	1 0			116					mAdo
(V <sub>OH</sub> = 2.5 Vdc)	Source		5.0	-2.5		-2.1	-4.2		-1.7		1
(V <sub>OH</sub> = 4.6 Vdc)			5.0	-0.52		-0.44	-0.88	100	-0.36		100
(VOH = 9.5 Vdc)			10	-1.3	-	-1.1	-2.25	-	-0.9	- Salito	1
(V <sub>OH</sub> = 13.5 Vdc)			15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.52	_	0.44	0.88	_	0.36	-	mAdo
(VOL = 0.5 Vdc)	20	0.	10	1.3	-	1.1	2.25	-	0.9	amil'E-pass	6150
(VOL = 1.5 Vdc)		- 00	15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)	- 0	lin	15		± 0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Current (CL/CP Devi	ce)	lin	15	-	± 0.3	-	±0.00001	± 0.3		±1.0	μAdc
		_	15	-	-0.0	-	5.0		+	- 1.0	pF
Input Capacitance (V <sub>in</sub> = 0)	31	Cin	-		-	-	5.0	7.5			pr-
				-			0.005	5.0	-		-
Quiescent Current (AL Dev		IDD	5.0		5.0	-	0.005	5.0	T garet	150	μAdc
(Per Package)	- 00	001	10	1 7	10	-	0.010	10	1	300	
	100	1350	15	-	20		0.015	20	1	600	
Quiescent Current (CL/CP)	Device)	IDD	5.0	-	20	-	0.005	20	-	150	μAdo
(Per Package)	The same of the sa		1(	-	40	CVIOT SI	0.010	40	of our pass	300	477
			15	-	80	-	0.015	80	-	600	
Total Supply Current ** †		IT	5.0		100 (0)	IT - (1	1.1 µA/kHz)	f + Inn	ion of "syl"	sonedel d	μAdo
(Dynamic plus Quiescen	it,		10			IT = (2	2.3 µA/kHz)	f + IDD			1
Per Package)			15				3.7 µA/kHz)				
(CL = 50 pF on all outp	uts, all										
buffers switching)											-

 $<sup>^*</sup>T_{low} = -55^\circ C$  for AL Device,  $-40^\circ C$  for CL/CP Device.  $T_{high} = +125^\circ C$  for AL Device,  $+85^\circ C$  for CL/CP Device.

\*\*The formulas given are for the typical characteristics only at 25°C.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I  $_T$  is in  $_\mu A$  (per package), C  $_L$  in pF, V = (V  $_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k = 0.003.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

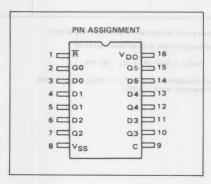
## MC14174B

SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

			West?	VDD		All Types		
Characteristic			Symbol	Vdc	Min	Тур#	Max	Unit-
Output Rise and Fall Time		1. 7	TLH, THL	- 1	10%	16997 7	6	ns
tTLH, tTHL = (1.35 ns/pF) CL +	32 ns			5.0	-	100	200	OX = my
tTLH, tTHL = (0.6 ns/pF) CL + 2	20 ns			10		50	100	
TLH, THL = (0.4 ns/pF) CL +	20 ns		1 3 1 3	15	HOA	40	80	
Propagation Dalay Time - Clock to C	2	30.0	tPLH.	15 14				ns
tpLH, tpHL = (0.9 ns/pF) CL + 16	35 ns		TPHL	5.0	-17	210	400	coulse V turi
tpLH, tpHL = (0.36 ns/pF) CL + 6	34 ns		d air	10	-	85	160	d A = mVI
tpLH, tpHL = (0.26 ns/pF) CL + 5			8.6	15	-	65	120	0.0 - 0.91
Propagation Delay Time - Reset to C			tPHL				1007 1 1 100	ns
tpHI = (0.9 ns/pF) C1 + 205 ns				5.0	1000	250	500	80 - 0V
tpHL = (0.36 ns/pF) CL + 79 ns				10	_	100	200	0.7= 0V1
tpHL = (0.26 ns/pF) CL + 62 ns			1 - 1 - 3	15		75	150	1 1 - 1 VI
Clock Pulse Width			tWH	5.0	150	75	JAI -may	ns
			- 0	10	90	45	_1 ×5 V 8	IVOH = 2
			1 76	15	70	35	_ neve	PE HOUT
Reset Pulse Width	5.74	2.0	tWL	5.0	200	100	Epv 8	ns
				10	100	50	ToleVill	- HOAL
				15	80	40	7,446	17 OF = D
Clock Pulse Frequency	8.8	PIT	fcl	5.0	-	7.0	2.0	MHz
				10	1 -01	12.0	5.0	V 10 IUstu
			1 3	15	-	15.5	6.5	F HOY
Clock Pulse Rise and Fall Time	42.25		tTLH, tTHL	5.0	-	-	15	Ms
				10	-	-	5	180V
				15	-		4	THOW
Data Setup Time	25	100	t <sub>su</sub>	5.0	40	20	740/3	ns
				10	20	10	+35V 5	10 VI
			10.1	15	15	0	Isones (A)	terraid too
Data Hold Time	(9000.04		th	5.0	80	40	Best (=1, 20)	ns
			1	10	40	20	- 4364	man 3 tues
			II. S. II.	15	30	15	_	10 - mVI
Reset Removal Time	E00.6		trem	5.0	250	125	each JAI mas	ns
				10	100	50	100	19gs Paci-
			1 11	15	80	40		

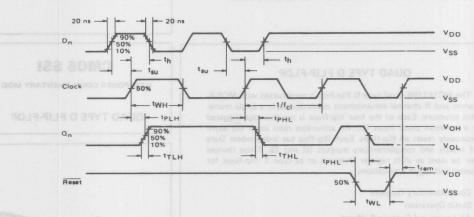
\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

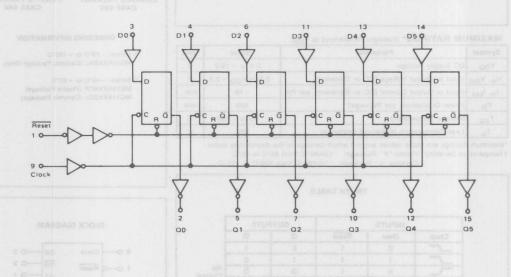


## MC14174B

#### TIMING DIAGRAM



#### **FUNCTIONAL BLOCK DIAGRAM**





## MC14175B

#### QUAD TYPE D FLIP-FLOP

The MC14175B quad type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input  $(\overline{R})$  asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and  $\overline{Q}$ ). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Compatible with Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74175

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	0.5 to + 18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	65 to · 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW °C from 65°C to 85°C Ceramic "L" Package: - 12mW °C from 100°C to 125°C

#### TRUTH TABLE

	INPUTS		OUT	PUTS	
Clock	Data	Reset	Q	ā	
	0	1	0	1	
	1	1	1	0	
~	X	1	Q	ā	No Change
X	X	0	0	1	Change

X = Don't Care

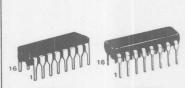
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

## **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

QUAD TYPE D FLIP-FLOP



L SUFFIX CERAMIC PACKAGE CASE 620

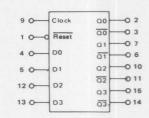
PSUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

BLOCK DIAGRAM



V<sub>DD</sub> = Pin 16 V<sub>SS</sub> = Pin 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

'0'' Level	Symbol	V <sub>DD</sub> Vdc	Min	Max	Min	Typ#	Max	Min	Max	1
'0'' Level	-		A CONTRACTOR	L Louis Co.	101111	'yp'	News	141111	ABINI	Unit
	VOL	5.0	-	0.05		0	0.05	-	0.05	Vdc
	0.	10	-	0.05	-	0	0.05	and the same	0.05	Courses.
607		15	-	0.05	-	0	0.05		0.05	1112
'1" Level	VOH	5.0	4.95	-	4.95	5.0	and I was	4.95	- 14-11	Vdc
(%)	TOH	10	9.95	_	9.95	10		9.95	- 1-17	6133
		15	14.95	_	14.95	15	- 24	14.95		
"O" Level	VII			57 6107		8.0	d Paralla	nimiT vo	aC netter	Vdc
	-11	5.0		1		2 25	1.5	20 - 20	1.5	1
68 1	-		_	-		7.67	3.0	100-10 G		100
05			-		_		4.0	0.20-00		100
"1" Level	VIII			1.0						
	*IH	5.0-	2.5	access.	26	2 75	I lend	3.5	leG nobes	Vdc
326	-		2711300	1	0.35		= 000	2000	un (L1) -	13.797
189				_			874ETT	10.000	n 88_01 +	Hell
	la.	13	11.0	-	11.0	0.23		411.0	FBE.01 F	mAdo
	ЮН	F.0	-30		-24	42		-17		IIIAGG
ource	250			601/4					fulle agluff	Closk
45	100				1					
36. 1	75		4		1					V = 1
			-	-		-		-		mAde
ink	10 TO TO 10			1993		10 0000000		100	Purse Velier	MAG
00-				-					-	
00 1		15	4.2	-	3.4	8.8		2.4		-
	ІОН							1.3		mAde
				7.07			-	179/70/70	part dalut	Diode
	-		1	-	1		-	1		
92	-			-			7.5		-	
			-	-		-		-		
ink	IOL			JH = JH			- 300	A STATE OF THE PARTY OF	said-cele	mAdd
				-	1		-	1	- 70	
- 1		15	3.6	-	3.0	8.8	-	2.4	-	150
	lin	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 1.0	μAdd
e)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdd
60			-	1 -	-	5.0	7.5	-	-	pF
100										
-01	lee	5.0	-	5.0	-	0.005	5.0	-	150	μAdd
ne -						100000000000000000000000000000000000000	- Carlotte	_		2
ar I			1 -1			The second second		_		
			+	+	-	-		-		-
evice)	'DD		9.		1					μAdd
08	001				1 7			1		
			-	1 80	LT	1			600	+
	IT									μAdd
		15			17 = (£	.U μA/kHz)	I + IDD			100 h
ts, all			Market							and a
	"1" Level evice) ource ink  P Device) ource ink e)	"1" Level VIH  evice) IOH ource  Ink IOL  P Device) OH ource  Inn Cin Cin e) IDD	"0" Level VIL 5.0 10 15 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 10 10 15 15 15 10 10 15 15 15 15 15 15 15 15 15 15 15 15 15	"0" Level VIL 5.0 — 10 — 15 — 11" Level VIH 5.0 3.5 10 7.0 15 11.0 15 — 11.0 15 — 15 — 15 — 15 — 15 — 15 — 15 — 15	"0" Level VIL 5.0 - 1.5 1.0 - 3.0 1.5 - 4.0 1.5 - 4.0 1.5 1.0 7.0 - 1.5 1.0 7.0 1.5 1.0 7.0 1.5 1.0 7.0 1.5 1.0 7.0 1.5 1.0 1.0 1.0 1.6 1.6 1.5 4.2 - 1.5 1.5 4.2 - 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5	"0" Level VIL 5.0 - 1.5 - 3.0 - 15 - 4.0 - 15 - 4.0 - 15 - 4.0 - 15 - 4.0 - 15 - 7.0	"0" Level VIL 5.0 - 1.5 - 2.25   10 - 3.0 - 4.50   15 - 4.0 - 6.75   "1" Level VIH 5.0 3.5 - 3.5 2.75   10 7.0 - 7.0 5.50   11 1.0 - 11.0 8.25   evice)	"0" Level VIL 5.0 - 1.5 - 2.25 1.5 1.5 1.0 1.0 - 3.0 - 4.50 3.0 3.0 - 4.50 3.0 1.5 - 4.0 - 6.75 4.0 1.5 - 4.0 - 6.75 4.0 1.5 - 4.0 - 6.75 4.0 1.5 1.0 7.0 - 7.0 5.50 - 1.5 11.0 - 11.0 8.25 - 1.5 11.0 - 11.0 8.25 - 1.5 11.0 - 11.0 8.25 - 1.5 11.0 - 11.0 8.25 - 1.5 11.0 - 11.0 8.25 - 1.5 11.0 - 11.0 8.25 - 1.5 11.0 - 11.0 8.25 - 1.5 11.0 - 11.0 8.25 - 1.5 1.5 1.0 1.0 1.6 - 1.3 2.25 - 1.5 1.5 1.0 1.6 - 1.3 2.25 - 1.5 1.5 1.0 1.6 1.3 2.25 - 1.5 1.5 1.0 1.6 1.3 2.25 - 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5	"0" Level VIL 5.0 - 1.5 - 2.25 1.5 - 100 - 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 4.50 3.0 - 7.0 5.50 - 7.0 5.50 - 7.0 5.50 - 7.0 1.5 11.0 - 11.0 8.25 - 11.0 9.20 - 7.0 5.50 - 7.0 1.5 11.0 - 11.0 8.25 - 11.0 9.20 - 11.0 9.20 - 7.0 1.5 1.0 8.2 - 11.0 9.20 - 11.0 9.20 - 11.0 9.20 - 11.0 9.20 - 11.0 9.20 - 12.0 9.20 9.20 9.20 9.20 9.20 9.20 9.20 9	"0" Level VIL 50 - 1.5 - 2.25 1.5 - 1.5 10 - 3.0

 $^*T_{low} = -55^\circ C$  for AL Device,  $-40^\circ C$  for CL/CP Device.  $T_{high} = +125^\circ C$  for AL Device,  $+85^\circ C$  for CL/CP Device.

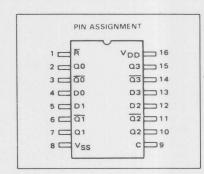
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: I  $_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V  $_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k = 0.004.



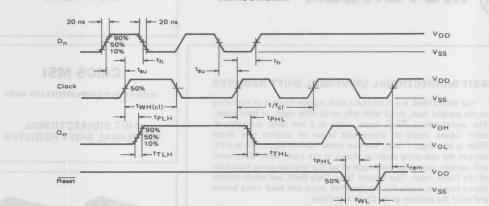
## MC14175B

SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

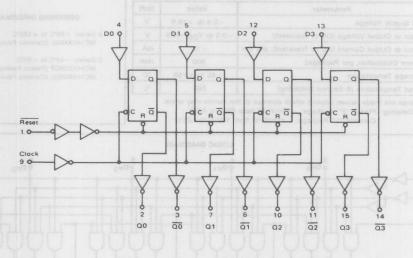
		XIIOT	VDD		All Types		
Characteristic		Symbol	Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	0	tTLH, THL	- 1 01			0 10 00	ns
tTLH, tTHL = (1.35 ns/pF) C1 + 3	2 ns	101, 1110	5.0		100	200	
tTLH, tTHL = (0.6 ns/pF)C1 + 20		2014	10	100	50	100	1
tTLH, tTHL = (0.4 ns/pF) CL + 20		80 E	15	- 1	40	80	De Const
Propagation Delay Time — Clock to	Q, Q	tpLH.		Taby In	aut "G"	391	ns
tpLH, tpHL = (0.9 ns/pF) CL + 175	ns	tPHL	5.0	-	220	400	0/49
tpLH, tpHL = (0.36 ns/pF) CL + 72		- 60 1	10 00	-	90	160	TOVI.
tpLH, tpHL = (0.26 ns/pF) CL + 57		0.8	15	-	70	120	GAI :
Propagation Delay Time — Reset to	Q, Q	t <sub>PHL</sub> ,	80 08		100	15 or 4 5 Vide	ns
tpHL = (0.9 ns/pF) CL + 280 ns		tPLH t	5.0	-	325	500	+ (2V)
tpHL = (0.36 ns/pF) Ct + 112 ns		011 - 1	10	-	130	200	POW)
tpHL = (0.26 ns/pF) CL + 87 ns			15	HDF	100	150	o.D.tugle
Clock Pulse Width	- SH-02	tWH	5.0	250	110	55V 8.4	ns
			10	100	45	15.Vde	SOVI
		i -	15	75	35	13.5 Visel	( MgVI
Reset Pulse Width	88,0	tWL	5.0	200	100	125V # C	ns
			10	80	40	0.5 Voc	DOM
			15	60	30	12tiV 8 1	1 30 K)
Clock Pulse Frequency	5.40	fcl	5.0	- 1	4.5	2.0	MH
90.0-		330-	10	- 1	11	5.0	ROVE
			15	-	14	6.5	MOVI
Clock Pulse Rise and Fall Time	88.0	TLH, THL	5.0	l Ini	-tnit	15	из
26 -			10	-	-	5	(VeV)
		90   -	3 15 01	- 1	-	4	J.eVI
Data Setup Time	10000.01	tsu	5.0	120	60	G 90 October	ns
			10	50	25	-	10000
THE ST	0.5		15	40	20	_tonatio	10 J July
Data Hold Time	800.0	th	5.0	80	40	1.18. Lossin	ns
000 - 01		07 1	10	40	20	-1889	7 951
		05	15	30	15		
Reset Removal Time	010.0	trem	5.0	250	125	- Capacia	ns
000 - 29		1 00	10	100	50	-	
			15	80	40	15 TaFling V	

\*The formulas given are for the typical characteristics only at 25°C. #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.





#### FUNCTIONAL BLOCK DIAGRAM





## MC14194B

#### 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The MC14194B is a 4-bit static shift register capable of operating in the parallel load, serial shift left, serial shift right, or hold mode. The asynchronous Reset input, when at a low level, overrides all other inputs, resets all stages, and forces all outputs low. When Reset is at a logic 1 level, the two mode control inputs, S0 and S1, control the operating mode as shown in the truth table. Both serial and parallel operation are triggered on the positive-going transition of the Clock input. The Parallel Data, Data Shift, and mode control inputs must be stable for the specified setup and hold times before and after the positive-going Clock transition.

- Synchronous Right/Left Serial Operation
- Synchronous Parallel Load
- Asynchronous Hold (Do Nothing) Mode
- Functional Pin for Pin Equivalent of LS194

MAXIMIM PATINGS\* (Voltages Referenced to Voc)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> . I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

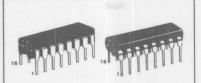
\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

LOGIC DIAGRAM Q DPO PDP2 Dp3 DSR 2 0 DSL VDD = Pin 16 VSS = Pin 8 DO DO DQ 600 001 0 02 03 12

#### ELECTRICAL CHARACTERISTICS (Voltages Referenced to Vss)

		VDD	110	ow*		25°C		'h	igh "	1
c lan	Symbol	Vdc	Min	Max	Min	Typ#	Max	Min	Мак	Unit
"0" Level	VOL	5.0	1/20	0.05	12	0	0.05	-	0.05	Vdc
50 50	10 1 00	10	-	0.05	-	0	0.05		0.05	
0 60 1	10 1 10	15	-	0.05	-	0	0.05	-	0.05	
"1" Level	Vou	5.0	4 95	2 4 6	4 95	5.0	1980	4 95	_	Vdc
10000	* OH			1			_		_	1
				0 1 1	1		Table 1		_	
"O" Lovel	V.,		11100					11.00		Vdc
O Cever	- AIL	E 0	1 3	15		2.25	1.5	Laure To	1.5	Vac
	7 7 2		25							
	1/	15	10 100	4.0	-	0.75	4.0		4.0	-
Level	VIH					0.00				
			1	-					-	Vdc
		(a) (3.52)	9.35	ropac =	The Control of the Co	March 1995 1995	alvisia:	THE RESERVE AND ADDRESS OF THE PERSON NAMED IN	423 (100)	0.7300
		15	11.0	-	11.0	8.25	_	11.0		
The second second	ЮН		1							mAdo
Source	RHW		and the second	Sing2			THE PERSON		-	
			1000000	31,737		1	-	\$200 miles 1 4 4 4	P bett and	ingrati
		10		-			いっから	A STATE OF THE PARTY OF	- 37/17	KUT?
08		15	-4.2	-	-3.4	-8.8	00 T (D)	-2.4	0.70177	1.175
Sink	101	5.0	0.64	-	0.51	0.88	35 4 35	0.36	· ATT	mAdo
		10	1.6		1.3	2.25	-	0.9	Suda Tipod	annan'
		15	4.2	- 1	3.4	8.8	-	2.4	To each	water.
(CP Device)	lou	0.0				80 000	4.019	Lies Foot =	DOMEST ALL O	mAdo
	·OH	5.0	-2.5		-2.1	-42	Same	-1.7	Marie and M	
80			100000			100			THE PARTY OF	
				-			_		and the same	1000
nar I			1 .	100					100,000	1000
	1-		-	-	-	-	HARON TA	100000000000000000000000000000000000000	100	mAdo
SINK	OL		1180-110-11		1000000	100000000000000000000000000000000000000				MAGC
	-			-	1000000		o ce o		CO1 - 174	
	OID			-			-		White on	2005
	I in	-	-		-	± 0.00001	± 0.1	-	± 1.0	μAdc
ice)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdc
ST.	Cin	_40.0 Dit	-	-	-	5.0	12.0	-	mits 15 or i	pF
vice)	Inn	5.0	-	5.0	-	0.005	5.0	-	150	μAdo
8.6	.00	10	-	10	-	0.010	10	25000		Clastic
0.6	9.1	15	-	20	-	0.015	20	Add the	600	(53:1)
Device	Inn			20		-	20			μAdo
Devicer	.00		1 20000	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2				T Hall bes	1 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -	имас
	- 1					100000000000000000000000000000000000000	-10-20			
	1-		-	1 00	1 - "				600	-
	'T		13							μAdc
nt,	102									10UIOS
0		15			IT = (2	2.9 µA/kHz)	1+1DD			SHIG.
puts, all	00.									
	"1" Level "0" Level "1" Level Device) Source	"0" Level VOL  "1" Level VOH  "0" Level VIL  "1" Level VIH  Device) IOH  Source IOH  Source IOH  CP Device) IOH  Lin  ice) Iin  Cin  Vice) IDD  Device) IDD	Company   Comp	Symbol   Vdc   Min	Companies   Symbol   Vdc   Min   Max	Color   Colo	Correct   Corr	Correct   Corr	C	Color

 $^{\circ}T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

"The formulas given are for the typical characteristics only at 25°C.

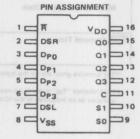
†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



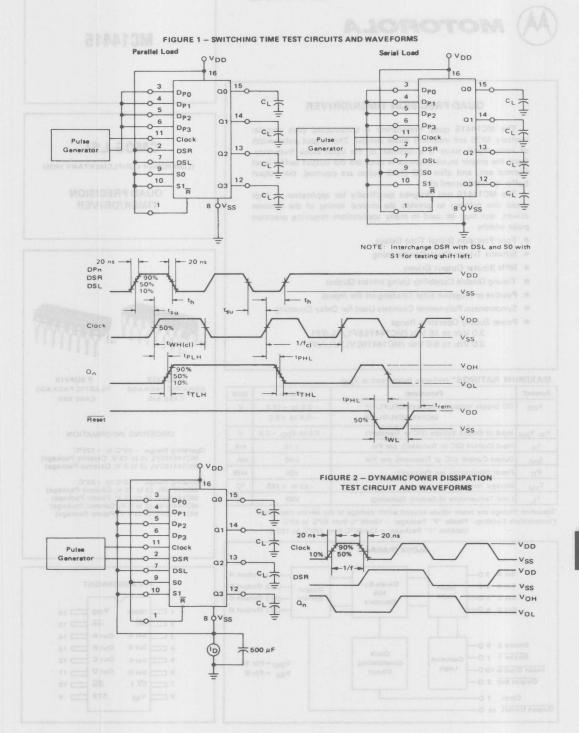
OPERATING	relait.		INPU (Reset			French	OUT	PUTS 1 + 1)	21	Character
MODE	S1	SO	DSR	DSL	DP0-3	QO	Q1	Q2	03	Howhold suggest
Hold	0	0	×	×	×	00	Q1	02	03	0 ip ogV + p
50.9	1	0	×	.0	×	01	02	Q3	0	
Shift Left	1	0	×	- 1	×	01	02	03	1	
	0	1	0	×	X	0	00	Q1	02	00V-00 = 2
Shift Right	0	1	1	×	×	1	00	Q1	02	
	1	1	×	×	0	0	0	0	0	ner Votruge
Parallel		1	X	X	9 1	- 1	1	1	1	BV 80 to 6 to 6VI

Characteristic	0.5-	Symbol	V <sub>DD</sub> Vdc	Min	Typ#	Max	Unit
Output Rise and Fall Time	68.0	TLH, THL	9.6			100 V 851	ns
TLH, THL = (1.35 ns/pF) CL + 32 ns		200	5.0		100	200	HEAR)
tTLH, tTHL = (0.6 ns/pF) CL + 20 ns		- L SA	10	- 1	50	100	How!
tTLH, tTHL = (0.4 ns/pF) CL + 20 ns		184	15	100	40	80	I WALL
Propagation Delay Time Clock to Q	10. E	tPLH,tPHL	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			s vact	ns
tpLH,tpHL = (0.9 ns/pF) CL + 230 ns			5.0	100	275	550	ord man
tpLH,tpHL = (0.36 ns/pF) CL + 92 ns		- 1 6.5	10		110	220	(Vinte
tpLH,tpHL = (0.26 ns/pF) CL + 72 ns		58.0	15	- 1	85	170	HOV?
Reset to Q		tPHL	-01			Tobal E.B	ns
tpHL = (0.9 ns/pF) CL + 305 ns		20	5.0	- 1	350	700	(VIIIV)
tpHL = (0.36 ns/pF) CL + 122 ns		1 531	10	-	140	280	1037
tpHL = (0.26 ns/pF) CL + 97 ns		5.1	15	1 1	110	220	38337
Clock Pulse Width	81/1	twH	5.0	280	140	1:4V 8.1	ns
		101	10	110	55	Sept. 3 - 4 F to	root Coor
		202	15	85	40		
Reset Pulse Width	-	tWH	5.0	180	90	_	ns
			10	70	35	806.81%	MAHO THE
			15	50	26		T rackly
Clock Pulse Frequency		fcl	5.0	F 845 1	3.6	1,8	MHz
(Shift Right or Left Mode)			10		9.0	4.5	17 12 17
			15		12	6.0	
Clock Pulse Rise and Fall Time		TLH, THL	5.0	A DICE T	19091/013	15	μѕ
		1	10		_	5	3 1957
		1/0	15			4	
Setup Time	1 or not	t <sub>su</sub>	0.7	1 1		777	ns
Data to Clock		-su	5.0	10	-8.0	Seamer strike or	and Articles
		18 11 11 11	10	20	0		100
			15	40	9.0	0 10 00 10 1	100
Mode Control (S) to Clock		-	5.0	200	100		ns
			10	75	36		113
		4 of t	15	55	27	80 JA-46 O'8	Russill.
Hold Time		th	- 10	MACH STREET, SQ	PERT HONE	CUATETAT (B)	ns
Data to Clock		<sup>t</sup> h	5.0	180	90	- 100	
Allow of EggV - QgV2 = V, Hq M, Q, Sephiling ray; A.		luntur	10	50	25	Fill "gill now	bit state
			15	35	10	STROIL SE SE	Internation
Mode Control (S) to Clock			5.0	0	-40	inter division and	ns
Parameter Community			10	0	-27		113
		la constant	15	0	-20		
Reset Removal Time	Leader to a	1	5.0	300	150		
Annual Control of Control of Control		trem	10	110	55	STREET CONTRA	ns
		anastion huses	15	80	40	10 TO 2.00	nov
			10	00	40	The second second	100000

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>\*</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.





MC14415

#### OUAD PRECISION TIMER/DRIVER

The MC14415 quad timer/driver is constructed with complementary MOS enhancement mode devices. The output pulse width of each digital timer is a function of the input clock frequency. Once the proper input sequence is detected the output buffer is set (turned on), and after 100 clock pulses are counted, the output buffer is reset (turned off).

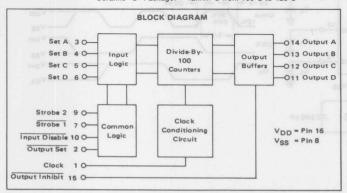
The MC14415 was designed specifically for application in high speed line printers to provide the critical timing of the hammer drivers, but may be used in many applications requiring precision pulse widths.

- Four Precision Digital Time Delays
- Schmitt Trigger Clock Conditioning
- NPN Bipolar Output Drivers
- Timing Disable Capability Using Inhibit Output
- Positive or Negative Edge Strobing on the Inputs
- Synchronous Polynomial Counters Used for Delay Counting
- Power Supply Operating Range
   3.0 Vdc to 18 Vdc (MC14415EFL/FL/FP)
   3.0 Vdc to 6.0 Vdc (MC14415EVL/VL/VP)

MAXIMUM RATINGS\* (Voltages Referenced to Voc.)

Symbol	Parameter	Value	Unit	
V <sub>DD</sub>	DC Supply Voltage - MC14415EFL/FL/FP	-0.5 to +18.0	V	
	MC14415EVL/VL/VP	-0.5 to +6.0		
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V	
lin	Input Current (DC or Transient), per Pin	±10	mA	
lout	Output Current (DC or Transient), per Pin	±20	mA	
PD	Power Dissipation, per Package†	500	mW	
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C	
TL	Lead Temperature (8-Second Soldering)	260	°C	

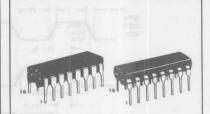
\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C
Ceramic "L" Package: -12mW/°C from 100°C to 125°C



## **CMOS LSI**

(LOW-POWER COMPLEMENTARY MOS)

QUAD PRECISION TIMER/DRIVER



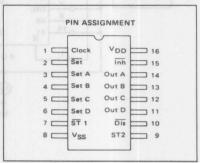
L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

Operating Range: -55°C to +125°C MC14415EFL (3 to 18 V, Ceramic Package) MC14415EVL (3 to 6 V, Ceramic Package)

Operating Range: -40°C to +85°C MC14415FL (3 to 18 V, Ceramic Package) MC14415FP (3 to 18 V, Plastic Package) MC14415VL (3 to 6 V, Ceramic Package) MC14415VP (3 to 6 V, Plastic Package)



EL ECTRICAL	CHARACTERISTICS	(Voltages Referenced to Vec)

starts seal	and a man		1 100	V <sub>DD</sub> T <sub>low</sub> *		25°C		Th				
Characteristic		Symbol	Vdc 5.0	Min	Max 0.01	Min	Typ#	Max	Min	Max	Unit	
Output Voltage "0" Level				-			0	0.01	4 (2)	0.05	Vdc	
(No Load)			OL.	10	-	0.01	-	0	0.01	3-196	0.05	24.473
			1 81	15	-	-	-	-	-in C	(3-19u)	n 0-11 -	84_EES
	"1"	Level	VOH	5.0	-		3.0	4.14	-	-	ment the	Vdc
			0.8	10	-	-	8.0	9.09	-50.57	0 (3)	Non-Series	16277
			es l	15	-	-	-	14.12	- 15	13-23-01	in di-cit	10000
Noise Immunity		VNL						46.37	33136	H-45-01-	Vdc	
(△Vout ≤ 1.5 Vdc)			1	5.0	1.5	-	1.5	2.25	-	1.4	WY who	Mo-mm
(△Vout ≤ 3.0 Vdc)			0.0	10	3.0	-	3.0	4.50	-1700	2.9	hin 122 mel	HERE
(△V <sub>out</sub> ≤ 4.5 Vdc)			de	15	-	-	-	6.75	- 10	1 213	San (2-1)	114997
(△V <sub>out</sub> ≤ 1.5 Vdc)			VNH	5.0	1.4	_	1.5	2.25	15.850	1.5	10 3 1 <u>2</u> 101 3	Vdc
(△V <sub>OU1</sub> ≤ 3.0 Vdc)			- No.	10	2.9	-	3.0	4.50	-	3.0	MIT HONO	att mile
(△V <sub>out</sub> ≤ 4.5 Vdc)			0.0	15	-	_	-	6.75	+1700	1 313	Non-E-17	534197
Output Drive Voltage (NPN Driver)			VOH						\$1.00	7.3919	14n Q.11 F	Vdc
(IOH = 0 mA)	Sou		OH	5.0		_	3.0	4.14	THE COLD	102174	10 GT_0)	JIME!
(IOH = 5.0 mA)				440	-	_	2.7	3.44	mul-D ou		self water	nD-nur
(IOH = 10 mA			0.8		-	_	2.5	3.30	_	_	-	
(I <sub>OH</sub> = 15 mA)			01		-	_	2.2	3.08	-	-	-	
(IOH = 0 mA)			at i	10	-	-	8.0	9.09	_	-	-	Vdc
(IOH = 5.0 mA)			-	-	-	_	7.7	8.45	to Certura	00200	AT - NO	Pi C-m
(IOH = 10 mA)			6.0		-	-	7.5	8.30	_	-	_	
(IOH = 15 mA)			0.0		-	-	7.1	8.14	_	-	_	
(I <sub>OH</sub> = 0 mA)			80	15	_	-	-	14.12	-	_	-	Vdc
(IOH = 5.0 mA)					13 - T	-	-	13.81	-10	OTHER DESIGNATION OF THE PERSON  -10	of me	
(IOH = 10 mA)			0.3		_	_	_	13.70	-	_	_	
(IOH = 15 mA)			1 01		-	-	-	13.61	-	-	-	
Output Drive Current		-	loL									mAd
(VOL = 0.4 Vdc)	Sinl	k		5.0	0.23	-	0.20	0.78	-	0.16	rate-A se	LUFT EURO
(VOL = 0.5 Vdc)		808	E.o.a.	10	0.60	-	0.50	2.0	_	0.40	-	
(VOL = 1.5 Vdc)		000	.01	15	-	-	-	7.8	-	-	-	
Input Leakage Current		1 -	lin	15	-	±0.3	-	± 0.00001	±0.3	-	±1.0	μAdo
Input Capacitance (Vin = 0)	7.0		Cin	- 1	-	-	-	5.0	-	- 401	1555=1 /S	pF
Quiescent Dissipation	1.0 10E		Pa	5.0		0.25		0.00005	0.25	_	3.5	mW
			7 78	10	0.172	1.0		0.00003	1.0	7 Hz 2 h	14	and street
		1 - 1	OF.	15	-	-	-	0.00022	-	-	-	
Power Dissipation **		PD	-	- In-		-			THE RESERVE OF		mW	
(Dynamic plus Quiescent) (C <sub>L</sub> = 15 pF)			5.0	P <sub>D</sub> = (56 mW/MHz) f + P <sub>Q</sub>						31 40 10 R ps (m-151 3.2)		
*T <sub>IOW</sub> = -55 <sup>O</sup> C for MC14415EFL, EVL				10 15	$P_D = (225 \text{ mW/MHz}) f + P_Q$ $P_D = (510 \text{ mW/MHz}) f + P_Q$						tenberge	

 $<sup>^{\</sup>circ}$ Tlow = -55 $^{\circ}$ C for MC14415EFL, EVL; -40 $^{\circ}$ C for MC14415FL,FP,VL,VP Thigh= +125 $^{\circ}$ C for MC14415EFL,EVL; +85 $^{\circ}$ C for MC14415FL,FP,VL,VP

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

<sup>\*\*</sup>The formulas given are for the typical characteristics only.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

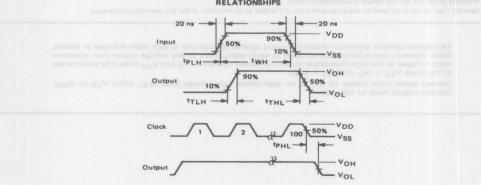
SWITCHING CHARACTERISTICS\* (C1 = 15 pF, TA = 25°C)

Characterist	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit			
Output Rise Time	tTLH	- Williams		31001.0					
tTI H = (2.0 ns/pF) C1 + 10 ns				- 1 03	5.0	in James	40	85	oV high
tTI H = (1.25 ns/pF) CI + 6 ns				- 1 61	10	-	25	60	out all it
tTLH = (1.10 ns/pF) CL + 3 ns				- 1 81	15	-	20	-	
Output Fall Time	21.5	0.01		tTHL	ноч	1695.	-		ns
tTHL = (1.5 ns/pF) CL + 47 ns				- 01	5.0	-	70	150	
tTHI = (0.75 ns/pF) C1 + 24 ns				15.	10	-	35	80	
tTHL = (0.55 ns/pF) CL + 17 ns					15	-	25	Ty Field	coret su
Turn-Off Delay Time	2.25	23		tPLH				nv 6.1 a	ns
tpl H = (2.7 ns/pF) C1 + 560 ns				9.6 91	5.0	-	600	1200	min Vel
tpHL = (1.2 ns/pF) CL + 282 ns				- 31	10	-	300	600	Con Val
tpLH = (0.91 ns/pF) CL + 286 ns				3.7 8.8	15	-	150	09712	www.viery
Turn-On Delay Time	02.6	0.8	8 9	tPHL				5V 9.83	ns
tpHL = (2.4 ns/pF) CL + 564 ns				- at	5.0	-	600	1200	sonV41
tpHL = (1.0 ns/pF) CL + 285 ns					10	- (40	300	600	10 hear
tpHL = (0.75 ns/pF) CL + 289 ns				- 9.8	15	-	150	The section	Titaniii.
Turn-On Delay Time (Inhibit to Output)	3.64	1.5	H- SA 1	tPHL				(Aun Ba	ns
					5.0	-	300	550	Frenti
					10	-	225	425	* (10)
				- 1 01	15	-	110	the mile	HOU
Turn-Off Delay Time (Inhibit to Output)	85.8	4.7		tPLH				1Am 02	ns
					5.0	-	300	550	- HOT
					10	-	225	425	× HQD
					15	-	110	Hand	P Holl
Input Pulse Coincidence (Figure 3)	19.01	191		PCmin				(Am 0.2	ns
					5.0	500	450	(84m (0)	ROH
					10	450	350	IAm al	FEIGH
shAm					15	-	-	1192 <del>15</del> () 98	eQ requiper
Input Pulse Width (Figure 1)		05.0		tWH			SHIE	059 HD	ns
				08.0 01	5.0	500	450	0.69 (0.0)	10A1
				- 11	10	450	350	DOY THE	- 10p)
55A1 9.5 - E.O. 1	6000.01		102	- 81	15	-	- 1	- ( <del>-)</del> - 10	franch tro
Input Clock Frequency	9.8			fcl	160	11-11		sone fit	MHz
					5.0	- 1	0.7	-	P- mV
					10	-	1.0	out the same	mages
1 00 - 1 000 1	0,0000		75.6	5.0	15	_	1.5	-	
Clock Input Rise and Fall Times (Figure		1.0	tTLH, tTHL	5.0	-	-	15	μs	
				- 1 81	10	-	-	5.0	
				and the distance of the	15	1	_	4.0	

\*The formulas given are for the typical characteristics only at 25°C.

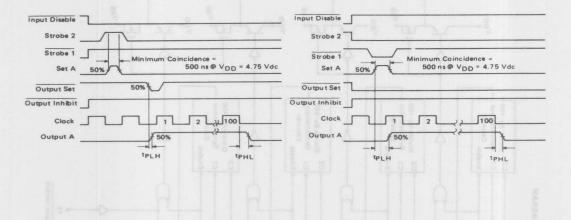
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# FIGURE 1 – SWITCHING CHARACTERISTICS – WAVEFORM RELATIONSHIPS



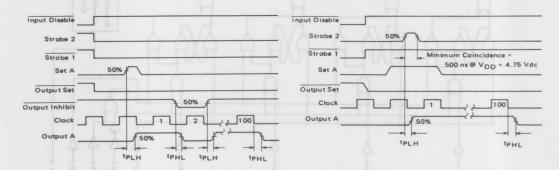
MODE 1 - OUTPUT SET INITIATES TIME DELAY

#### MODE 2 : SET A INITIATES TIME DELAY

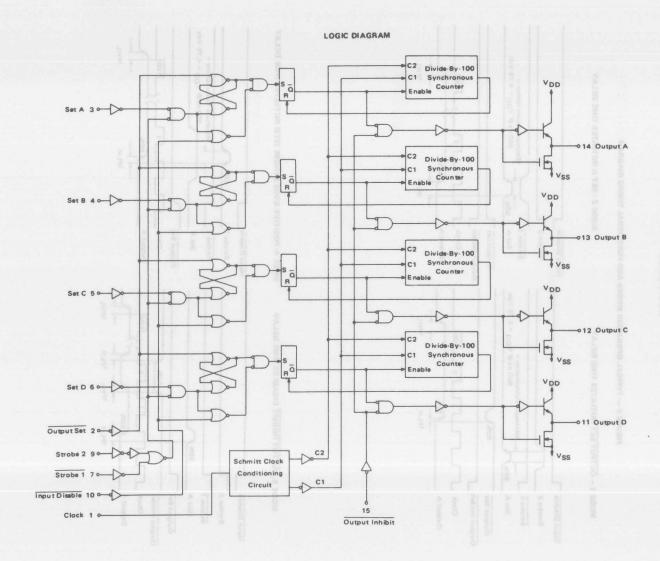


#### MODE 3: OUTPUT INHIBIT DISABLES TIME DELAY

#### MODE 4: POSITIVE-EDGE STROBE (ST2) INITIATES TIME DELAY



6-218





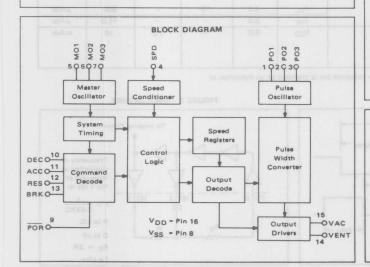
### AUTOMOTIVE SPEED CONTROL PROCESSOR

The MC14460 device is designed to measure vehicle speed and provide pulse-width modulated outputs to trim a throttle positioning servo to maintain an internally stored reference speed.

The stored reference speed can be altered by the DECEL and ACCEL driver commands. The DECEL command trims down the speed, while ACCEL trims up the speed.

A BRAKE input is provided to turn off the outputs with a RESUME driver command to return the vehicle to the last stored speed.

- On-Chip Master Oscillator for System Time Reference
- Separate On-Chip Pulse Oscillator for Output Pulse Width Adjustment (Analogous to System Gain)
- Diode Protection on All Inputs
- Internal Redundant Brake and Minimum Speed Checks
- Acceleration Rates Controlled During ACCEL and RESUME Modes of Operation
- Low Frequency Speed Sensors Used
- No Throttle Position Feedback Required
- Power-On Reset
- Buffered Outputs Compatible with Discrete Transistor
   Driver Interface
- Low Power Dissipation
- Operating Temperature Range: -40° to +85°C



### **CMOS LSI**

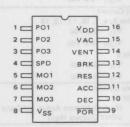
(LOW-POWER COMPLEMENTARY MOS)

AUTOMOTIVE SPEED CONTROL PROCESSOR



P SUFFIX
PLASTIC PACKAGE
CASE 648

#### PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

~

# MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +6.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

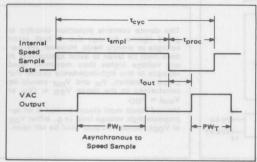
\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: -12mW/°C from 65°C to 85°C

# ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>, T<sub>A</sub> = -40°C to +85°C)

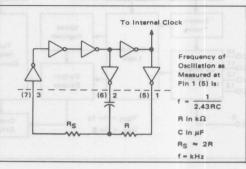
Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Supply Voltage Pin 16	V <sub>DD</sub>	nio l=sm	4.0	5.0	6.0	Vdc
Output Voltage	VOL	5.0	to mut of be	ls onovide	0.5	Vdc
Pins 1, 2, 5, 6, 14, 15	VOH	5.0	4.5	of brief	man Telab	Vdc
Input Voltage	VIL	-	-	-	0.3 V <sub>DD</sub>	Vdc
Pins 3, 7, 9, 10, 11, 12, 13	VIH	January Thank	0.7 V <sub>DD</sub>	and the same	Character St. of	Vdc
Pin 4	VIL	N 2014 3 71	V <sub>DD</sub> -1.5	lisa ( <del>)</del> salu	gidO+rO ar	Vdc
WHRUS 4	VIH	-	- 4	ugnt-liA n	V <sub>DD</sub> +1.5	Vdc
Input Hysteresis	HYS	loor(C+bes	0.4	ns s <del>t</del> arti )	is Bu + rodes	Vdc
Pin 4 (V <sub>IH</sub> - V <sub>IL</sub> )	эмиа	IR Line 13	DOA sning ACC	Controlle	eseR solser	Book: I
Output Drive Current					1300-7 11 500	
Pins 1, 2, 5, 6 V <sub>OH</sub> = 4.6 Vdc			0.00		og vandmings	wo.J.
V <sub>OL</sub> = 0.4 Vdc	ГОН	5.0	-0.29	-	-	mAdo
Pins 14, 15	lor	5.0	+0.36	-	-	mAdo
V <sub>OH</sub> = 2.5 Vdc	ГОН	5.0	-2.0			mAdo
Input Current		PARAMETER.		United the		
Pins 3, 4, 7, 10, 11, 12, 13					1061 101H 101	
VIL - 0.0 Vac	IIL	6.0	-	-noit	-1.0	μAdc
VOH - 0.0 Vdc	ПН	6.0	NI TON	non-El ma	+1.0	μAdc
Pin 9 V <sub>II</sub> = 0.0 Vdc			45			
V <sub>IH</sub> = 6.0 Vdc	IL	6.0	15	_	200	μAdc
11 010 100	11н	6.0	-	-	+1.0	μAdc
Pin 16 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	IDD	6.0	-	1.0	10	mAdo
(Both Oscillators Active, VAC and VENT Outputs High)	2.3	2			1 2 3	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# FIGURE 1 - SYSTEM TIMING



# FIGURE 2 - OSCILLATORS



SWITCHING CHARACTERISTICS (TA = 25°C, VDD = 4-6 Vdc)

Characteristics	Symbol	Min	Тур	Max	Unit
ACCEL Input Hold Time	tACC	16/f <sub>M</sub>	9.52*	0 - 1	ms
DECEL Input Hold Time	†DEC	16/f <sub>M</sub>	9.52°	- 1	ms
RESUME Input Hold Time	tRES	danax.	300 - 00 P	Sac Sac	μs
BRAKE Input Hold Time	†BRK	1	-	W- 1	μs
Master Oscillator Frequency (Figure 2)  T <sub>A</sub> = -40°C to +85°C, R <sub>S</sub> = 100 kΩ  R = 43 kΩ, C = 5600 pF  Useful Range	fM	1596 1344	1680 1680	1764 2016	Hz Hz
Pulse Oscillator Frequency (Figure 2)  T <sub>A</sub> = -40°C to +85°C, R <sub>S</sub> = 100 kΩ  R = 43 kΩ, C = 5600 pF  Useful Range	fp	1596 400	1680 1600	1764 3200	Hz Hz
Speed Input Frequency	fs	-	- 1	300	Hz
Speed Sample Time (1008/f <sub>M</sub> )	tsmpl	K toward	600°	TVM = WI	ms
Speed Processing Time (16/f <sub>M</sub> )	tproc	-	8.9*	1000 -	ms
System Cycle Time (1024/f <sub>M</sub> )	tcyc	12	608.9*	A -	ms
Output Delay Time (9/f <sub>M</sub> )	tout	rate distant	5.4*		ms
Output Pulse Width Initializations (≈ 1/f p) Trim Outputs (≈ 1/f p)	PW <sub>I</sub> PW <sub>T</sub>	280° 10°	a) b	760° 80°	ms ms

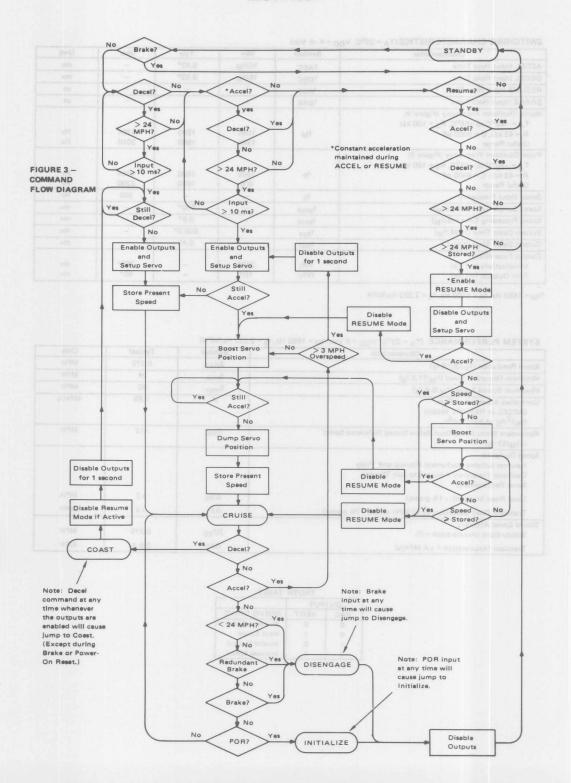
<sup>\*</sup>fM = 1680 Hz, fp = 1600 Hz, fs = 2.222 Hz/MPH

SYSTEM PERFORMANCE (TA = 25°C, VDD = 5 Vdc, fM = 1680 Hz, fs = 2,222 Hz/MPH)

Characteristic	Symbol	Typical	Unit
Speed Resolution (f <sub>M</sub> /2016 f <sub>S</sub> )	SRES	0.375	MPH
Minimum Operating Speed (f <sub>M</sub> /31.5 f <sub>S</sub> )	S <sub>min</sub>	24	MPH
Maximum Stored Speed (f <sub>M</sub> /8.4 f <sub>S</sub> )	S <sub>max</sub>	90	MPH
Controlled Acceleration Rate (ACCEL or RESUME Modes) (f <sub>M</sub> ) <sup>2</sup> /f <sub>S</sub> (6.881) (10 <sup>5</sup> )	A	1.85	MPH/s
Redundant Brake Speed Drop Below Stored Reference Speed (-f <sub>M</sub> /63 f <sub>S</sub> )	S <sub>RB</sub>	-12	МРН
Speed Deviation			
Assumes Suitable Mechanical Hookup and Pulse Oscillator Frequency Adjusted to Suit Throttle Servo Requirements	104min.may2 500min		Dieldseig : w. 1 kg/
Level Road (no wind, ± 1% grades)	ΔSN	±2	MPH
Transient Road Conditions (± 10 MPH winds, ± 7% grades)	ΔST	±3	MPH
Stored Speed Accuracy	The same of the sa	No. of the second	
Steady-State (Acceleration = 0)	RSSS	0.375	MPH
Transient (Acceleration = ± A MPH/s)	RST	0.6 A	MPH

TRUTH TABLE

OUT	PUT	
VAC	VENT	SERVO DRIVE
0 0		Decrease Speed
0	1	Hold Speed
1	0	Invalid Output
1	1	Increase Speed



# DEVICE OPERATION

# PULSE OSCILLATOR (PO1 PO2 PO3 Pins 1 2 3)

These pins are the output pins of the output Pulse Oscillator, which is a three-terminal RC type. See Figure 2 for design parameters. This oscillator sets the relative pulse width of the VAC and VENT outputs.

### SPEED (SPD Pin 4)

This is the Speed input to be controlled or stored. This input is level sensitive with hysteresis to allow use of slowly changing waveforms. Input frequency should never exceed 1/3 the Master Oscillator frequency (fm).

# MASTER OSCILLATOR (MO1, MO2, MO3; Pins 5, 6, 7)

The Master Oscillator is a three-terminal RC type. See Figure 2 for design parameters. This oscillator sets the master system timing.

### POWER-ON RESET (POR Pin 9)

This pin is the Power-On Reset input. As long as this input is LOW, the internal system is cleared and the VAC and VENT outputs are disabled. An internal pullup device will source 15-200 µAdc of current from this pin to allow capacitor charging for automatic power-on reset.

FIGURE 4 - TYPICAL AUTOMOTIVE CRUISE CONTROL APPLICATION

# DECEL (DEC Pin 10)

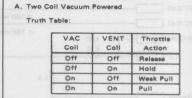
This is the DECEL command input. When held HIGH both VAC and VENT outputs will be LOW. When the DECEL input returns LOW the last sample of the SPD input will be stored as the reference speed. The flow disgram in Figure 3 gives the detailed constraints/operation of this input.

### ACCEL (ACC Pin 11)

This is the ACCEL command input. When held HIGH the VAC and VENT outputs will be modulated to maintain a fixed rate of acceleration. When the ACCEL input returns LOW the last sample of the SPD input will be stored as the reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

continued

### THROTTLE SERVO



### B. Coil Type

Coil Inductance: 125-150 mH

### C Servo Response

Poles:

Output Freq:

Output Voltage:

Maximum Freq:

DC Resistance:

Minimum Pulse Width: 5 ms Throttle Travel: 50-60° full travel Throttle Response 300/s Pull @ 7" VAC

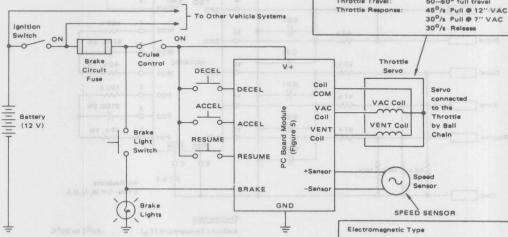
8/revolution

< 40 O

2.222 Hz/MPH (8000 pulses/mile)

> 3.0 Vp-p @ 24 MPH

360 Hz (162 MPH)



### DEVICE OPERATION continued

# RESUME (RES, Pin 12)

This is the RESUME command input. When taken HIGH the system will lock into a mode where the VAC and VENT outputs are modulated to maintain a fixed rate acceleration. This acceleration ends when the SPD input sample matches the stored reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

# BRAKE (BRK, Pin 13)

This is the BRAKE command input. When this input is taken HIGH the system is disabled (both VAC and VENT outputs LOW) until a DECEL, ACCEL, or RESUME com-

mand is received. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

# VENT (Pin 14) and to anisy function and anisy sent

This is the VENT output. See Truth Table for operation.

### VAC (Pin 15)

This is the VAC output. See Truth Table for operation.

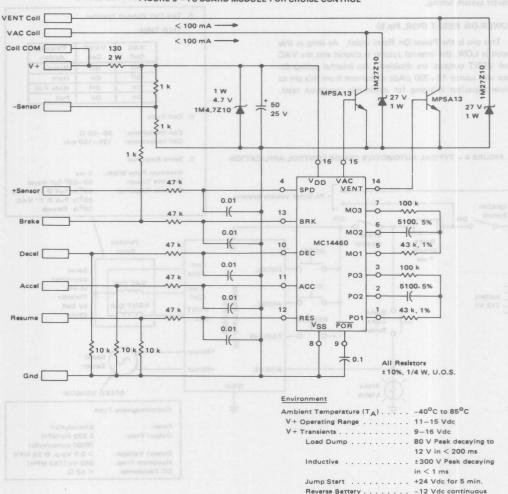
# GROUND (VSS, Pin 8)

Pin 8 is the ground connection for the package.

# POSITIVE POWER SUPPLY (VDD, Pin 16)

Pin 16 is the power supply connection for the package.

# FIGURE 5 - PC BOARD MODULE FOR CRUISE CONTROL





# HEX CONTACT BOUNCE ELIMINATOR

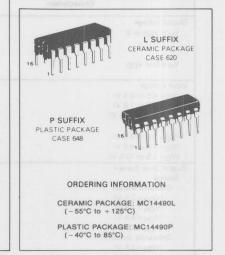
The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490 (see Figure 5).

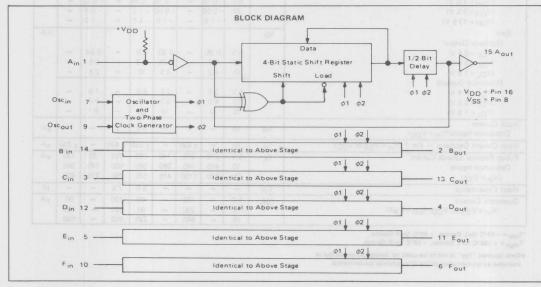
- Diode Protection on All Inputs
- Six Debouncers Per Package
- Internal Pullups on All Data Inputs
- Can Be Used as a Digital Integrator, System Synchronizer, or Delay Line
- Internal Oscillator (R-C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both "Make" and "Break" Contacts
- Does Not Require "Form C" (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 V to 18 V
- Chip Complexity: 546 FETs or 136.5 Equivalent Gates

# CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

HEX CONTACT BOUNCE ELIMINATOR





# MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin	Input Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

# PIN ASSIGNMENT

A <sub>in</sub>	91	16	VDD
Bout	2	15	A <sub>out</sub>
C <sub>in</sub>	13	14	Bin
D <sub>out</sub>	04		Cout
E <sub>in</sub>	<b>C</b> 5	12	Din
Fout	6	11	Eout
v prior Osc <sub>in</sub>		10	Fin
VSS	8	9	Oscou

# ELECTRICAL CHARACTERISTICS (Voltages Referenced to Vss)

Characteristic	SV	mbol	VDD	Tio	w°	100 TO	25°C	laure	This	gh <sup>*</sup>	Uni
Characteristic	34	111001	Vdc	Min	Max	Min	Тур#.	Max	Min	Max	On
Output Voltage "0" L	evel V	OL	50	496	0.05	ou-o	0	0 05	on-to-	0.05	V
$V_{in} = V_{DD}$ or 0	froms to		10	inst- in	0 05	02-13	0	0.05	- 0	0 05	
	199		15	-	0.05	-	0	0.05	7.00	0.05	
"I" I BETTER TO THE CHANG PACKAGE	evel V	ОН	50	4 95	-	4 95	50	-	4 95	-	V
$V_{ID} = 0$ or $V_{DD}$		0,1,1	10	9 95	_	9 95	10		9 95	9 7 10	
	7.4		15	14 95	-	14 95	15	-	14 95	_	
Input Voltage "0" L	_evel \	/11									V
(VO = 4.5 or 0.5 V)			50		15	Seding R	2 25	15	abiso 3	15	al s
	BO IN M		10	metas	30	6110911	4 50	30	turil	30	0.4
$(V_0 = 13.5 \text{ or } 1.5 \text{ V})$			15	_	40	_	6 75	40	_	40	1
	evel \	/IH	92700	1 11900	O Servi	erika a	10	57 108	HII-O-CA	160 00	V
	-CVCI V	ПН	50	3.5	21-11	35	2 75	-	3.5		
(Vo = 1.0 or 0.0 V)			10	70	-	70	5.50	A13.7 194	70	03 J	T
$(V_0 = 1.5 \text{ or } 13.5 \text{ V})$	DESTRUCTION OF THE PROPERTY OF		15	110	17 7125	110	8 25	O Jan	11 0	J e gn	2.1
	4 10 2 10	your!	15	110	- oles	3110	0 23	anio	110	91 100	9.
Output Drive Current Source	10	ОН								1600	mA
					SVB	HIT AN	LET THE	ino.J	er end	Line yes	500
Oscillator Output			5.0	0.0		100					2
(V <sub>OH</sub> = 2.5 V)	APOLICE TO		50	-06	= 19	0.5	100000000000000000000000000000000000000	D= 10	0 4	III-	8.4
$(V_{OH} = 4.6 \text{ V})$			50	- 0 12	VBI	-01	-03	dun e	- 0 08	VICION	2 4
$(V_{OH} = 9.5 \text{ V})$			10	- 0 23	3 7 18	- 0 20	7.11.1929	SE VIII	- 0 16	1 m	6 1
(V <sub>OH</sub> = 13.5 V)	F. Lug		15	- 1 4	-	- 12	- 30	-	-10	_	
Debounce Outputs											
(V <sub>OH</sub> = 2.5 V)			50	-09	-	- 0 75		-	-06	-	
(V <sub>OH</sub> = 4.6 V)			50	- 0 19		- 0 16		-	- 0 12	-	
$(V_{OH} = 9.5 \text{ V})$	MARBAI		10	- 0 60	-	- 0 50		-	-04	-	
(V <sub>OH</sub> = 13.5 V)	THE REAL PROPERTY.		15	-18	-	- 15	-45	-	- 12	-	
Sink	1	OL		11111111			1 12				mA
Oscillator Output							12 3			P. 9 E.	
(V <sub>OL</sub> = 0.4 V)	9		50	0 36		0 30	09	-	0 24	-	
(V <sub>OL</sub> = 0.5 V)	2012/11/2		10	0.9	-	0 75	23	-	06	m =	
$(V_{OL} = 1.5 \text{ V})$	electric.		15	42	-	35	10	-	28	-	
Debounce Outputs			7								
(V <sub>OL</sub> = 0.4 V)			50	26	-	22	40	_	18	_	
$(V_{OL} = 0.5 \text{ V})$	4-1		10	40	-	33	9	- 10	27	-130	a .
$(V_{OL} = 1.5 \text{ V})$			15	12	-	10	35	-	81	_	
Input Current			15		2	1000	0.0	-			
Debounce Inputs (V <sub>In</sub> = V <sub>DD</sub> )		IH	15	-	2	HOZAN	02	2	- 8	110	μΔ
Input Current Oscillator - Pin 7 (Vin = VSS or VDD)		l <sub>in</sub>	15	-	± 620	-	± 255	± 400	-	± 250	μΔ
Pullup Resistor Source Current	The state of the s	l <sub>II</sub>	5.0	210	375	140	190	255	70	130	μA
Debounce Inputs			10	415	740	280	380	500	145	265	
$(V_{in} = V_{SS})$	91.010		15	610	1100	415	570	750	215	400	
Input Capacitance	(	Cin	-	-	-	-	50	7.5	-	-	pF
Quiescent Current	-	SS	50	-	150	_	40	100	-	90	μА
$(V_{ID} = V_{SS} \text{ or } V_{DD}, I_{Out} = 0 \mu A)$	0000	55	10	HOL			90				μ
. III . 32 or 4DD' , OUT - 0 12-1			15		280	-		225		180	
the state of the s		Low	15	-	840	-	225	650	-	550	

 $^*T_{\mbox{low}} = -55^{\circ}\mbox{C}$  for L Device,  $-40^{\circ}\mbox{C}$  for P Device.  $T_{\mbox{high}} = +125^{\circ}\mbox{C}$  for L Device,  $+85^{\circ}\mbox{C}$  for P Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS (C) = 50 pF, TA = 25°C)

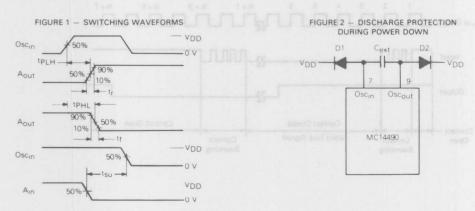
Characteristic	villanced at the	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise Time I come and a small a second and a second a second and	bas qui alod i	reaguleri	5.0	10/40	180	360	ns
All Outputs data and appropriate from the former of the first section of		ITLH	10	in with	90	180	EMIT
		rla Jenga	15	deplo	65	130	DAID
Output Fall Time					L BANG	17.10	ns
Oscillator Output		THL	50	900	100	200	10.0
		d significant	10	Ursage	50	100	Barton I
		ethoet s	15	9.40	40	80	Olly
Debounce Outputs and an langua success and principles A		THL	5.0	107-10	60	120	TIM
		loss oin	10	: Hig	30	60	01.19
longer or shorter than the clean mous signal plus or minus	ens Henrick D	the stort	15	U.T	20	40	T. FR
Propagation Delay Time		tPHL 1		V890	BOOM !	est m	ns
Oscillator Input to Debounce Outputs		miles es	5.0	iuano	285	570	BORDH
		DOOR REW	10	B quil	120	240	Ham
		second of	15	INT. I	95	190	Lug I
		tPLH	5.0	25-10	370	740	gni t
		DINUGIACIO D	10	1148	160	320	q bni
		rie ou rich	15	41711	120	240	Supp
Clock Frequency (50% Duty Cycle)	di Steletico eve	t <sub>Cl</sub>	5.0	Hev	2.8	1.4	MHz
(External Clock) lample hugon and pasts estimate and law lample		aharin ti	10	0.5	6	30	goin !
		TSWING 5	15	nte a	9	4.5	nom
Setup Time (See Figure 1): One state of the setup time (See Figure	right self they	t <sub>su</sub>	5.0	100	50	ities i	ns
		straul ar	10	80	40	s ,bor	leval:
		o T lon	15	60	30	09-00	teger
Maximum External Clock Input	babuol and 160	tr. tr	5.0	e)iri	N BEST	202 0	ns
Rise and Fall Time		. level r	10	s ar tr	No Limi	not be	6 8145
Oscillator Input of Ferop call for Alexin it replace as and savet		e sarting	15	18 01			-floats
Oscillator Frequency Note: These equations are intended to be	a design guide.	fosc, typ	1 1011	erb o	1.5		Hz
OSC <sub>out</sub> Laboratory experimentation may be require	ed. Formulas	rgt-e avri	5.0	C.	ext (in p	(F)	PH H
C <sub>ext</sub> ≥ 100 pF* are typically ± 15% of actual frequencies.		T right		100 6	4.5		Signal
part (gin 7). However if an extrenal clock is not available the		and sugs 4	10	C	ext (in /		nd argi
				TRVG	6.5	and but	mil +
		d Jengse d	15	-		F) 100	12.00
		de nooi h	s other	C,	ext (in #	111	000

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

### \*POWER-DOWN CONSIDERATIONS

Large values of Cext may cause problems when powering down the MC14490 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge through the input protection diodes at Pin 7 or the parasitic diodes at Pin 9. Current through these internal diodes must be limited to 10 mA, therefore the turn-off time of the power supply must not be faster than t =  $(V_{DD} - V_{SS}) + C_{ext}/(10 \text{ mA})$ . For example, if  $V_{DD} - V_{SS} = 15 \text{ V}$  and  $C_{ext} = 1 \mu F$ , the power supply must turn off no faster than t = (15 V) •(1 µF)/10 mA = 1.5 ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate When a more rapid decrease of the power supply to zero volts occurs, the MC14490 may sustain damage. To avoid this possibility, use exter-

nal clamping diodes, D1 and D2, connected as shown in Figure 2.



<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a 41/2-bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is open, (see Figure 4) the high level is inverted, and the shift register is loaded with a low on each negative edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with lows and the output is at a high level.

At clock edge 1 (Figure 3) the input has gone low and a high has been loaded into the first bit or storage location of the shift register. Just after the negative edge of clock 1, the input signal has bounced back to a high. This causes the shift register to be reset to lows in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus, a high has been shifted into all four shift register bits and, as shown, the output goes low during the positive edge of clock pulse 6.

It should be noted that there is a 3% to 4% clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at N+1 a low is loaded into the first bit. Just after N+1, when the input bounces low, all bits are set to a high. At N+2 nothing happens because the input and output are low and all bits of the shift register are high. At time N+3 and thereafter the input signal is a high, clean signal. At the positive edge of N+6 the output goes high as a result of four lows being shifted into the shift register.

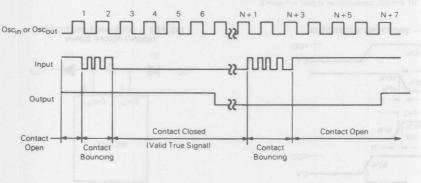
Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

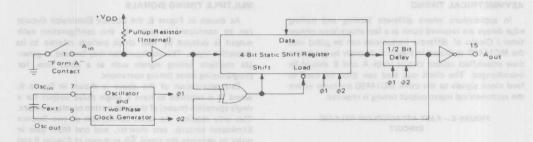
The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if the leading edge bounce is included in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.







### OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B)  $\,$ 

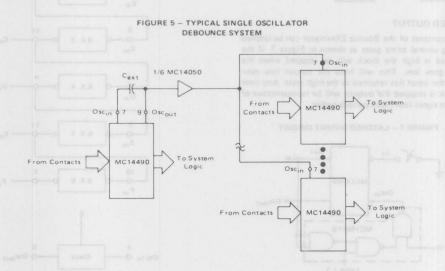
The circuit has a built in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between VDD and the input

Because of the built-in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when V<sub>DD</sub> is below 5 V. At this voltage, the input should be driven with

paralleled standard gates or by the MC14049 or MC14050 buffers

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5). Up to six MC14490s may be driven by a single buffer.

The MC14490 is TTL compatible on both the inputs and the outputs. When VDD is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

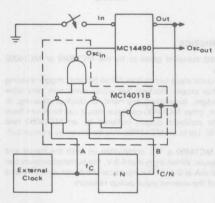


# TYPICAL APPLICATIONS

### ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads. A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

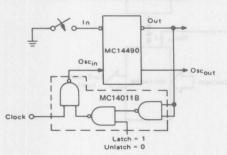
FIGURE 6 - FAST ATTACK/SLOW RELEASE CIRCUIT



# LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

FIGURE 7 - LATCHED OUTPUT CIRCUIT

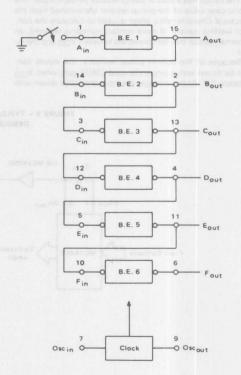


### **MULTIPLE TIMING SIGNALS**

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal  $\overline{A}B$  as shown in Figures 9 and 10. The signal  $\overline{A}B$  is four clock periods in length. If the inverter is switched to the A output, the pulse  $\overline{A}B$  will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

FIGURE 8 - MULTIPLE TIMING CIRCUIT CONNECTIONS



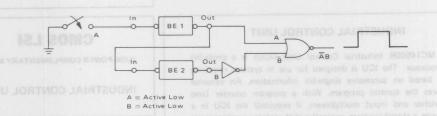
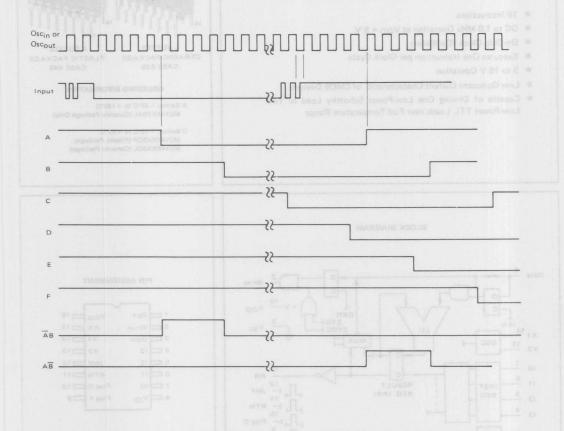


FIGURE 10 - MULTIPLE OUTPUT SIGNAL TIMING DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



MC14500B

# INDUSTRIAL CONTROL UNIT

The MC14500B Industrial Control Unit (ICU) is a single-bit CMOS processor. The ICU is designed for use in systems requiring decisions based on successive single-bit information. An external ROM stores the control program. With a program counter (and output latches and input multiplexers, if required) the ICU in a system forms a stored-program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control. The ICU also may control an MPU or be controlled by an MPU.

- 16 Instructions
- DC to 1.0 MHz Operation at VDD = 5 V
- On-Chip Clock (Oscillator)
- Executes One Instruction per Clock Cycle
- 3 to 18 V Operation
- Low Quiescent Current Characteristic of CMOS Devices
- Capable of Driving One Low-Power Schottky Load or Two Low-Power TTL Loads over Full Temperature Range

# **CMOS LSI**

(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL CONTROL UNIT



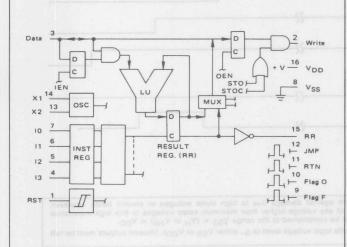
CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

### ORDERING INFORMATION

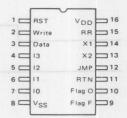
A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

# BLOCK DIAGRAM



### PIN ASSIGNMENT



Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin. lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

### ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

				VDD	Tlo	w		25°C		Thi	gh*	
Characteristic			Symbol	V	Min	Max	Min	Тур#	Max	Min	Max	Uni
Output Voltage	03	"0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	V
Vin = VDD or 0			.02	10	_	0.05	-	0	0.05	-	0.05	1000
· III · DD · · ·			T T	15	_	0.05	-The	0	0.05	The latest	0.05	CHE
V <sub>in</sub> = 0 or V <sub>DD</sub>		"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95	-Tuni	V
AIN - O OL ADD		Level	VOH	10	9.95	_	9.95	10		9.95	creat	0.10
				15	14.95	923144	14.95	15	- Suive	14.95	0055	Fund?
Input Voltage "0" Level		V	10	11.00	SUCKE.	NAME OF THE	1.07951	SSIVEG	LE 101.1	GS ( + -	V	
RST, D, X2		O Level	VIL		M 255 PC			rio Isbiri		-ora miss		1 38
$(V_0 = 4.5 \text{ or } 0.5 \text{ V})$			shot on or	5.0	hi si todi	1.5	Delegh.	2.25	1.5	og b	1.5	ning
(VO = 9.0 or 1.0 V)				10	_	3.0	_	4.50	3.0	atheg to	3.0	(7) or
				15	-	4.0	S	6.75	4.0		4.0	-
		"1" Level	VIH	100	875.000		1 2		tot Date		a la la la la la la la la la la la la la	111
$(V_0 = 0.5 \text{ or } 4.5 \text{ V})$		I Level	VIH	5.0	3.5		3.5	2.75	mail for	3.5		
$(V_0 = 1.0 \text{ or } 9.0 \text{ V})$				10	7.0	_	7.0	5.50	_	7.0	_	
(V <sub>O</sub> = 1.5 or 13.5 V)				15	11.0	Stuyit	11.0	8.25	pozine	11.0	_	
Input Voltage #	635	"0" Level	VIL	-		211		0.23	-		OIL S	V
10, 11, 12, 13		O Level	VIL	OI.	1 1		3					V
(V <sub>O</sub> = 4.5 or 0.5 V)				5.0	1 _ 1	0.8	_	1.1	0.8	_	0.8	
$(V_0 = 9.0 \text{ or } 1.0 \text{ V})$				10		1.6		2.2	1.6	Flag O.1	1.6	\$1 FX
(VO = 13.5 or 1.5 V)				15		2.4		3.4	2.4		2.4	
(*0 - 15.5 61 1.5 */		"1" Level	\/	13		2.7		5.4	6.7			-
(V <sub>O</sub> = 0.5 or 4.5 V)		1 Level	VIH	5.0	2.0	129	2.0	1.9		2.0	SELVEN	11 730
				10	-			3.1		6.0		
(V <sub>O</sub> = 1.0 or 9.0 V)				15	6.0	-	6.0	1977			-	
(V <sub>O</sub> = 1.5 or 13.5 V)	051			15	10	_	10	4.3		10	E-110	11.408
Output Drive Current		Source	ІОН	.81								m/
Data, Write (AL/CL/CP Device)				0.3.							88.6	139
(V <sub>OH</sub> = 4.6 V)				5.0	-1.2	-	-1.0	-2.0	-	-0.7		
(V <sub>OH</sub> = 9.5 V)				10	-3.6	-	-3.0	-6.0	-	-2.1	-	
(V <sub>OH</sub> = 13.5 V)				15	-7.2	-	-6.0	-12	_	-4.2		725
(V <sub>OL</sub> = 0.4 V)		Sink	IOL	5.0	1.9	4 -	1.6	3.2	-	1.1	-	
(V <sub>OL</sub> = 0.5 V)				10	3.6	-	3.0	6.0	-	2.1	-	
(V <sub>OL</sub> = 1.5 V)	0.09-			15	7.2	-	6.0	12	-	4.2	Topic o	TSA
Output Drive Current		Source	ІОН	01								m
Other Outputs (AL Device)												
(V <sub>OH</sub> = 2.5 V)				5.0	-3.0	_	-2.4	-4.2	_	-1.7	SELLEN O	干奇形
(V <sub>OH</sub> = 4.6 V)				5.0	-0.64	-	-0.51	-0.88		-0.36	-	
(V <sub>OH</sub> = 9.5 V)				10	-1.6	-	-1.3	-2.25	-	-0.9	- T	17 10
(V <sub>OH</sub> = 13.5 V)				15	-4.2	257061	-3.4	8.8	_	-2.4	_	1000
$(V_{O1} = 0.4 V)$		Sink	IOL	5.0	0.64	_	0.51	0.88	_	0.36	_	1
(VOL = 0.5 V)		out	OL	10	1.6	1100/9-	1.3	2.25	-	0.9	child as	4 700
(VOL = 1.5 V)			The Hart	15	4.2	_	3.4	8.8	_	2.4	-	
Output Drive Current		Source	ТОН	64								m/
Other Outputs (CL/CP Device)			·Un		1 1 1	hard .				militaria		7 30
(VOH = 2.5 V)				5.0	-2.5	_	-2.1	-4.2	_	-1.7		
(VOH = 4.6 V)				5.0	-0.52		-0.44	-0.88	_	-0.36	_	1.0
(VOH = 9.5 V)				10	-1.3	hed.	-1.1	-2.25	_	-0.9		CINQ.
(VOH = 13.5 V)				15	-3.6	_	-3.0	-8.8	_	-2.4	_	
(VOI = 0.4 V)		Sink	lou	5.0	0.52		0.44	0.88	_	0.36	_	1
(V <sub>OL</sub> = 0.5 V)			IOL	10	1.3	Della .	1.1	2.25	-	0.36	1991 - an	- T Di
(V <sub>OL</sub> = 1.5 V)			11. 14	15	3.6		3.0	8.8		2.4	_	
		Andrew March	and the state of	10	3.0		3.0	0.0		2.4		

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance

the IC's potential performance.

\*T<sub>Iow</sub> = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = + 125°C for AL Device, +85°C for CL/CP Device.

# **ELECTRICAL CHARACTERISTICS (continued)**

to ancateologies brown of nester ad las	or emost	VDD	Tı	ow*		25°C		Th	igh*	
Characteristic	Symbol	V	Min	Max	Min	Typ #	Max	Min	Max	Unit
Input Current, RST (AL/CL/CP Device)	Iin	15	25	Pillippin Town		150	NEW DELL	io it <u>u</u> itad	250	μА
Input Current (AL Device)	lin	15	0821	± 0.1	-	± 0.00001	± 0.1	mularing.	±1.0	μА
Input Current (CL/CP Device)	lin	15	- 0	± 0.3	-	± 0.00001	±0.3	D negran	± 1.0	μА
Input Capacitance (Data)	Cin	-	lu luit yat	s assistante a	est on <del>a</del> gain	15	novets en	ties majort	eta Tonim	pF
Input Capacitance (All Other Inputs)	Cin	-	- 0	58 OF TA	8 marLD%	5.0	7.5	1000	god-ted e	pF
Quiescent Current (AL Device) (Per Package) I <sub>Out</sub> = 0 μA, V <sub>in</sub> =0 or V <sub>DD</sub>	IDD	5.0 10 15	-	5.0 10 20	sponsTeta	0.005 0.010 0.015	5.0 10 20	STDAR	150 300 600	µА ИДТО
Quiescent Current (CL/CP Device) (Per Package) I <sub>Out</sub> = 0 μA, V <sub>in</sub> =0 or V <sub>DD</sub>	IDD	5.0 10 15	ni <u>ld</u>	20 40 80	odaty8_ JspV = to	0.005 0.010 0.015	20 40 80	2010	150 300 600	μА
**Total Supply Current at an External Load Capacitance (C <sub>L</sub> ) on All Outputs	I <sub>T</sub>	80.0	4.95	ar oa	IT = (3	.5 μA/kHz) 3.0 μA/kHz) 4.5 μA/kHz)	f + IDD		0 10 Se	μА

<sup>Tlow = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.
The formulas given are for the typical characteristics only at 25°C.</sup> 

SWITCHING CHARACTERISTICS ( $T_A = 25^{\circ}C$ ;  $t_r = t_f = 20$  ns for X and I inputs;  $C_L = 50$  pF for JMP, X1, RR, Flag O, Flag F;  $C_L = 130$  pF + 1 TTL load for Data and Write.)

				0.5		10.6	VDD			All Types	(A 9's	3 - 0 TE
	Chara	cteristic		100	Symb	ol	Vdc	100	Min	Тур#	Max	Unit
Propagation Delay	Time	X1 to RR			tPLH	1.	5.0	116		250	500	ns
					tPHI		10	the.	layer. C	125	250	o boatio
					-00		15		-	100	200	12, 13
X1 to Flag F, I	lag O,	RTN, JMP	4.5	1			5.0		-	200	400	20-1
							10		-	100	200	0.8 - 0
				-			15	1		85	170	13.5
X1 to Write				1			5.0	HED	THE PARTY OF	225	450	1
				0.8		0.8	10		-	125	250	80 -
				0.83		0.8	15			100	200	0.1 0
X1 to Data				0.1		0.0	5.0		-	250	500	18100
				TEN			10	101	Squice	120	240	avisti :
				1 0			15	74	1 - 11	100	200	NE ALCOV
RST to RR				BEL		2.5-	5.0		-	250	500	To State
				6.64		200	10		-	125	250	P THO
				0.8		66-	15			100	200	FG . HC
RST to X1				-			5.0	-		450	Note 1	EL . HC
				0.1		G.7	10	100	THE IS	200	114	M.D. M.
				0.5		8.6.	15		-	150	(1/2	1.0 4 30
RST to Flag F	Flag (	D, RTN, JN	1P	0.8		2.2	5.0		- 10,-	400	800	A PRINC
				1 - ( )			10	s mi	Bourse	200	400	Secret 1
							15		-	150	300	Prestru O
RST to Write,	Data			15.		0.2.	5.0		-	450	900	
				18.0			10		-	225	450	E RO
	2000		80.0	50,00	10 10 11 11	49:0-	15			175	350	BP HE
Clock Pulse Width	, X1			1 7 7	tW(c	1)	5.0		400	200	- 100	ns
				LER		V 20-	10		200	100	_ (V) 3	St. HO
	98.0		88.6	18.0		48.0	15	101-	180	90	- 10	10.4 46
Reset Pulse Width	, RST			0.1	tW(R	1)	5.0		500	250	- 13 TV	ns
				0.5		9.4	10		250	125	- A	13 4 15
Am.							15		200	100	-	
Setup Time - Inst	ructio	n			t <sub>su(I)</sub>	)	5.0		400	200	Testvice Divisel	ns
				75-		810-	10		250	125	- 1	15 + m
				68.0		han.	15		180	90	-	D = 100
Data				1.1	t <sub>su(D</sub>	)	5.0		200	100	- 18	7 10 10 10
				O.E.		67	10		100	50	_	EL = HO
							15		80	40	- 384	HI = NO
Hold Time - Insti	uction			1000	th(1)	100	5.0	101	100	0	- 0	ns
				1319		01	10		50	0	- 19	10 - 10
				3,0		d.L.	15		50	0	- //(V	11-10
Data					th(D	)	5.0		200	100	-	
				10,1,00		1000	10	140 5	100	50	id of fon <u>al</u> "Gift"	Incelled
						0.006	15		100	50	echamiching lait	Autoo was

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

NOTE 1. Maximum Reset Delay may extend to one-half clock period.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 — TYPICAL CLOCK FREQUENCY versus RESISTOR (R<sub>C</sub>)

100 kg 100 kg 100 kg 1 Mgg

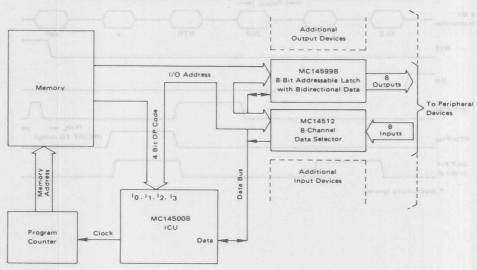
Pin No.	Function	Symbols
1	Chip Reset	RST
2	Write Pulse	Write
3	Data In/Out	Data
4	MSB Instruction Word	13
. 5	Bit 2 Instruction Word	12
6	Bit 1 Instruction Word	11
7	LSB Instruction Word	10
8	Negative Supply (Ground)	Vss
9	Flag on NOP F	Flag F
10	Flag on NOP O	Flag O
11	Subroutine Return Flag	RTN
12	Jump Instruction Flag	JMP
13	Oscillator Input	X2
14	Oscillator Output	X1
15	Result Register	RR
16	Positive Supply	VDD

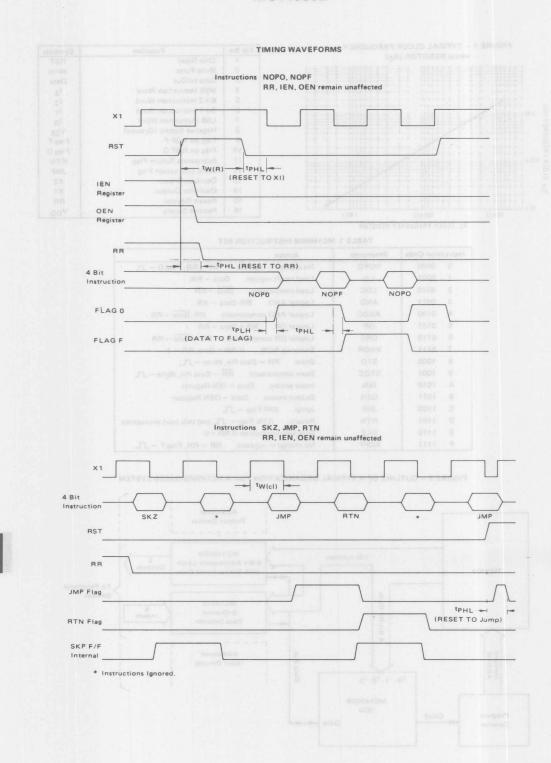
RC. CLOCK FREQUENCY RESISTOR

TARLE 1. MC14500R INSTRUCTION SET

Instruction Code	Mnemonic	Action
0 0000	NOPO	No change in registers. RR → RR, Flag O →
1 0001	LD	Load result register. Data → RR
2 0010	LDC	Load complement. Data → RR
3 0011	AND	Logical AND. RR · Data → RR
4 0100	ANDC	Logical AND complement. RR · Data → RR
5 0101	OR	Logical OR. RR + Data → RR
6 0110	ORC	Logical OR complement. RR + Data → RR
7 0111	XNOR	Exclusive NOR. If RR = Data, RR → 1
8 1000	STO	Store. RR → Data Pin, Write → JL
9 1001	STOC	Store complement. RR → Data Pin, Write →
A 1010	IEN	Input enable. Data → IEN Register
B 1011	OEN	Output enable. Data → OEN Register
C 1100	JMP	Jump. JMP Flag → Л
D 1101	RTN	Return. RTN Flag → _TL and skip next instruction
E 1110	SKZ	Skip next instruction if RR = 0
F 1111	NOPF	No change in registers. RR → RR, Flag F → JL

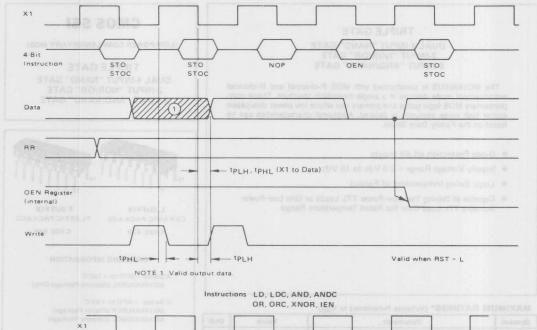
FIGURE 2 - OUTLINE OF A TYPICAL ORGANIZATION FOR A MC14500B-BASED SYSTEM

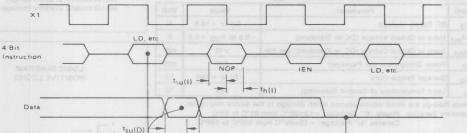




TIMING WAVEFORMS

Instructions STO, STOC, OEN





th(D)

tplH, tpHL (X1 to RR)

IEN Register (internal)

RR

Valid when RST = L

Valid when RST = L



# MC14501UB

# TRIPLE GATE

**DUAL 4-INPUT "NAND" GATE** 2-INPUT "NOR/OR" GATE 8-INPUT "AND/NAND" GATE

The MC14501UB is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

MAYIMUM DATINGS! O/strees Defense

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin, Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TI	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

# CIRCUIT SCHEMATIC VDD Q16 VDD 110-120-(6) 10 014 (7) 20-(9) 30-(5) 40 VSS 08 Numbers in parenthesis are for second 4 input gate.

# **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE GATE **DUAL 4-INPUT "NAND" GATE** 2-INPUT "NOR/OR" GATE 8-INPUT "AND/NAND" GATE



L SUFFIX CERAMIC PACKAGE **CASE 620** 

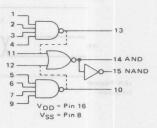
P SUFFIX PLASTIC PACKAGE **CASE 648** 

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXUBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXUBCP (Plastic Package) MC14XXXUBCL (Ceramic Package)

> LOGIC DIAGRAM (POSITIVE LOGIC)



Use Dotted Connection Externally to Obtain 8-Input AND/NAND

Note: Pin 14 must not be used as an input

# MC14501UB

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

			VDD	Tic	ow*		25°C		Thi	gh*	
Characteristic	1	Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "0"	Level	VOL	5.0		0.05		0	0.05		0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	Level	OL	10		0.05		0	0.05		0.05	
in DD or o		20.4	15		0.05		0	0.05	-	0.05	
	Level	V	5.0	4.95	-	4.95	5.0	75117	4.95	-	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	Level	VOH	10	9.95		9.95	10		9.95	-	
in So DD	1 3	00 1 3	15	14.95	dx.8	14.95	15	101	14.95	3 381 314	
1 0 81 1		20 1 3	200 h 1		28.8		Dil. 1		+ +	-	Vdc
	Level	VIL			16		2.25	1.5		1.4	vuc
(V <sub>O</sub> = 3.6 or 1.4 Vdc)	1 1	17 1 1	5.0		1.5	- 1	4.50	3.0	January G. H.	2.9	
(V <sub>O</sub> = 7.2 or 2.8 Vdc)		12 0	10	- 1	3.75	- 1	6.75	3.75		3.6	
$(V_0 = 11.5 \text{ or } 3.5 \text{ Vdc})$		1.P	15	-	11111				3.5	3.0	1/2.
	Level	VIH	5.0	3.6	- inspire	3.5	2.75	-		********	Vdc
$(V_0 = 2.8 \text{ or } 7.2 \text{ Vdc})$	- 3	ni + E (sb)	10	7.1	-	7.0	5.50	-	7.0	ention ed	
$(V_O = 3.5 \text{ or } 11.5 \text{ Vdc})$		at e trail	15	11.4	-	11.25	8.25	-	11.0		Day Pacing
Output Drive Current		ЮН	16						lie zmori	o lia no	mAdc
(AL Device)										Commission	
(VOH = 2.5 Vdc) Source			5.0	-1.2	-	-1.0	-1.7	-	-0.7	-	
(V <sub>OH</sub> = 4.6 Vdc)	io apa al	in Marqua	5.0	-0.25	PT	-0.2	-0.36	HQ1_20 10/	-0.14	0000 JA V	
(VOH = 9.5 Vdc) NAND	*	0.000	10	-0.62	-	0.5	-0.9	101 TO 101 C	-0.35	101 101	
(VOH = 13.5 Vdc)			15	-1.8	-	-1.5	-3.5	minution of a	-1.1	-	- Karlanda A
(VOH = 2.5 Vdc) NOR	Ru ni o	denienta, c	5.0	-2.1	- I	-1.75	-3.0	u lali <del>n</del> atori	-1.22	-	mAdc
(V <sub>OH</sub> = 4.6 Vdc)	400.0	e al brittage	5.0	-0.42	11 -	-0.35	-0.63	-	-0.24	-	
(VOH = 9.5 Vdc)			10	-1.06	-	-0.88	-1.58	emorgano è	-0.62	of Director	
(V <sub>OH</sub> = 13.5 Vdc)			15	-3.1		-2.63	-6.12	- 1	-1.84	-	
(VOH = 2.5 Vdc) NOR-			5.0	-3.6	-	-3.0	-5.1	-	-2.1	-	mAdc
(V <sub>OH</sub> = 4.6 Vdc)			5.0	-0.72	- (3)	-0.6	-1.08	or February	-0.42	AREK	
(VOH = 9.5 Vdc) Invert	er	-	10	-1.8	-	-1.5	-2.7		-1.05	-	
(VOH = 13.5 Vdc)	634	W foot	15	-5.4	-	-4.5	-10.5	all persons	-3.15	-	
			5.0	0.64		0.51	0.88		0.36		mAdc
	*	OL	10	1.6	HON	1.3	2.25		0.9		
	1 6	9	15	4.2		3.4	8.8		2.4	( double	
(V <sub>OL</sub> = 1.5 Vdc)	9					1723			DE SERVICE DE LA	CONTRACTOR.	A 4
(VOL = 0.4 Vdc) NOR	- 0		5.0	0.92		0.77 1.95	1.32	_	0.54	(Ruma	mAdc
(VOL = 0.5 Vdc)		.15	10	2.34	(70)		13.2		3.57	1985	
(V <sub>OL</sub> = 1.5 Vdc)	9.		15	6.12	_	5.1				Challen !	O'D Just
(VOL = 0.4 Vdc) NOR-	19		5.0	1.54	-	1.28	2.2	- 000	0.90	विकास व	mAdc
(VOL = 0.5 Vdc) Invert	er		10	3.90	-	3.25	5.63	- 49	2.27	Ada a	
(V <sub>OL</sub> = 1.5 Vdc)		18.3	15	10.2	(E) (E) (E)	8.5	22	-	5.95	-	T to 18 700
Output Drive Current	0.	ІОН							HIR + JO	Righan (E)	mAdc
(CL/CP Device)	- 0								10 - 20	Rights Of	
(VOH = 2.5 Vdc) Source			5.0	-1.0	-	-0.8	-1.7	- 31	-0.6	Piglie B	
(VOH = 4.6 Vdc)		300	5.0	-0.2	195100	-0.16	-0.36	-	-0.12	911	
(VOH = 9.5 Vdc) NAND	* 0.	8	10	-0.5	-	-0.4	-0.9	- 011	-0.3	Rolan U	
(V <sub>OH</sub> = 13.5 Vdc)	- 0		15	-1.4	-	-1.2	-3.5	- 40 7	-1.0	Holim (II)	.01 = 10em
(VOH = 2.5 Vdc) NOR	8		5.0	-1.68	-	-1.4	-3.0	- 101	-1.05	Phylics 11	mAdc
(VOH = 4.6 Vdc)		1	5.0	-0.34	-	-0.28	-0.63	_	-0.21	Section 1	
(V <sub>OH</sub> = 9.5 Vdc)	0	100	10	-0.84	- 1	-0.7	-1.58	10+00×	-0.52	1 T.17 -	
(V <sub>OH</sub> = 13.5 Vdc)	10		15	-2.52	-	-2.1	-6.12	mit c	-1.57	88.54-	
(VOH = 2.5 Vdc) NOR-	8		5.0	-2.88	-	-2.4	-5.1	NE-35 N	-1.8	# 8.25E =	mAdc
(VOH = 4.6 Vdc)	1 0	1 10	5.0	-0.58	- 1	-0.48	-1.08	\$8-0E s	-0.36	C 24-	
(VOH = 9.5 Vdc) Invert	er	210	10	-1.44	-	-1.2	-2.7	m=0+	-0.9	80.04-	
(V <sub>OH</sub> = 13.5 Vdc)	1 0		15	-4.32	-	-3.6	-10.5	8-05	-2.7	0.00-	
(VOL = 0.4 Vdc) Sink	0	loL	5.0	0.52	1967101	0.44	0.88	p_3b_s	0.36	1 K 34-11	mAdc
(V <sub>OL</sub> = 0.5 Vdc) NAND	*	.OL	10	1.3	-	1.1	2.25	2027	0.9	SERVICE .	THE STATE OF
(V <sub>OL</sub> = 1.5 Vdc)	1 1	-	15	3.6		3.0	8.8	64-00	2.4	0.0.04	
	-		5.0	0.79		0.66	1.32		0.54		mAdc
(V <sub>OL</sub> = 0.4 Vdc) NOR	160 161 3	sen ad at a	10	1.98	400 T	1.65	3.37	monarco	1.36	sot ma ne	MAGC
(Vol = 0.5 Vdc)	BILLINGOOD	0 01 966 13		ALCOHOLOGY OF THE PARTY OF	-		10455				
(V <sub>OL</sub> = 1.5 Vdc)			15	5.4	-	4.5	13.2	_	3.57		
(VOL = 0.4 Vdc) NOR-			5.0	1.32	-	1.1	2.2		0.90	-	mAdc
(VOL = 0.5 Vdc) Invert	er		10	3.3	-	2.75	5.63	-	2.27	-	
(V <sub>OL</sub> = 1.5 Vdc)	- 1		15	9.0	-	7.5	22.0	-	5.95	-	

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

<sup>\*</sup>The output drive current of Pin 15 is tested with Pin 14 open-circuited.

# ELECTRICAL CHARACTERISTICS (Continued)

	Vnn	D Tlow*		25°C			Thigh*		
Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
lin	15	-	±0.1	-	±0,00001	±0.1	Tieber	±1.0	μAdc
lin	15	-	±0.3	-	±0,00001	± 0.3	-	±1.0	μAdo
Cin	0 -		(O.OL	-	5.0	7.5	3.7	-	pF
IDD	5.0 10 15	Ē	0.25 0.50 1.00	-	0.0005 0.0010 0.0015	0.25 0.50 1.00	-	7.5 15.0 30.0	μAdo
IDD	5.0 10 15	=	1.0 2.0 4.0		0.0005 0.0010 0.0015	1.0 2.0 4.0	-	7.5 15.0 30.0	μAdo
lτ	5.0 10 15	0.1		IT =	2.4 µA/kHz	f+IDD		V 2 V 3c) V 2 V 3c) V 5 V det	μAdd
	I <sub>in</sub> I <sub>in</sub> C <sub>in</sub> I <sub>DD</sub>	I <sub>in</sub>   15   I <sub>in</sub>   15   C <sub>in</sub>   -     I <sub>DD</sub>   5.0   10   15   10   15   15   15   17   10   10   10   10   10   10   10	Symbol   Vdc   Min	Symbol   Vdc   Min   Max	Symbol   Vdc   Min   Max   Min   Iin   15   -   ±0.1   -     Iin   15   -   ±0.3   -     Cin   -   -   -   -     IDD   5.0   -   0.50   -     15   -   1.00   -     IDD   5.0   -   1.0   -     IDD   5.0   -   1.0   -     IDD   5.0   -   1.0   -     IT   5.0   IT = (	Symbol   Vdc   Min   Max   Min   Typ #	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Symbol   Vdc   Min   Max   Min   Typ # Max   Min     Iin   15   - ±0.1   - ±0.00001 ±0.1   -     Iin   15   - ±0.3   - ±0.00001 ±0.3   -     Cin   -   -   -   5.0   7.5   -     IDD   5.0   -   0.25   -   0.0005   0.25   -     10   -   0.50   -   0.0010   0.50   -     15   -   1.00   -   0.0015   1.00   -     IDD   5.0   -   1.0   -   0.0005   1.0   -     10   -   2.0   -   0.0015   4.0   -     IT   5.0   IT = (1.2 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (2.4 μA/kHz) f + IDD     IT = (1.2 μA/kH	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

 $<sup>^*</sup>T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance. †To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_{\overline{I}}$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD - V\_SS) in volts, f in kHz is input frequency, and k = 0.004.

# SWITCHING CHARACTERISTICS\*\* (CL = 50 pF, TA = 25°C)

Characteristic		. 2.4-	Figure	Symbol	VDD	Тур#	Max	Unit
Output Rise Time tTLH = (3.0 ns/pF) C <sub>L</sub> + 30 ns tTLH = (1.5 ns/pF) C <sub>L</sub> + 15 ns	0.88 2.24 8.8	NAND, NOR	2,3	tTLH C	5.0	180	360 180	ns
tTLH = (1.1 ns/pF) CL + 10 ns		110		01	15	65	130	- Imv
Output Fall Time t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	2.61	NAND, NOR	2,3	tTHL	5.0	100	200	ns
t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	2.2	83.5		0.0	10 15	50 40	100	You?
Output Rise Time  t <sub>TLH</sub> = (1.35 ns/pF) C <sub>L</sub> + 32.5 ns  t <sub>TLH</sub> = (0.60 ns/pF) C <sub>L</sub> + 20 ns  t <sub>TLH</sub> = (0.40 ns/pF) C <sub>L</sub> + 17 ns	1.1-	NOR-Inverter	3	TLH	5.0 10 15	100 50 40	200 100 80	ns nd ma
Output Fall Time t <sub>THL</sub> = (0.67 ns/pF) C <sub>L</sub> + 26.5 ns t <sub>THL</sub> = (0.45 ns/pF) C <sub>L</sub> + 17.5 ns t <sub>THL</sub> = (0.37 ns/pF) C <sub>L</sub> + 11.5 ns	2E 0- 0.0- 0.0-	NOR-Inverter	3	THL	5.0 10 15	60 40 30	120 80 60	HOV HOV
Propagation Delay Time tp_H, tpHL = (1.7 ns/pF) CL + 45 ns tp_H, tpHL = (0.66 ns/pF) CL + 37 ns tp_H, tpHL = (0.5 ns/pF) CL + 25 ns	1.58 -1.58 -5.12	NAND	2	tPLH, tPHL	50 10 15	130 70 50	260 140 100	ns
tpLH, tpHL = (1.7 ns/pF) CL + 30 ns tpLH, tpHL = (0.66 ns/pF) CL + 32 ns tpLH, tpHL = (0.5 ns/pF) CL + 20 ns		NOR	## 03   PA	tPLH, tPHL	5.0 10 15	115 65 45	230 130 90	ns
tpLH, tpHL = (1.7 ns/pF) CL + 45 ns tpLH, tpHL = (0.66 ns/pF) CL + 37 ns tpLH, tpHL = (0.5 ns/pF) CL + 25 ns		NOR-Inverter	3	tPLH, tPHL	5.0 10 15	130 70 50	260 140 100	ns 10 V

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

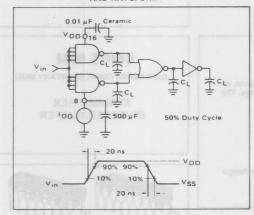
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14501UB

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT
AND WAVEFORM



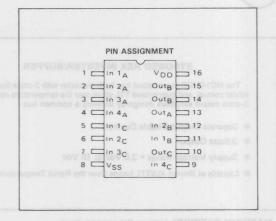


FIGURE 2 – 4-INPUT "NAND" GATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

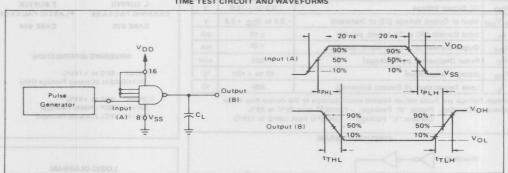
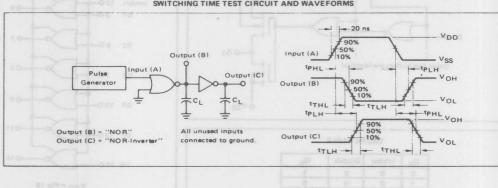


FIGURE 3 - "NOR" GATE and "NOR-INVERTER" SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



# MC14502B

### STROBED HEX INVERTER/BUFFER

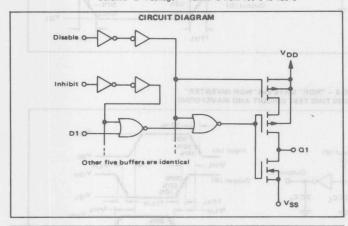
The MC14502B is a strobed hex buffer/inverter with 3-state outputs, an inhibit control, and guaranteed TTL drive over the temperature range. The 3-state output simplifies design by allowing a common bus.

- Separate Output Disable Control
- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving 4LSTTL Loads Over the Rated Temperature Range

# MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin	Input Current (DC or Transient), per Pin	± 10	mA
lout	Output Current (DC or Transient), per Pin	+30	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C



### TRUTH TABLE Dn Inhihit Disable an 0 0 0 0 0 0 0 X 0 × High ×

# **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

STROBED HEX INVERTER/BUFFER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

LOGIC DIAGRAM

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

# 3-State Output Disable Inhibit 120 D1 30 D2 60 D7 02 D3 10 D4 100 D9 04 D6 150 D6 150 D14 06

V<sub>DD</sub> = Pin 16 V<sub>SS</sub> = Pin 8

6

X = Don't Care

# ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

All Fagues		VDD	Tio	w*		25°C	Land St.	Thi	gh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
	21.8	10	- 1	0.05	_	0	0.05	_	0.05	
V <sub>in</sub> = V <sub>DD</sub> or 0	08	15	_	0.05	_	0	0.05	- 1	0.05	
GB "1" Level	VOH	5.0	4.95	_	4.95	5.0	-	4.95	_	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	V OH	10	9.95	and the second	9.95	10		9.95	and the	1 Vac
TIN O ST TOO	0.8	15	14.95		14.95	15		14.95	-	1
Input Voltage "0" Level	VIL									Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	88	5.0		1.5	-	2.25	1.5	- 1	1.5	1
(VO = 9.0 or 1.0 Vdc)	0.8	10	-	3.0	-	4.50	3.0	100-01	3.0	111001
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	200	15		4.0	_	6.75	4.0		4.0	
"1" Level	VIH									
(VO = 0.5 or 4.5 Vdc)	6.8	5.0	3.5	***	3.5	2.75	O to sid	3.5	and the same	Vdc
(VO = 1.0 or 9.0 Vdc)	61	10	7.0		7.0	5.50	-	7.0	- Indiana	-
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	87	15	11.0	_	11.0	8.25	-	11.0	-	
Output Drive Current (AL Device)	ГОН	Co veri		-		C) or sint	GI Bar	radi uniti	ner Ebelay	mAde
(VOH = 2.5 Vdc) Source	102	5.0	-3.0	_	-2.4	-4.2	-	-1.7		
(V <sub>OH</sub> = 4.6 Vdc)	n 1	5.0	-0.64	_	-0.51	-0.88	_	-0.36	_	
/V 0 E V/d-1		10	-1.6	ingle and the	-1.3	-2.25	THE RESIDENCE	-0.9	-	ares &
(VOH = 13.5 Vdc)	0.3	15	-4.2	-	-3.4	-8.8	- 700000	-2.4	a custoscilos	- SELECTION
(VOI = 0.4 Vdc) Sink	IOL	5.0	3.5		2.8	6.6	_	2.0	_	mAd
04 05 144	the state of the same	10	7.8		6.3	17		4.4		111110
(V <sub>OL</sub> = 0.5 Vdc)	8.8	15	29	_	24	66	encita rigi	16	oingago:	2000
Output Drive Current (CL/CP Device)	ГОН	-	-		-			-		mAd
(V <sub>OH</sub> = 2.5 Vdc) Source	The state of the s	5.0	-2.5		-2.1	-4.2		-1.7		I
	0.0	5.0	-0.52		-0.44	-0.88	D. Marie	-0.36	Control of the contro	District -
	BY	10	-1.3		-1.1	-2.25	_	-0.9	_	
(Va 13 5 Vda)	87	15	-3.6		-3.0	-8.8	-	-2.4		-
(V <sub>OL</sub> = 0.4 Vdc) Sink	1-	5.0	2.3	_	-	6.6	-	1.6	-	mAd
(V <sub>OL</sub> = 0.5 Vdc)	IOL	10	5.0		1.9	17		3.4	- 47	MAG
(VOL = 1.5 Vdc)	- 87	15	19		4.2	66		13		
	-	and board and	The second		16			-		-
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	± 0.1		± 1.0	μAdd
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	- 1	± 1.0	μAdo
nput Capacitance	Cin	-		-	-	5.0	7.5	-	-	pF
(V <sub>in</sub> = 0)										
Quiescent Current (AL Device)	IDD	5.0	-	1.0	-	0.002	1.0	-	30	μAde
(Per Package)		10	-	2.0	-	0.004	2.0	- 1	60	
WANTED TRANSPORT	- KUNDE	15	-	4.0	- 39	0.006	4.0	TYP w 1	120	
Quiescent Current (CL/CP Device)	IDD	5.0	-	4.0	-	0.002	4.0	Tunis.	30	μAd
(Per Package)		10	-	8.0	-	0.004	8.0	-	60	1
		15	-	16	-	0.006	16	-	120	
Total Supply Current**†	IT	5.0			IT = (2	2.7 μA/kHz	) f + IDD	- 81		μAde
(Dynamic plus Quiescent,		10			IT = (5	5.3 μA/kHz	) f + IDD			11-
Per Package)	-	15				B.O HA/KHZ				
(CL = 50 pF on all outputs, all	S Security		W 5				la V			
buffers switching)					No. of the					
Three-State Leakage Current	ITL	15	-	± 0.1	-	+0.00001	± 0.1	102	±3.0	μAdo
inree-State Leakage Current										1
(AL Device)	I providence					Life will		00 1		
	ITL	15	-	±1.0	-	+0.00001	±1.0	-001	± 7.5	μAd

 $^*T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device. Thigh = + 125°C for AL Device, +85°C for CL/CP Device.

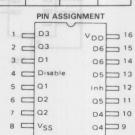
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: IT is in  $\mu$ A (per package), CL in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.006.



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

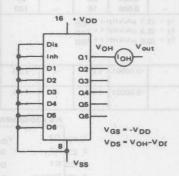
SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

			Chause	teristic				Symbol	W		All Types		Unit
			Charac	TOVISTIC				aymooi	VDD	Min	Тур#	Max	Un
Output Ris	se Time		80.0	9	1 4	80.0	100	tTLH .	105/	- Biced	10.7	901/10	n
								01	5.0	-	100	200	120
								- at 1	10	-	50	100	1
								0.2	15	imal-	40	80	
Output Fa	II Time	98.6	1 - 1	- 01	1,56.6		88.0	†THL				GUV ID U	n
								ar si	5.0	-	40	80	
									10	M- 10	20	40	V ID
								0.3	15	-	15	30	lev.
Propagatio	on Delay	Time Dat	ta to Q	02.8	1 1	0.4		tPHL	5.0	-	135	270	n
								- EI	10	-	55	110	OVI
									15	avel 11	40	80	
Propagatio	on Delay	Time, Int	nibit to Q	ACS.	1 10		E.C.	tPHL	5.0	-	335	670	O n
								01	10.	-	145	290	OV
								. 31	15	-	95	190	OVI
Propagatio	on Delay	Time Dat	ta to Q, Inh	ibit to Q			1 1 1 1 1	tPLH	5.0	- 100	295	590	n
								i ble	10	- 55	130	260	1010
								9.8	15	-	95	190	HBY)
3-State Pr	opagatio	Delay, C	Output "1"	to High I	mpedance			tPHZ	5.0	-	65	130	n
									10	-	30	60	HOA
		0.5						0.8	15	-	25	50	JOV3
3-State Pr	opagatio	n Delay, h	High Imped	lance to "1	I" Level		100	tPZH	5.0	-	260	520	n
								1815	10	-	106	210	DA.
Sham					1				15	-	80	180	hullp
3-State P	ropagatio	on Delay,	Output "0	" to High	Impedance			tPLZ	5.0	- 99	150	300	n
								0.8	10	-	70	140	1010
		80-		-2.35			1.0		15	-	55	110	OA
3-State Pr	opagation	Delay, H	High Imped	lance to "(	O" Level		11.5	tPZL	5.0	-	160	320	n
								0.0	10	-	66	130	OVI
								61	15	-	50	100	103/1

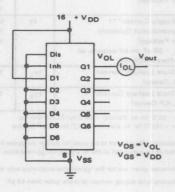
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# FIGURE 1 - TYPICAL OUTPUT SOURCE CURRENT TEST CIRCUIT (IOH)



### FIGURE 2 - TYPICAL OUTPUT SINK CURRENT TEST CIRCUIT (IOL)



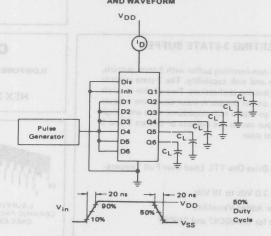
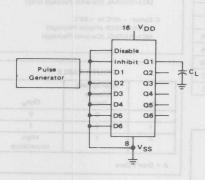
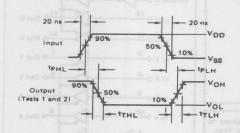


FIGURE 4 — AC TEST CIRCUIT AND WAVEFORMS (tTLH, tTHL, tPLH, and tPHL)

FIGURE 5 — 3-STATE AC TEST CIRCUIT AND WAVEFORMS (tpHZ, tpLZ, tpZH, tpZL)



For all tTLH, tTHL, tpHL, and tpLH measurements  $V_{in}$  may be applied to any other  $D_n$  input or to Inhibit.





Disable

D1

Inhibit Q1

02

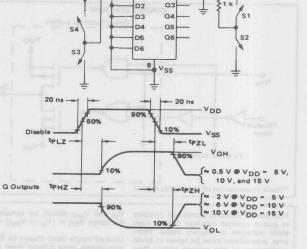
03

VDD

Pulse

Generator

VDD



# MC14503B

# **HEX NON-INVERTING 3-STATE BUFFER**

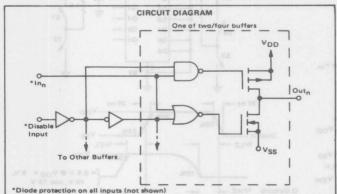
The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin	Input Current (DC or Transient), per Pin	±10	mA
lout	Output Current (DC or Transient), per Pin	± 25	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,

 $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

# **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

**HEX 3-STATE BUFFER** 





L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

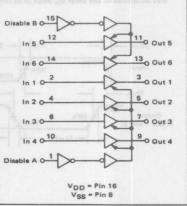
C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### TRUTH TABLE

ln <sub>n</sub>	Appropriate Disable Input	Outn
0	0	0
1	80 0	1
×	1	High Impedance

X = Don't Care

# LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

95092 Ris		VDD	Tic	ow *		25°C		Thi	gh	
Characteristic	Symbol		Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	1-1	0.05	- 1	0	0.05	-	0.05	Vdc
V <sub>in</sub> = 0	0.	10	_	0.05	_	0	0.05	2 12 (9)	0.05	
30.	120	15		0.05	_	0	0.05	3 + 10 1 m	0.05	
"1" Level	Van	5.0	4.95	-	4.95	5.0	4n 0:	4.95	ben 2.05,	Vdc
V <sub>in</sub> = V <sub>DD</sub>	VOH		9.95	-100	9.95	10		9.95	server to	7 record
111 00		10	14.95	200	14.95	15	260 00	14.95	Carrie Zigiti e	
01 1		15	14.95	-	14.95	15		14.95	200 (200)	Vdc
Input Voltage "0" Level	VIL						400	35,440	100 Page 100	
(V <sub>O</sub> = 3.6 or 1.4 Vdc)	35	5.0	-	1.5	-	2.25	1.5	F 12 (36	1.5	
(V <sub>O</sub> = 7.2 or 2.8 Vdc)		10	-	3.0	7 - 1	4.50	3.0	SVOTE S	3.0	
(V <sub>O</sub> = 11.5 or 3.5 Vdc) "1" Level		15	- 1	4.0	-	6.75	4.0	04 51 (3)	4.0	14,343
(Vo = 1.4 or 3.6 Vdc)	VIH	5.0	3.5	-	3.5	2.75	÷11.13	3.5	on ((4.0)	Vdc
(VO = 2.8 or 7.2 Vdc)	22	10	7.0	-	7.0	5.5	-1014	7.0	Am 4.01	
(V <sub>O</sub> = 3.5 or 11.5 Vdc)	-	15	11	110	11	8.25	- 019	110	entT water	inD-mu
Output Drive Current (AL Device)***	ОН	n.					20-1	34 D R	Sent C.dl	mAde
(VOH = 2.5 Vdc) Source	-OH	4.5	-4.3		-3.6	-5.0	-/4 5/5	-2.5	W 22 0)	12457
	200	5.0	-5.8		-4.80	-6.1		-3.0	100 E 100	1000
(V <sub>OH</sub> = 2.5 Vdc)	NO.			-		Marine Control of the			-	
(V <sub>OH</sub> = 4.6 Vdc)	19	5.0	-1.2	"Ste	-1.02	-1.4	- 57	-0.7	10,012100	
(V <sub>OH</sub> = 9.5 Vdc)		10	-3.1	-	-2.60	-3.7	498100	-1.8	D1 - 1	ochran-
(V <sub>OH</sub> = 13.5 Vdc)	8	15	-8.2	-	-6.80	-14.1	-	-4.8	-	
Sink	IOL			3.0	el .		manyari	radius, spins	03 101 3	mAd
(V <sub>OL</sub> = 0.4 Vdc)		4.5	2.2	-	1.8	2.1	-	1.2	-	
(VOL = 0.4 Vdc)	5	5.0	2.6		2.1	2.3	-	1.3	-	war
(Vol = 0.5 Vdc)	19	10	6.5	_HS	5.5	6.2	194	3.8	CONTRACTOR OF THE	rigits
(V <sub>OL</sub> = 1.5 Vdc)	1	15	19.2	_	16.10	25.00	-	11.2	_	
Output Drive Current (CL/CP Device)***	Іон						-	c 100900		mAd
(VOH = 2.5 Vdc) Source	-OH	4.75	-4.0	45	-3.60	-5.5	1440	-2.4	COMMUNICATION OF THE	1 september 1
		5.0	-4.6		-4.20	-6.1		-3.0		
(V <sub>OH</sub> = 2.5 Vdc)			183	1.7		1	and ellarest	-0.7		
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-1.0	_	-0.88	-1.4	gris Isola	打海湖 测路 原	e navig us	INTERES OF
(V <sub>OH</sub> = 9.5 Vdc)		10	-2.4	-	-2.20	-3.7	tortass	-1.8	Tod Type	odni Misi
(V <sub>OH</sub> = 13.5 Vdc)		15	-6.6		-6.00	-14.1	month of the	-4.8	DIGUETAN IN	000000
Sink	IOL									mAde
(VOL = 0.4 Vdc)		4.75	2.1	-	1.95	2.2	-	1.25	-	
(VOL = 0.4 Vdc)		5.0	2.3		2.10	2.3	-	1.3	-	
(VOL = 0.5 Vdc)		10	6.0	_	5.45	6.2	-	3.8	_	
(V <sub>OL</sub> = 1.5 Vdc)		15	15.2	20228	13.80	25.00	_	11.2	_	
Input Current (AL Device)	lin	15		± 0.1	-	±0.00001	±0.1	-	±1.0	μAdd
Input Current (CL/CP Device)	-	15	and V	± 0.3	To least	±0.00001	±0.3		±1.0	μAdo
	lin	3-		±0.3	-1 -D 5	5.0	7.5	-		
Input Capacitance (V <sub>in</sub> = 0)	Cin		0.00	-		-	-	-	-	pF
Quiescent Current (AL Device)	IQ	5.0	a n:	1.0	10 122 5	0.002	1.0	-	30	μAdd
(Per Package)		10	a Teo	2.0	01/23/	0.004	2.0	-	60	
		15		4.0		0.006	4.0	-	120	
Quiescent Current (CL/CP Device)	IDD	5.0	-	4.0	-	0.002	4.0	-	30	μAdd
(Per Package)		10	2 100	8.0	-	0.004	8.0	-	60	
		15	Dog.	16	0 50	0.006	16	-	120	
Total Supply Current **†	I <sub>T</sub>	5.0	BILLO	8	av Hart			-	-	μAdo
(Dynamic plus Quiescent, Per Package)	1	10				$= (2.5 \mu A/k$				
(C <sub>L</sub> = 50 pF on all outputs)		15				$= (6.0 \mu A/k$				
All outputs switching, 50% Duty Cycle)		15			1 <sub>T</sub>	$= (10 \mu A/k)$	Hz) f + 1	DD		1
	-		-			T				-
3-State Output Leakage Current	ITL	15	-	±0.1	-	±0.0001	±0.1	-	±3.0	μAdd
(AL Device)			-		-			-		
3-State Output Leakage Current	ITL	15	-	±1.0	-	±0.0001	±1.0	-	± 7.5	μAdo
(CL/CP Device)										

<sup>\*</sup>Tlow = -55°C for AL Device, -40°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (VDD – VSS) in volts, f in kHz is input frequency, and k = 0.006.

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

Thigh = + 125°C for AL Device, +85°C for CL/CP Device.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>\*\*\*</sup>Care must be taken not to exceed maximum current ratings (see maximum ratings table)

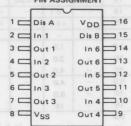
SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

	40.001284		VDD	All T	ypes	
Characteristic		Symbol	Vcc	Typ #	Max	Unit
Output Rise Time	0	tTLH	1 62	1019 F	-13 To	ns ns
TLH = (0.5 ns/pF) CL + 20 ns		80.0	5.0	45	90	C-mY
TLH = (0.3 ns/pF) CL + 8.0 ns		- 20.0	10	23	45	
TLH = (0.2 ns/pF) CL + 8.0 ns		1 202	15	18	35	
Output Fall Time	- 01	tTHL	9.8			ns
THL = (0.5 ns/pF) CL + 20 ns		39.87.	5.0	45	90	
THL = (0.3 ns/pF) CL + 8.0 ns			10	23	45	- Apark N Jugmes
THL = (0.2 ns/pF) CL + 8.0 ns		1	15	18	35	17 to 8.0 = 0.00
Turn-Off Delay Time, all Outputs	05.0	tPLH	1 01		1997	ns
tpLH = (0.3 ns/pF) CL + 60 ns		0.0	5.0	75	150	1 - 911 - 040
tpLH = (0.15 ns/pF) CL + 27 ns		1 26 1 - 1	10	35	70	ACTOR DE MANO
tpLH = (0.1 ns/pF) CL + 20 ns		Has I	15	25	50	140 = 2.8 er 18
Furn-On Delay Time, all Outputs	8,36	tPHL	37 61		CHEA S	ns ov
tpHL = (0.3 ns/pF) CL + 60 ns			5.0	75	150	lutput Crise Corps
tpHL = (0.15 ns/pF) CL + 27 ns		1-22-1 - 1	10	35	70	WOH # \$5 VO
tpHL = (0.1 ns/pF) CL + 20 ns	1,0-	08,5-	15	25	50	(PRA STEN HOA)
3-State Propagation Delay Time	RGE C	tPHZ	5.0	75	150	ns
Output "1" to High Impedance		00.5-	10	40	80	Dev ER - HOVE
		CR S-	15	35	70	AND THOM
Output "0" to High Impedance		tPLZ	5.0	80	160	ns
		1 41 1 - 1	10	40 35	80 70	\$5V 8.0 + 15VI
W		11	5.0	65		Diggs D. & Ved
High Impedance to "1" Level		tPZH	10	25.	130	INVENTS JOY
		01.87	15	20	40	-07 g 3 = 30A)
High Impedance to "0" Level		tpZL	5.0	100	200	ns
-2.4		02.0-	10	35	70	COVER NOV
		05.6-	15	25	50	IVON - 2.5 Yes

"The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

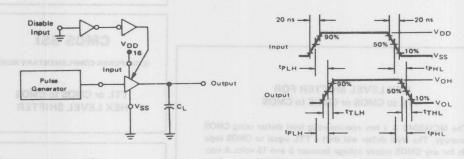




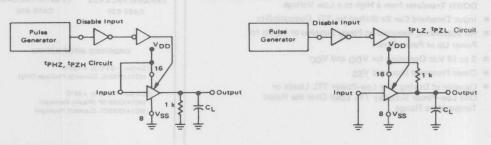
# MC14503B

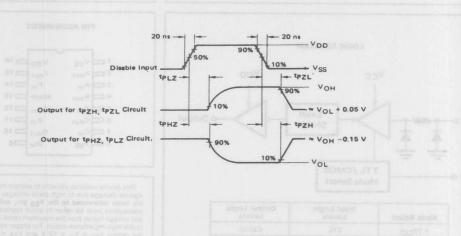






# FIGURE 2 - 3 STATE AC TEST CIRCUITS AND WAVEFORMS (tplz, tphz, tpzh, tpzl)





# MC14504B

# CMOS SSI

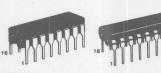
(LOW-POWER COMPLEMENTARY MOS)

TTL or CMOS to CMOS HEX LEVEL SHIFTER

# HEX LEVEL SHIFTER FOR TTL to CMOS or CMOS to CMOS

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level. Either up or down level translating is accomplished by selection of power supply levels VDD and VCC. The VCC level sets the input signal levels while VDD selects the output voltage levels.

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for VDD and VCC
- Diode Protected Inputs to VSS
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

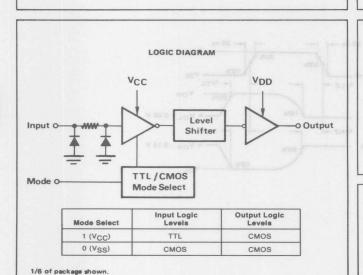


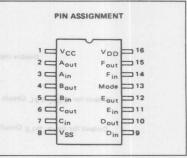
L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

### ORDERING INFORMATION

A Series: -55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields **referenced to the Vsg pin, only.** Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges Vsg. s Vin  $\leq$  18 V and Vsg.  $\leq$  Vout  $\leq$  VpD are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

# MC14504B

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage	-0.5 to +18.0	V
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin	Input Voltage (DC or Transient)	- 0.5 to + 18.0	V
Vout	Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin, lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package**	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

# ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

	(4)	Vcc	VDD	Tic	w*		25°C		Thi	gh*	
Characteristic	Symbol	Vdc	Vdc	Min	Max	Min	Тур #	Max	Min	Max	Uni
Output Voltage "0" Level	VOL	-	5.0	-	0.05	-	0	0.05	-	0.05	Vdd
Vin = 0 V	86	-	10	-	0.05	-	0	0.05	-	0.05	
		-	15	-	0.05	s new Table	0	0.05	Sun T 's	0.05	ni anati
V <sub>in</sub> = V <sub>CC</sub> "1" Level	Vон	_	5.0	4.95	_	4.95	5.0	s Quest	4.95	I delicate b	Vdd
	011	_	10	9.95	_	9.95	10	-	9.95	_	
	TURWS	3900	15	14.95	19400	14.95	15	distrant	14.95	W 7 3	RUBSE
Input Voltage "0" Level	VII										Vdd
(VOL = 1.0 Vdc) TTL-CMOS	11	5	10	_ 1	0.8	_	1.3	0.8	_	0.8	N. F
(VOL = 1.5 Vdc) TTL-CMOS		5	15	_	0.8	1	1.3	0.8	_	0.8	- 5
(VOL = 1.0 Vdc) CMOS-CMOS	8 2 7 18	5	10	_	1.5	1	2.25	1.5		1.4	F . W
(VOL = 1.5 Vdc) CMOS-CMOS		5	15	- 1	1.5		2.25	1.5	-	1.5	3
(VOL = 1.5 Vdc) CMOS-CMOS		10	15	_	3.0	200	4.5	3.0	-	2.9	0 5
Input Voltage "1" Level	VIH		1								Vdd
(VOH = 9.0 Vdc) TTL-CMOS	* IH	5	10	2.0		2.0	1.5	1.0	2.0		
(VOH = 13.5 Vdc) TTL-CMOS		5	15	2.0		2.0	1.5		2.0	_	7
(VOH = 9.0 Vdc) CMOS-CMOS		5	10	3.6		3.5	2.75	N	3.5	_ 1	1
(V <sub>OH</sub> = 13.5 Vdc) CMOS-CMOS		5	15	3.6	_	3.5	2.75		3.5		6 3
(VOH = 13.5 Vdc) CMOS-CMOS	J 1	10	15	7.1		7.0	5.5		7.0	_	- 5
Output Drive Current (AL Device)	lou	-	100		+						mAd
(V <sub>OH</sub> = 2.5 Vdc) Source	ІОН	100	5.0	-3.0	-	-2.4	-4.2		-1.7	_	mac
(V <sub>OH</sub> = 4.6 Vdc)		L	5.0	-0.64		-0.51	-0.88		-0.36		. 3
(V <sub>OH</sub> = 9.5 Vdc)	Part of	I	10	-1.6		-1.3	-2.25		-0.9		-
(V <sub>OH</sub> = 13.5 Vdc)		L	15	-4.2		-3.4	-8.8		-2.4		- 79
	1.	-	-	-			+	_	-		A d
	IOL	Ū	5.0	0.64	08 -	0.51	0.88	_	0.36	- 6	mAd
$(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	paV i	-	15	1.6		1.3	2.25 8.8	ARAMI	0.9		
	-		15	4.2		3.4	0.0		2.4		
Output Drive Current (CL/CP Device) (VOH = 2.5 Vdc) Source	ЮН		5.0	-2.5		-2.1	-4.2		-1.7		mAd
(V <sub>OH</sub> = 2.5 Vdc) Source (V <sub>OH</sub> = 4.6 Vdc)		_	5.0	-0.52	- E	-0.44	-4.2	_	-0.36	-	
(V <sub>OH</sub> = 9.5 Vdc)	-	Tou	10	-1.3		-0.44	-2.25		-0.36		500
(V <sub>OH</sub> = 13.5 Vdc)	Lane.	I	15	-3.6	-10	-3.0	-8.8		-2.4		11 - 11
			-	-	-	-	+		-		-
(V <sub>OL</sub> = 0.4 Vdc) Sink	IQL	T	5.0	0.52	-38	0.44	0.88		0.36	-	mAd
(V <sub>OL</sub> = 0.5 Vdc)		-1-8	10	1.3	1 18	1.1	2.25	12.20	0.9		18 B
(V <sub>OL</sub> = 1.5 Vdc)	(C)	T		3.6	L. Chi		8.8	7.7	2.4		
Input Current (AL)	lin		15	-	± 0.1	11-11	± 0.00001	±0.1	( ) = ·	± 1.0	μAd
Input Current (CL/CP)	lin	-	15	-	± 0.3	-	± 0.00001	±0.3	77-	± 1.0	μAd
Input Capacitance (Vin = 0)	Cin	-	-	-	-18	10-77	5.0	7.5	NE.	- 1	pF
Quiescent Current (AL Device)	IDD or	1	5.0	-	0.05	2270	0.0005	0.05	137	1.5	μAd
(Per Package)	Icc	+	10	-	0.10	13.73	0.0010	0.10	250	3.0	1
CMOS-CMOS Mode		-	15	-	0.20	-	0.0015	0.20	27.73	6.0	. 3
Quiescent Current (CL/CP Device)	IDD or	-	5.0	-	0.5	17.77	0.0005	0.5	1121	3,8	μAd
(Per Package)	Icc		10	_	1.0	81773	0.0010	1.0	2000	7.5	0
CMOS-CMOS Mode	00	-	15	-	2.0	217	0.0015	2.0	223	15.0	. 0
Quiescent Current (AL/CL/CP Device)	IDD	5.0	5.0	_	0.5	-	0.0005	0.5	2000	3.8	μAd
(Per Package)	.00	5.0	10		1.0		0.0003	1.0		7.5	μΑ
TTL -CMOS Mode		5.0	15	_	2.0		0.0015	2.0		15.0	
Quiescent Current (AL/CL/CP Device)	Lan	5.0	-				-		-		
(Per Package)	Icc	5.0	5.0	-	5.0	89	2.5	5.0	8	6.0	mAd
TTL -CMOS Mode	100		1	-	5.0	bolovini	A COLUMN TO THE PARTY OF	5.0	2007	6.0	
I I L - CMIOS MIODE	199	5.0	15	_	5.0		2.5	5.0	-	6.0	

<sup>\*</sup>T<sub>LOW</sub> = -55°C for AL Device, -40°C for CL/CP Device T<sub>HIGH</sub> = +125°C for AL Device, +85°C for CL/CP Device

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*</sup>Maximum ratings are those values beyond which damage to the device may occur.

\*\*Power dissipation temperature derating: Plastic "P" package: - 12 mW/°C from 65°C to 85°C.

Ceramic "L" package: - 12 mW/°C from 100°C

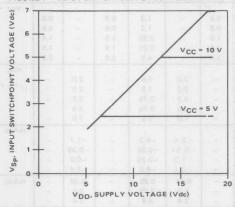
to 125°C.

SWITCHING CHARACTERISTICS (C1 = 50 pF, TA = 25°C)

			Vcc	VDD		Limits		
Characteristic	Symbol	Shifting Mode	Vdc	Vdc	Min	Тур#	Max 280 240 240 240 370 370 350 340 340 340 200 550 290 200 100 80	Unit
Propagation Delay, High to Low	tPHL	TTL-CMOS	5.0	10	- 1	140	280	ns
	- ne V of a 0-4	V <sub>DD</sub> > V <sub>CC</sub>	5.0	15	-	140	280	
		CMOS-CMOS	5.0	10	-	120	240	1
	dia 1	V <sub>DD</sub> > V <sub>CC</sub>	5.0	15	_ 100	120	240	
			10	15		70	140	
	500	CMOS-CMOS	10	5.0	- 1	185	370	1.00
	03 m 60-	V <sub>CC</sub> > V <sub>DD</sub>	15	5.0	S	185	370	
			15	10	-	175	350	
Propagation Delay, Low to High	tPLH	TTL-CMOS	5.0	10	_	170	340	ns
	the device may	V <sub>DD</sub> > V <sub>CC</sub>	5.0	15	LINET INTO	160	320	
	or Onway St	CMOS-CMOS	5.0	10	-	170	340	1
	CONTRACTOR	V <sub>DD</sub> > V <sub>CC</sub>	5.0	15	-	170	340	
		200000	10	15	-	100	200	
		CMOS-CMOS	10	5.0	47.5	275	550	rost i
		VCC > VDD	15	5.0	THE OWNER OF	275	550	1000
	186	Court Court	15	10	-	145	290	
Output Rise and Fall Time	tTLH, tTHL	ALL	11-1	5.0	-	100	200	ns
	6		-	10	1000-170	50	100	Memo
	0		-	15	-	40	80	1.50

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - INPUT SWITCHPOINT CMOS to CMOS MODE



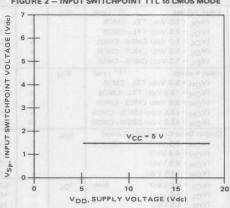


FIGURE 3 - OPERATING BOUNDARY CMOS to CMOS MODE

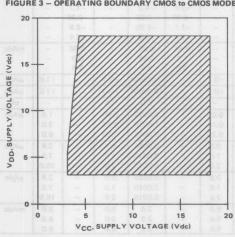
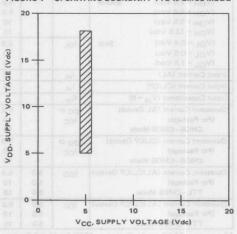


FIGURE 4 - OPERATING BOUNDARY TTL to CMOS MODE





MOTOROLA

MC14506UB

# DUAL 2-WIDE, 2-INPUT EXPANDABLE AND-OR-INVERT GATE

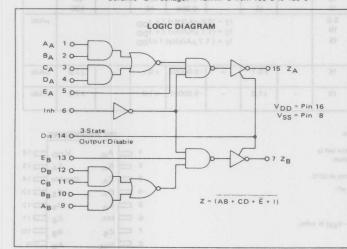
The MC14506UB is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

- 3-State Output
- Separate Inhibit Line
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS\* (Voltages Referenced to Vos)

Symbol	Parameter english	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	-65 to +150	°C
Tı	Lead Temperature (8-Second Soldering)	260	°C

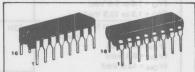
\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C



# **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL EXPANDABLE AND-OR-INVERT GATE



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

### ORDERING INFORMATION

A Series: - 55°C to +125°C

MC14XXXUBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXUBCP (Plastic Package) MC14XXXUBCL (Ceramic Package)

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

# TRUTH TABLE

A	В	C	D	E	INHIBIT	DISABLE	Z
0	0	0	0	1	. 0	0	1
0	X	0	X	1	0	0	1
0	X	X	0-	1	. 0	0	1
X	0	0	X	1	0	0	1
X	0	X	0	1	0	0	1
1	-1	×	X	X	X	0	0
X	X	1	1	X	X	0	0
X	X	X	X	0	X	0	0
X	X	X	X	X	1	0	0
×	×	×	×	X	×	1	High Impedance

X = Don't Care

# ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tio	w°		25°C		Thigh*		
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Uni
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	- 1	0.05	Vdc
Vin = VDD or 0	of the last of the	10	-	0.05	-	0	0.05	-	0.05	-
ten or mandada de		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	_	4.95	_	Vde
Vin = 0 or VDD	*OH	10	9.95	3.19/AC	9.95	10	: ,aguil	9.95	ACI	1
AIN A CO. ADD	0,01	15	14.95		14.95	15	ROLOV	14.95	_	
Input Voltage "0" Level	VII	10	14.55		14.00	10		14.55		Vde
	AIL	5.0	IND THE	1.0	DVA 6	2.25	1.0	NEGBUH	1.0	Val
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		10	wolls n	2.0	control to	4.50	2.0	E how	2.0	Pine.
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		15	162 86	2.5	el suggest	6.75	2.5	Loren et al.	2.5	
(V <sub>O</sub> = 13.5 or 1.5 Vdc) "1" Level		15	10-10	2.0	W 1 - 11	0.75	2.0	-	2.0	-
	VIH		4.0		4.0	TOTAL STATES	Horitonet R	1		
(V <sub>O</sub> = 0.5 or 4.5 Vdc)		5.0	1000000	0 (40)	10.00	2.75	M12-3101	4.0	DE-3512	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	8.0	EDITED X	8.0	5.50	rent ari	8.0	B.1 7086U	.902
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	12.5	: loTange	12.5	8.25	alvīto a	12.5	C ST TURN	12
Output Drive Current (AL Device)	ІОН		7 11 15	1 2 11			.8110	Borigha I		mAd
(VOH = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	-	-0.36	8158-6	10
(VOH = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	- 0.00	-0.9		1 44
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc) Sink	lOL	5.0	0.64	-	0.51	0.88	I II DE TO	0.36	15 EDOLO	mAd
(VOL = 0.5 Vdc)	Carrie II	10	1.6	- 55	1.3	2.25	e esos	0.9	/ viagua	-00
(VOL = 1.5 Vdc)	The same	15	4.2	_	3.4	8.8	-	2.4	_	
Output Drive Current (CL/CP Device)	ГОН			22.30					D. HAGO.	mAd
(VOH = 2.5 Vdc) Source	IOH	5.0	-2.5	NERT BRU	-2.1	-4.2	1 YEAC I	-1.7	Schotlag	1
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	-0.44	-0.88	_	-0.36		
(V <sub>OH</sub> = 9.5 Vdc)	4	10	-1.3	_	-1.1	-2.25		-0.9		-
(VOH = 13.5 Vdc)		15	-3.6	_	-3.0	-8.8	_	-2.4		
011			0.52	-	-			-	THE RESERVE	- 0
(VOL = 0.4 Vdc) Sink	IOL	5.0			0.44	0.88	Sergeral'	0.36	-	mAd
(VOL = 0.5 Vdc)		15	1.3		1.1	2.25	-	0.9	-	-
(V <sub>OL</sub> = 1.5 Vdc)			3.6	10-	3.0	8.8	-	2.4	ignation	.00
Input Current (AL Device)	lin	15	0 - 7000	±0.1	-	±0.00001	±0.1	ov Tune	±1.0	μAd
Input Current (CL/CP Device)	1 <sub>in</sub>	15	- 000	± 0.3	us dies	±0.00001	±0.3	T.T.	±1.0	μAd
Input Capacitance	Cin	-		-	-	5.0	7.5	-	-	pF
(V <sub>in</sub> = 0)			Des			T dis	ESCHOL 100	NO THE		- d-
Quiescent Current (AL Device)	Ipp	5.0	-	1.0	-	0.002	1.0	-	30	μAd
(Per Package)	.00	10	- 000	2.0	_	0.004	2.0	_	60	-
secon Pushing agents a strongs	entire I	15	-	4.0	-	0.006	4.0	-	120	
Quiescent Current (CL/CP Device)	10-	5.0	100 1110	4.0		0.002	4.0		30	-
(Per Package)	IDD	10	-27 GB	8.0	- 199			nma-1 g		μAd
(Per Package)	affew	15	-			0.004	8.0	nex-	60	
L. bloodsU.b.ob Vnslinboro_s	saera I		-	16		0.006	16	1 -	120	-
Total Supply Current * * †	T	5.0			IT = (0	.6 μA/kHz)	f + IDD			μAd
(Dynamic plus Quiescent,	Shop,	10				$.1  \mu A/kHz)$				1
Per Package)	SHIPU : 4	15			IT = (	1.7 µA/kHz	f+IDD			10
(CL = 50 pF on all outputs, all	equing 1 a									1
buffers switching)	19 10				21	-	-01			200
Three-State Leakage Current	ITL	15	-45	± 0.1	- 9	+0.00001	± 0.1	-	±3.0	μAd
(AL Device)									O A	KO.
Three-State Leakage Current	ITL	15	-	±1.0	_	+0.00001	±1.0		± 7.5	µAd-
(CL/CP Device)	1.6									1 10

\*T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

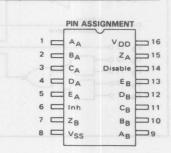
Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: IT is in  $\mu$ A (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.



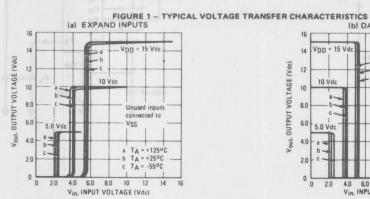
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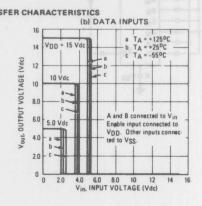
SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

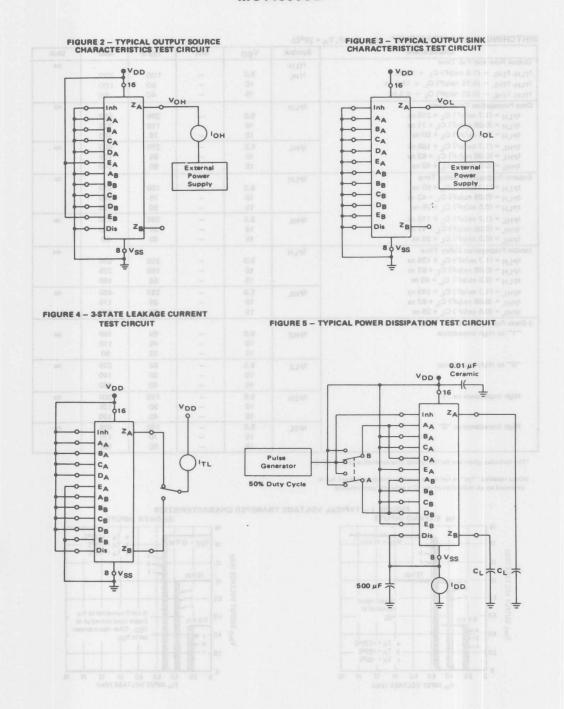
Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH-					ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTHL	5.0		100	200	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns		10	-	50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		15	-	40	80	
Data Propagation Delay Time	tPLH		- process	-0	0015	ns
tpLH = (1.7 ns/pF) CL + 210 ns		5.0	-	295	580	
tpLH = (0.66 ns/pF) CL + 77 ns		10	- FX	110	225	4
tpLH = (0.5 ns/pF) CL + 50 ns		15	10'(-)	75	180	
tpHL = (1.7 ns/pF) CL + 185 ns	tPHL	5.0	-	270	480	ns
$t_{PHI} = (0.66 \text{ ns/pF}) C_1 + 62 \text{ ns}$		10	-	95	175	1
tpHL = (0.5 ns/pF) CL + 40 ns		15	Notes and	65	140	
Expand Propagation Delay Time	tPLH		Values N		45	ns
tpLH = (1.7 ns/pF) CL + 95 ns		5.0	-	180	430	121
tpLH = (0.66 ns/pF) CL + 42 ns		10	-	75	160	
tpLH = (0.5 ns/pF) CL + 25 ns		15	-	50	125	
tpHL = (1.7 ns/pF) CL + 115 ns	tPHL	5.0	-	200	330	ns
tpHL = (0.66 ns/pF) CL + 47 ns		10	- 1	80	110	
tpHL = (0.5 ns/pF) CL + 30 ns		15	-	55	90	
Inhibit Propagation Delay Time	tPLH				9910	ns
tpLH = (1.7 ns/pF) CL + 135 ns		5.0	-	220	500	
tpLH = (0.66 ns/pF) CL + 67 ns		10	-	100	225	
tpLH = (0.5 ns/pF) CL + 40 ns		15	-	65	160	
tpHL = (1.7 ns/pF) CL + 145 ns	tPHL	5.0	-	230	400	ns
tpHL = (0.66 ns/pF) CL + 62 ns		10	-	95	175	
tpHL = (0.5 ns/pF) CL + 35 ns		15	17000000	60	150	A SHUDS
3-State Propagation Delay Time	AGISYT - ITSINUO				O Trur	
"1" to High Impedance	tPHZ	5.0	-	60	150	ns
		10	-	45	110	
		15	-	35	90	
"0" to High Impedance	tPLZ	5.0	-	90	225	ns
		10	-	55	140	
		15	-	40	100	
High Impedance to "1"	tPZH	5.0	-	110	300	ns
		10	- cav	50	125	
		15	- 0	40	100	
High Impedance to "0"	tPZL	5.0	-	170	425	ns
		10	-	70	175	
43		15	-	50	125	

\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

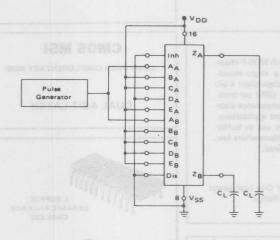


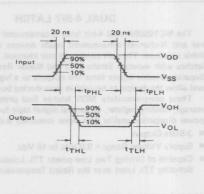




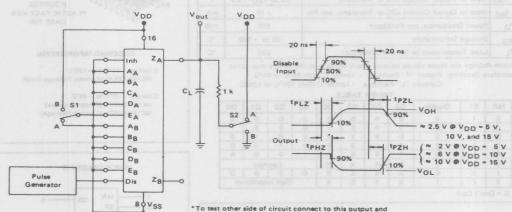
## MC14506UB

## FIGURE 6 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS (Data Inputs)





### FIGURE 7 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS (For 3-State Output)



\*To test other side of circuit connect to this output and change switch (S1) to other expand input (E).

### SWITCH POSITIONS

TEST	S1	S2
tPLZ	A	A
tPHZ	В	В
tPZL	A	A
tPZH	8	В

### **DUAL 4-BIT LATCH**

The MC14508B dual 4-bit latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4-bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired.

- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

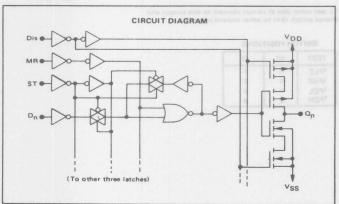
\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C

Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

### TRUTH TABLE

			Contract Con			-				
MR	ST	Disable	D3	D2	D1	DO	03	Q2	Q1	00
0	1	0	0	0	0	0	0	0	0	0
0	100	0	0	0	0	1	0	0	0	1
0	110.	0	0	0	1	0	0	0	1	0
0	1	0	0	1.1.	0	0	0	1	0	0
0	1	0	1	0	0 .	0	1	0	0	0
0	0	0	X	X	X	X		Late	ched	
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X		High I	mpedar	ice

X = Don't Care



## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

**DUAL 4-BIT LATCH** 

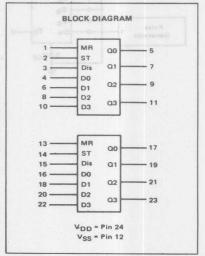




### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tio	w*		25°C		Thi	Thigh*	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05		0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	- 1	0.05	-	0	0.05	soni I tak	0.05	Dumly/O
662 de 1001 de 14 de 15	10.8	15	-	0.05	-	.0	0.05	Flaven 6. I	0.05	LITT
"1" Level	Vон	5.0	4.95	_	4.95	5.0	7 20	4.95	2017	Vdc
$V_{in} = 0 \text{ or } V_{DD}$	On	10	9.95		9.95	10	4 Pat	9.95	The latest	5.177
		15	14.95	_	14.95	15	SIE SO A	14.95	dad <del>v</del> oid	Pinna
nput Voltage "0" Level	VIL	11191				an B	7+156	11,7 miles	e dayet a	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	01	5.0		1.5		2.25	1.5	inn 20.01	1.5	1
(VO = 9.0 or 1.0 Vdc)	. 25	10		3.0	_ "	4.50	3.0	(6.5-rutp)	3.0	one -
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	D 9 7	15	-	4.0	-	6.75	4.0	A-101	4.0	
"1" Level	VIH									
(VO = 0.5 or 4.5 Vdc)	20	5.0	3.5	-	3.5	2.75	_	3.5	-	Vdc
(VO - 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50		7.0		
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	0.8	15	11.0	m1=25	11.0	8.25	9	11.0	eB mmA	resount
Output Drive Current (AL Device)	ТОН				1					mAdo
(VOH = 2.5 Vdc) Source	On	5.0	-3.0	_	-2.4	-4.2	_	-1.7	_	
(V <sub>OH</sub> = 4.6 Vdc)	0.0	5.0	-0.64	_	-0.51	-0.88	_	-0.36	OW THE	ndont2
(V <sub>OH</sub> = 9.5 Vdc)	Dr.	10	-1.6	_	-1.3	-2.25		-0.9	_	
(VOH = 13.5 Vdc)	at 1	15	-4.2	-	-3.4	-8.8	-	-2.4	-	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88		0.36	-100	mAd
(VOL = 0.5 Vdc)	OL	10	1.6		1.3	2.25	_	0.9	don't or	1
(V <sub>OL</sub> = 1.5 Vdc)	WF 13	15	4.2		3.4	8.8	_	2.4	_	
Output Drive Current (CL/CP Device)	ГОН		1.2	-	-	0.0				mAd
(V <sub>OH</sub> = 2.5 Vdc) Source	ЮН	5.0	-2.5		-2.1	-4.2		-1.7	emi an turibus	Incid
(V <sub>OH</sub> = 4.6 Vdc)	53	5.0	-0.52		-0.44	-0.88		-0.36		
(VOH = 9.5 Vdc)		10	-1.3	_	-1.1	-2.25		-0.9		
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6		-3.0	-8.8	agray 7	-2.4	11600:91	18-8
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	_	0.44	0.88	-	0.36	-	mAde
(VOL = 0.5 Vdc)		10	1.3		1.1	2.25		0.9		III
(VOL = 1.5 Vdc)	01	15	3.6		3.0	8.8	112 - 1	2.4	_	
Input Current (AL Device)	107	15	-	± 0.1	-	±0.00001	± 0.1		± 1.0	μAdo
Control of the Contro	lin	15	-	± 0.3	1	±0.00001	± 0.3		±1.0	μAdd
Input Current (CL/CP Device)	Iin				-	-		-		-
Input Capacitance	Cin	- 1		-	-	5.0	7.5	-	Title	pF
(V <sub>in</sub> = 0)	[2]									-
Quiescent Current (AL Device)	IDD .	5.0	-	5.0	-	0.005	5.0	11, 40, 60	150	μAde
(Per Package)	the state of the	10	-	10	-	0.010	10	-	300	
	985	15		20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20	-	150	μAde
(Per Package)		10	-	40	-	0.010	40	I'U" AT SON	300	925
018   301 -	0.0	15	-	80	-	0.015	80	-	600	
Total Supply Current**†	IT	5.0	1 3 9		IT = (1	.46 μA/kHz	f + Ipp			μAd
(Dynamic plus Quiescent,	01	10			IT = (2	.91 μA/kHz	) f + IDD			
Per Package)		15			1T = (4	.37 μA/kHz	If + IDD			Pol-out
(C <sub>L</sub> = 50 pF on all outputs, all	Sylle In St									
buffers switching)					0 100 days	SANG THE BUYE	RIT DEED NO	for lon in "t	pyT belied	1 215/2
Three-State Leakage Current (AL Device)	ITL	15	-	± 0.1	- Augmiss	+0.00001	± 0.1	100 1100 1100	±3.0	μAde
Three-State Leakage Current	1	15	20040000	±1.0	-	+0.00001	± 1.0	-	± 7.5	μAd
(CL/CP Device)	ITL	15	THE PERSON NAMED IN	11.0		0.00001	11.0		17.5	μΑα

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_{T}$  is in  $\mu A$  (per package),  $C_{L}$  in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.008.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device.
T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

					GG 1			All Types		
	haracteristic		A SOUTH	1	Symbol	VDD	Min	Тур#	Max	Uni
Output Rise and Fall Time					tTLH.	90	10000		11000000	ns
tTLH, tTHL = (1.5 ns/pF) CL +	25 ns				THL	5.0	-	100	200	HIS .
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns						10	-	50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns					5.8	15	dang n	40	80	alk .
Propagation Delay Time, Dn or MR to Q		56/61		14.95	tPLH.					ns
tpLH, tpHL = (1.7 ns/pF) CL +	135 ns				tPHL	5.0	Wa. H 31	220	440	V rose
tpLH, tpHL = (0.66 ns/pF) CL	+ 57 ns				19.8	10	-	90	180	In WE
tpLH, tpHL = (0.5 ns/pF) CL +	35 ns				- 01	15	-	60	120	10000
Master Reset Pulse Width	6/ 6		0.0		tWH(R)	5.0	200	100	10.40	ns
						10	100	50	-	
					5.0	15	70	35	1022.5	OVI
Master Reset Removal Time	38.30	0.81		015	trem	5.0	30	- 15	1000	ns
						10	25	0	100	200
						15	20	0	Tail twitt	No Gir
Strobe Pulse Width	88.0-	18-0-		100	twH(S)	5.0	140	70	V. Tav	ns
					003	10	70	35	V = 0	CALL
					di la	15	40	20	1 E	200
Setup Time	89.0	F8.D		98.0	tsu	5.0	50	25	V ( <del>e</del> 0)	ns
Data to Strobe					01	10	20	10	V 200	nVi
- 1 25 1 -					- 16	15	10	5.0	1200	0.80
Hold Time	4.4				th	5.0	50	20	hu Devoit	ns
Strobe to Data					0.8	10	35	10	1 22	101/1
- 06.0-	18.0	88.0		58.0 -	0.8	15	35	10	-	OWY
3-State Propagation Delay Time					tPHZ				A 878-1	ns
Output "1" to High Impedance					0.0			(95)	2.61	Calva
					91	5.0	- 1	55	170	OAL
					21	10	-	35	100	OAL
					-	15	-	30	70	9V1
Output "0" to High Impedance					tPLZ	50	-	75	470	O Teste
						5.0		75 40	170	O ruge
						15	_	35	70	O ruga
High Impedance to "1" Level					10711	-				
3000 1 14 1 Or					<sup>t</sup> PZH	5.0		80	170	SUSTAIN SUSTAIN
					l ar	10	_	35	100	1
						15	_	30	70	-
High Impedance to "0" Level							18.00	ME WILLIAM		7.54
ana ana ana ana ana ana ana ana ana ana					tPZL	5.0	_	105	010	19/91
					A STATE OF THE STA	10	_	105 <b>50</b>	210 100	
					0.7	15		35	70	S min
					1 00	10	_	30	/0	A COL

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

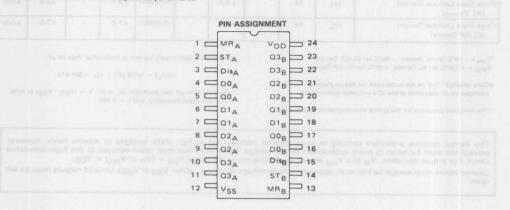
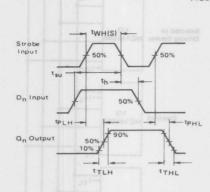


FIGURE 1 - AC WAVEFORMS



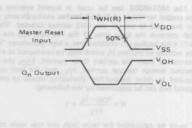
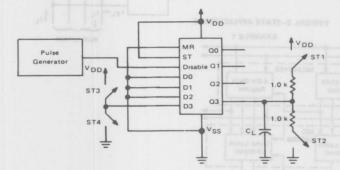
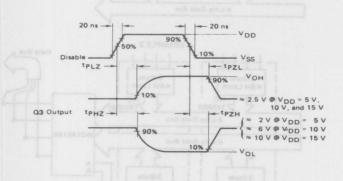


FIGURE 2 - 3-STATE AC TEST CIRCUIT AND WAVEFORMS



TEST	ST1	ST2	ST3	ST4
tPHZ	OPEN	CLOSE	CLOSE	OPEN
tPLZ	CLOSE	OPEN	OPEN	CLOSE
tPZL	CLOSE	OPEN	OPEN	CLOSE
tPZH	OPEN	CLOSE	CLOSE	OPEN



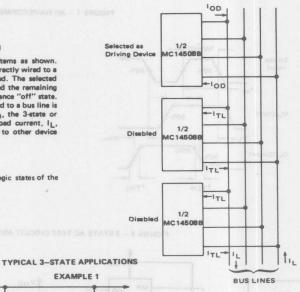
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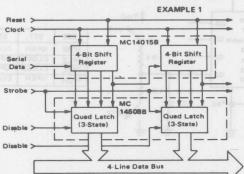
### 3-STATE MODE OF OPERATION

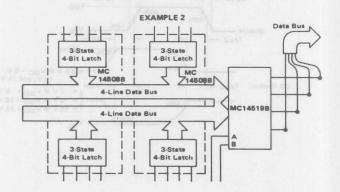
The MC145088 can be used in bussed systems as shown. The output terminals of N 4-bit latches can be directly wired to a bus line, and to one of the 4-bit latches selected. The selected latch controls the logic state of the bus line, and the remaining (N-1) 4-bit latches are disabled into a high impedance "off" state. The number of latches, N, which may be connected to a bus line is determined from the output drive current, I<sub>DD</sub>, the 3-state or disabled output leekage current, I<sub>TL</sub>, and the load current, I<sub>L</sub>, required to drive the bus line (including fanout to other device inputs) and can be calculated by the following:

$$N = \frac{I_{OD} - I_{L}}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.









## BCD UP/DOWN COUNTER

The MC14510B synchronous up/down BCD counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide type T flip-flop capability.

This counter can be preset by applying the desired value in BCD to the Preset inputs (P1, P2, P3, P4) and then bringing the Preset Enable (PE) high. The direction of counting is controlled by applying a high (for up counting) or a low (for down counting) to the UP/DOWN input. The state of the counter changes on the positive transition of the clock input.

Cascading can be accomplished by connecting the Carry Out to the Carry In of the next stage while clocking each counter in parallel. The ouputs (Q1, Q2, Q3, Q4) can be reset to a low state by applying a high to the Reset (R) pin.

This CMOS counter finds primary use in up/down and difference counting. Other applications include: (1) Frequency synthesizer applications where low power dissipation and/or high noise immunity is desired, (2) Analog-to-digital and digital-to-analog conversions, and (3) Magnitude and sign generation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads or One Lowpower Schottky TTL Load Over the Rated Temperature Range.

### MAXIMIM BATINGS\* (Voltages Referenced to Voc)

Symbol	Parameter Otto	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C
Ceramic "L" Package: -12mW/°C from 100°C to 125°C

### TRUTH TABLE

Carry In	Up/Down	Preset Enable	Reset	Clock	Action
1	X	0 49	0	×	No Count
0	E 1 E 9	0	0		Count Up
0	0	0	0		Count Down
X	X	1 10	0	Х	Preset
X	×	×	1	X	Reset

X = Don't Care

Note: When counting up, the Carry Out signal is normally high, and is low only when Q1 and Q4 are high and Carry In is low. When counting down, Carry Out is low only when Q1 through Q4 and Carry In are low.

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)
BCD UP/DOWN COUNTER

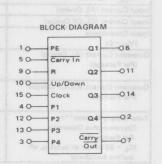


L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)



V<sub>DD</sub> = Pin 16 V<sub>SS</sub> = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tio	w*		25°C		Thi	gh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05		0	0.05	- 1	0.05	Vdc
Vin VDD or 0	-	10	-	0.05	-	0	0.05	- 1	0.05	
55		15	-	0.05		0	0.05		0.05	
"1" Level	VOH	5.0	4.95	10	4.95	5.0		4.95		Vdc
Vin = 0 or VDD	· OH	10	9.95	Munico.	9.95	10	margan	9.95	P COMP	1
SAME ASSESSED TO THE PARTY PROPERTY OF THE PARTY OF THE P	10.01	15	14.95	HUDTER	14.95	15	Somano	14.95	Dilyi bat	unie
nput Voltage "0" Level	VIL		100					1		Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	11.	5.0	Sandar a	1.5	Mercal Co.	2.25	1.5	1531584 S	1.5	1
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10		3.0	at Bay	4.50	3.0	- 1	3.0	Cap
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	de colonia	15	-	4.0	an Sulk	6.75	4.0	PLBD 19	4.0	Lana .
"1" Level	VIH			1.0		0.110				
(VO = 0.5 or 4.5 Vdc)	- 111	5.0	3.5	Son Bar Rus	3.5	2.75	Dec man	3.5	OSMS 13	Vdc
(VO = 1.0 or 9.0 Vdc)	Sin I	10	7.0	in invent	7.0	5.50	muoo q	7.0	a gar	1
(V <sub>Q</sub> = 1.5 or 13.5 Vdc)		15	11.0	Uniario 1	11.0	8.25	d out	11.0	NUDM.	961
Output Drive Current (AL Device)	Law	10	11.0	N 100 1	11.0	0.20	>	11.0	CEST DI	mAdc
(VOH = 2.5 Vdc) Source	ІОН	5.0	-3.0	and dark for	-2.4	-4.2		-1.7		MAGC
(VOH = 4.6 Vdc)		5.0	-0.64	and the said	-0.51	-0.88	MATERIAL DE	-0.36	OT ZIME	SET .
	1 1 3	10	-1.6	OF IT W	-1.3	-2.25	AT THE	-0.36	UD. BATS	pils
(V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	APPEN .	15	-4.2	fore mis	-3.4	-8.8	007001	-2.4	R 6 QUIL	lide
STATE OF THE STATE			-	100 - 100	_		11 E 10 H	-	110000	1
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	( <del>-</del> 110)	0.51	0.88	BU-SIES	0.36	O FIRM	mAdc
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	M1 (= 711)	1.3	2.25	in <del>-</del> oq v	0.9	an <del>a</del> liga	1038
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	man + m	3.4	8.8	OL-ECTRI	2.4	70	(Fitt)
Output Drive Current (CL/CP Device)	IOH				-11010293	sun often		In Sevin		mAdc
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	anl TitA	-1.70	with any	0
(V <sub>OH</sub> = 4.6 Vdc)	S 11	5.0	-0.52	-	-0.44	-0.88	-	-0.36	_	
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	7.6- 30	-0.9	ow Appli	100
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	no Fano	-2.4	M.T.	1
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	witten	0.44	0.88		0.36	-	mAdc
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3	-	1.1	2.25	BASH I	0.9	0.0 _00,0	
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8	-	2.4	0 10 310	
nput Current (AL Device)	lin	15	-	± 0.1	- 1	±0.00001	±0.1	190 E-01101	± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	ed_and	± 0.3	1 -1	±0.00001	± 0.3	NUMBER 1	±1.0	μAdc
nput Capacitance	Cin	_	gnen bi	rotogn	200	5.0	7.5	-	-	pF
(V <sub>in</sub> = 0)	olu					0.0	7.0			
Quiescent Current (AL Device)	IDD	5.0	-	5.0	12.7	0.005	5.0	200	150	μAdc
(Per Package)	'DD	10	-cutat	10	-	0.010	10		300	Ande
HO-SE N-OB		15	- Venture	20	-	0.015	20	_	600	10320
2	1		1		-				-	
Quiescent Current (CL/CP Device)	IDD	5.0	St cav	20	-	0.005	20 40	Nov term	150	μAdc
(Per Package)		10	-	40	-	0.010		_	300	1000
	1		-	80		0.015	80	-	600	-
Total Supply Current**†	IT	5.0	902			.58 μA/kHz				μAdc
(Dynamic plus Quiescent,		10	987 4 62			1.2 µA/kHz)				
Per Package)		15	1		IT = (1	1.7 µA/kHz)	f + IDD			1
(CL = 50 pF on all outputs, all			1000							1 1
buffers switching)	18		Dan yamir							of the second

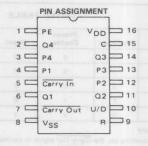
 $^{*}T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C. †To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts, f in kHz is input frequency, and k = 0.001.



SWITCHING CHARACTERISTICS\* ( $C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$ , See Figure 2)

				All Types		
Characteristic	Symbol	V <sub>DD</sub>	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH.	A. L. B.				ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTHL	5.0	_	100	200	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns	THE	10		50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		15	_	40	. 80	
Propagation Delay Time	tpLH,	100			7	ns
Clock to Q	tPHL					ns
tpLH, tpHL = (1.7 ns/pF) C <sub>L</sub> + 230 ns	PHL	5.0		315	630	
tpLH, tpHL = (0.66 ns/pF) CL + 97 ns	1 0	10	-	130	260	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns	-0	15	100	100	200	
Clock to Carry Out	tour	C15				ns
tpLH, tpHL = (1.7 ns/pF) C <sub>L</sub> + 230 ns	tPLH,	5.0		315	630	110
tpLH, tpHL = (0.66 ns/pF) CL + 97 ns	FIL	10		130	260	
tpLH, tpHL = (0.5 ns/pF) C <sub>L</sub> + 75 ns	1 1	15	_	100	200	
Carry In to Carry Out						ns
tpLH, tpHL = (1.7 ns/pF) C <sub>L</sub> + 230 ns	tPLH,	5.0		180	360	115
tp <sub>LH</sub> , tp <sub>HL</sub> = (0.66 ns/pF) C <sub>L</sub> + 47 ns	tPHL	10		80	160	
tpLH, tpHL = (0.5 ns/pF) CL + 35 ns		15		60	120	
		.0		00	.20	
Preset or Reset to Q	tPLH,	5.0		245	630	ns
tplH, tpHL = (1∜7 ns/pF) C <sub>L</sub> + 230 ns	<sup>t</sup> PHL	5.0	31010	315 130	260	
$t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$		10 15		100	200	
$t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$		15	-	100	200	
Preset or Reset to Carry Out	tPLH,	100,000				ns
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$	<sup>t</sup> PHL	5.0	_	550	1100	
$t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 192 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$		10	-	225	450	
TPLH, TPHL = (U.5 NS/PF) CL + 125 NS		15	_	150	300	
Reset Pulse Width	tw(H)	5.0	360	180	_	ns
		10	210	105	_	
		15	160	80	_	
Clock Pulse Width	1	5.0	350	200		ns
Clock Pulse Width	tw(H)	10	170	100	-9	115
	-	15	140	75		
And the second s	10.0		140			
Clock Pulse Frequency	fcl	5.0		3.0	1.5	MHz
	100	10	-	6.0	3.0	
	and the second	15	_	8.0	4.0	
Preset or Reset Removal Time	trem	5.0	650	325	_	ns
The Preset or Reset Signal must be low prior to a	10111	10	230	115		
positive-going transition of the clock.		15	180	90	-	
Clock Rise and Fall Time	t	5.0	_		15	μs
Clock That and Fall Time	tTLH,	10			5	до
	tTHL	15	_	_	4	
Setup Time	tsu	5.0	260	130		ns
Carry In to Clock		10	120	60	_	
		15	100	50		
Hold Time	th	5.0	0	- 50	_	ns
Clock to Carry In	Inches and	10	10	- 15	_	
		15	10	-5	-	
Setup Time		5.0	500	250	9	
Up/Down to Clock	tsu	10	200	100	D	ns
Op Down to Olock		15	175	75		
and the first and						
Hold Time	th	5.0	-70	-140	-	ns
Clock to Up/Down		10	-30	- 80		
	44	15	- 20	- 50	nervir -	
Setup Time	t <sub>su</sub>	5.0	-50	- 100		ns
Pn to PE	'su	10	-30	-65	_	
Hav	1916	15	-25	- 55	_	
Held The			200		D 10 100	
Hold Time	th	5.0	480	240	_	ns
PE to Pn		10	410	205		
1 1/09/95		15	410	205	_	
Preset Enable Pulse Width	twH	5.0	200	100	_	ns
	1	10	100	50	_	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

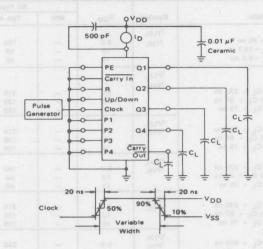
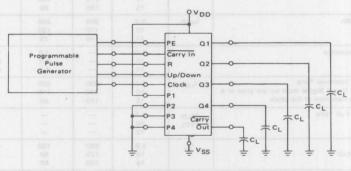
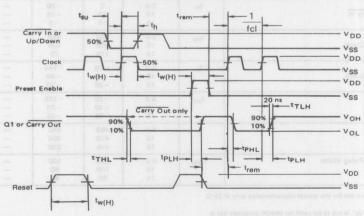
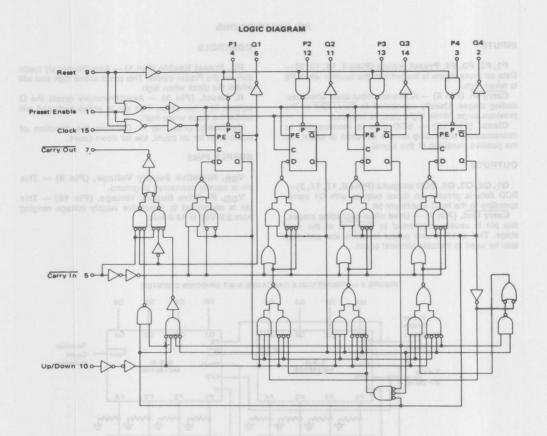


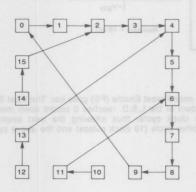
FIGURE 2 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



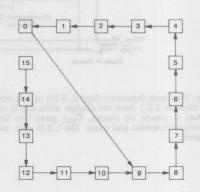




### STATE DIAGRAM FOR UP COUNTING



### STATE DIAGRAM FOR DOWN COUNTING



### PIN DESCRIPTIONS

### INPUTS

P1, P2, P3, P4, Preset Inputs (PIns 4, 12, 13, 3) — Data on these inputs is loaded into the counter when PE is taken high.

Carry In, (Pin 5) — Active-low input used when cascading stages. Usually connected to Carry Out of the previous stage. While high, clock is inhibited.

Clock, (Pin 15) — BCD data is incremented or decremented, depending on the direction of count, on the positive transition of this signal.

### **OUTPUTS**

Q1, Q2, Q3, Q4, BCD outputs (Pins 6, 11, 14, 2)—BCD data is present on these outputs with Q1 corresponding to the least significant bit.

Carry Out, (PIn 7) — Used when cascading stages, this pin is usually connected to Carry in of the next stage. This synchronous output is active low and may also be used to indicate terminal count.

### CONTROLS

PE, Preset Enable (Pin 1) — Asynchronously loads data on the Preset Inputs. This pin is active high and will inhibit the clock when high.

R, Reset, (Pin 9) — Asynchronously resets the Q outputs to a low state. This pin is active high and will inhibit the clock when high.

Up/Down, (PIn 10) — Controls the direction of count: high for up count, low for down count.

### SUPPLY PINS

VSS, Negative Supply Voltage, (Pin 8) — This pin is usually connected to ground.

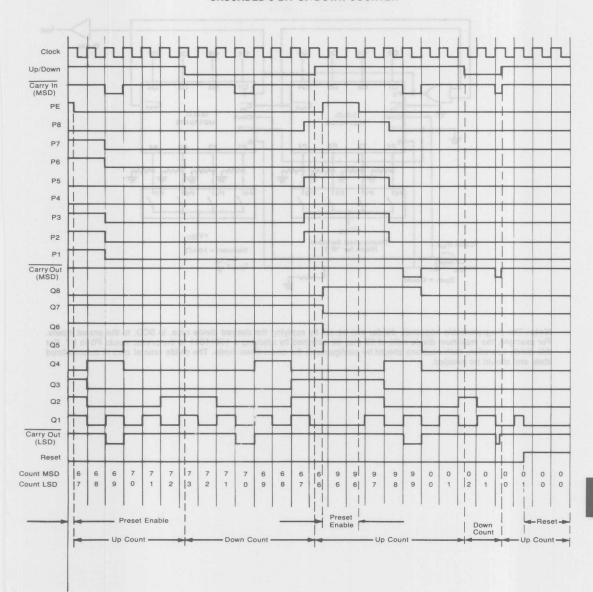
VDD, Positive Supply Voltage, (Pin 16) — This pin is connected to a positive supply voltage ranging from 3.0 Vdc to 18.0 Vdc.

#### FIGURE 3 — PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER Q8 02 03 04 01 Preset Enable Q4 Q1 Q3 0 = Count Terminal 1 = Preset Cout Cin Cin Count L.S.D. M.S.D. Indicator Clock Clock MC14510B MC14510B 1 =' Up U/D U/D 0 = Down P P3 P4 +VDD +VDD umbwheel Switches (Open for "0") Resistors = 10 kΩ Rese +VDD Open = Count

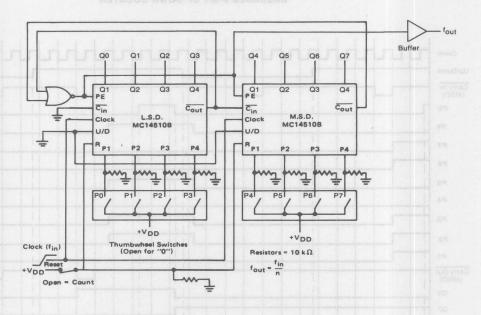
6

**Note:** The Least Significant Digit (L.S.D.) counts from a preset value once Preset Enable (PE) goes low. The Most Significant Digit (M.S.D.) does not change while  $\overline{C}_{in}$  is high. When the count of the L.S.D. reaches 0 (count down mode) or reaches 9 (count up mode),  $\overline{C}_{out}$  goes low for one complete clock cycle, thus allowing the next counter to decrement/increment one count. The L.S.D. now counts through another cycle (10 clock pulses) and the above cycle is repeated.

## TIMING DIAGRAM FOR THE PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER



### FIGURE 4 — PROGRAMMABLE CASCADED FREQUENCY DIVIDER



**Note:** The programmable frequency divider can be set by applying the desired divide ratio, in BCD, to the preset inputs. For example, the maximum divide ratio of 99 may be obtained by applying a 10011001 to the preset inputs P0 to P7. For this divide operation, both counters should be configured in the count down mode. The divide ratio of zero is an undefined state and should be avoided.



## MC14512B

### 8-CHANNEL DATA SELECTOR

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Diode Protection on All Inputs
- Single Supply Operation
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin-lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

### TRUTH TABLE

C	В	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	⊙ 1·	0	0	Х3
1	0	. 0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
×	×	X	×	1	High Impedance

X = Don't Care

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

8-CHANNEL DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

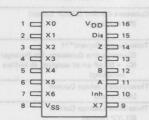
P SUFFIX
PLASTIC PACKAGE
CASE 648

### ORDERING INFORMATION

A Series: -55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: IT is in  $\mu A$  (per package), CL in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.001.

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

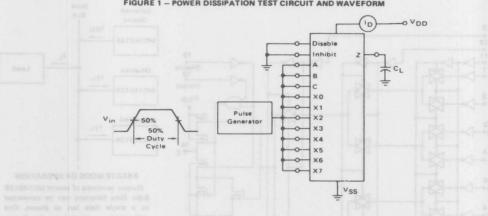
<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

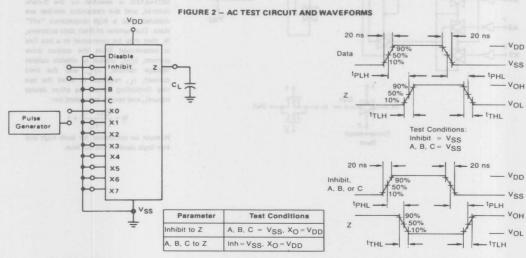
SWITCHING CHARACTERISTICS (C<sub>1</sub> = 50 pF, T<sub>A</sub> = 25°C, See Figure 1)

			All T	ypes	
Characteristic	Symbol	V <sub>DD</sub>	Typ #	Max	Unit
Output Rise and Fall Time $\label{eq:true} \begin{array}{l} \text{Tuth. TrHL} = (1.5 \text{ ns/pF}) \text{ C}_L + 25 \text{ ns} \\ \text{TrH. TrHL} = (0.75 \text{ ns/pF}) \text{ C}_L + 12.5 \text{ ns} \\ \text{TrH. TrHL} = (0.55 \text{ ns/pF}) \text{ C}_L + 9.5 \text{ ns} \end{array}$	ttlh, tthl	5.0 10 15	100 50 40	200 100 80	ns
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	<sup>t</sup> PLH	5.0 10 15	330 125 85	650 250 170	ns
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	<sup>†</sup> PHL	5.0 10 15	330 125 85	650 250 170	ns
3-State Output Delay Times (Figure 3) "1" or "0" to High Z, and High Z to "1" or "0"	tPHZ, tPLZ, tPZH, tPZL	5.0 10 15	60 35 30	150 100 75	ns

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

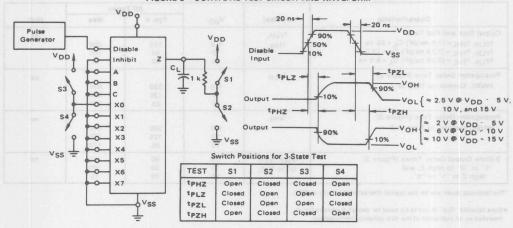
FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



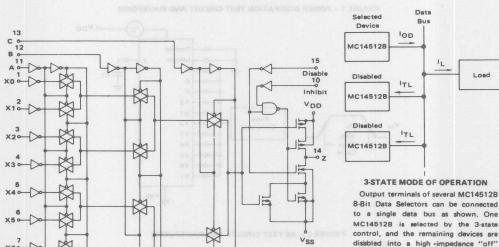


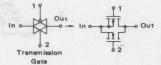
<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.





### LOGIC DIAGRAM





MC14512B is selected by the 3-state control, and the remaining devices are disabled into a high impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I<sub>OD</sub>, 3-state or disable output leakage current, I<sub>TL</sub>, and the load current, I<sub>L</sub>, required to drive the bus line (including fanout to other device

$$\dot{N} = \frac{1}{1} \frac{1}{1} + 1$$

inputs), and can be calculated by:

N must be calculated for both high and low logic state of the bus line.



## MC14514B MC14515B

### 4-BIT TRANSPARENT LATCH/4-TO-16 LINE DECODER

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical "1" at the selected output, whereas the MC14515B (output active low option) presents a logical "0" at the selected output. The latches are R-S type flip-flops which hold the last input data presented prior to the strobe transition from "1" to "0". These high and low options of a 4-bit latch/4 to 16 line decoder are constructed with N-channel and P-channel enhancement mode devices in a single monolithic structure. The latches are R-S type flip-flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C
Ceramic "L" Package: -12mW/°C from 100°C to 125°C

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

4-BIT TRANSPARENT LATCH/4-TO-16 LINE DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

### ORDERING INFORMATION

A Series: - 55°C to + 125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

			-		
BLOCK DIAGRA	AM		SO	11 o Ā	BCC
199 00 4	arti milio abe	Har Joernio A	S1	9 O A	BCC
V <sub>DD</sub> = Pin			S2	OĀ	всс
VSS = Pin	12	Fig. 02)71 + (	53	OA	BCC
pullary of the V - mid	B - V Again	J (imalase	S4	-0 A	BCD
Data 1 0 2	A 100	C = A bring glan	S5	OA	B C C
3 Transpar	ent B		S6	5 O Ā	
Data 2 O	-	4 to 16	S7		всб
Data 3 O 21. Latch	C	Decoder	S8	18 O A	BCC
	Page 1	anp abaus	59	17 O A	BCC
Data 4 0 22	D	of the latter of	\$10	OĀ	BCC
	at bee	sthered ed	\$11	OA	BCC
1			\$12	OA	BCC
Strobe O		wyst opatics	513	OA	BCC
			514	16 O A	BCC
			S15	15 O A	BCC

	1	ATA	INPUT	SELECTED OUTPUT	
INHIBIT	D	С	В	A	MC14514 = Logic "1" MC14515 = Logic "0"
0	0	0	0	0	SO SO
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	\$3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	\$6
0	0	1	1	1	S7
0	1	0	0	0	\$8
0	1	0	0	1	\$9
0	1	0	0.153	0	S10
0	1 days	0	1	001	S11
0	1.	111	0	0	S12
0	11	0.17	0	erist.	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	×	×	Χ.	×	All Outputs = 0, MC 1451 All Outputs = 1, MC 1451

X = Don't Care
\*Strobe = 0, Data is latched

ELECTRICAL CHARACTERISTICS (Voltages Referenced to Vss)

		VDD	Tie	ow*		25°C		Thi	igh *	1
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Uni
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdd
Vin = VDD or 0	02	10	-	0.05		0	0.05	_	0.05	
III 00		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	G 3561 1	4.95	5.0	U TM3	4.95	AST	Vde
Vin = 0 or VDD	- OH	10	9.95	n smin	9.95	10	en carrie	9.95	WHEN E 113	- 210
ON POWER COMPLEMENTARY MOS	01	15	14.95	roizan se	14.95	15	MEDM 6	14.95	MOM et	1
nput Voltage "0" Level	VIL		The Tues	161 HAT	0.7 (3)(0)	10	tie loss	1710 Yes	000 D 3n	Vd
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	-IL	5.0	MARKET I	1.5		2.25	1.5	memo	1.5	land of
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	1. 2. 1. 1.	10	Por Lines	3.0	market for	4.50	3.0		3.0	and a
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	18-4	15	10 - 100 cm	4.0	Strange Inc	6.75	4.0	1	4.0	- Control
"1" Level	VIH	13	SEL STATUS	4.0	1 10000	0.75		1100100	4.0	Vdc
(VO = 0.5 or 4.5 Vdc)	AIH	5.0	3.5	KONTROVENIO	2.5	2.75		3.5	2365t H 3556	200
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	A CHESSEL TO F	of Milos	3.5	100000000000000000000000000000000000000	0.1001 1	The second of	early s	-07
			7.0	na leani	7.0	5.50	if min	7.0	on Pag 1	Dab
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	State and	11.0	8.25	in Tark	11.0	contrate p	loon.
Output Drive Current (AL Device)	ІОН	. 9	10 500	cioni, ban	ice a po	to listrin	15 21 SE	o bos a		mAd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-1.2	- 1	-1.0	-1.7	and one	-0.7	rutes a	STEE
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.25	ento pri d	-0.2	-0.36	omin vae	-0.14	nos seud	1
(V <sub>OH</sub> = 9.5 Vdc)		10	-0.62	-	-0.5	-0.9	and the same	-0.35	and when	non-
(V <sub>OH</sub> = 13.5 Vdc)		15	-1.8	1 9000	-1.5	-3.5	SELECT NO. 10	-1.1		12000
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36		mAd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.25	5 5 - 1	0.9	di Tana	1
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	- 11	2.4	A Tributa	
Output Drive Current (CL/CP Device)	ЮН	1000	N. BANCO	30 ID 8	002	The state of	Out the	District Co.	2 20 112 90	mAd
(VOH = 2.5 Vdc) Source		5.0	-1.0	90023	-0.8	-1.7	WHIT ISAC	-0.6	T valitoria	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.2	-	-0.16	-0.36	-	-0.12	-	
(V <sub>OH</sub> = 9.5 Vdc)		10	-0.5	-	-0.4	-0.9	-	-0.3	-	100
(VOH = 13.5 Vdc)		15	-1.4	-	-1.2	-3.5	_	-1.0	-	1
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	III amount	0.36	HT HILL	mAd
(V <sub>OL</sub> = 0.5 Vdc)	0.	10	1.3	-	1.1	2.25	-	0.9	_	1
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8	Situation.	2.4		tou
Input Current (AL Device)	lin	15	202	±0.1	-	±0.00001	±0.1	OF THE PARTY	±1.0	μAd
Input Current (CL/CP Device)		15	0 -250	±0.3		±0.00001	± 0.3	1000	±1.0	μAd
	lin			-	-	-				-
(V <sub>in</sub> = 0)	Cin	IV/m	- 01	-	mi'S +mg	5.0	7.5	neG-augh	O SHUNN	pF
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAd
(Per Package)	00	10	001 - 0	10	-	0.010	10	Pulate on	300	9 0
Service Chains Income		15	- 08	20	-	0.015	20	i a-dam	600	
Quiescent Current (CL/CP Device)	IDD	5.0	pro-same	20	01 Epon	0.005	20	WV 430.00	150	μΑσ
(Per Package)	.00	10	_30	40	mont_544	0.010	40	100-00	300	Jar.
		15	07201	80	on Spron	0.015	80	me_60	600	
Total Supply Current**†	IT	5.0		1 00	114				000	1.0
(Dynamic plus Quiescent,		10			T = (1	.35 μA/kHz .70 μA/kHz	DD			LAC
Per Package)	F 360036	15				.05 μA/kHz				
(CL = 50 pF on all outputs, all		15	-		T-(4	.υο μΑ/κΗΖ	ססי דיי			
buffers switching)	1/69									

\*T<sub>IOW</sub> = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

## MC14514B•MC14515B

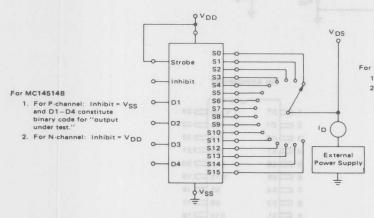
SWITCHING CHARACTERISTICS\* (C1 = 50 pF, TA = 25°C)

		4	9	All Types		
Characteristic	Symbol	VDD	Min	Тур#	Typ # Max	
Output Rise Time	tTLH	华 007 李	() 0			ns
tTLH = (3.0 ns/pF) C1 + 30 ns	73171916 100.21	5.0	-	180	360	
tTLH = (1.5 ns/pF) C1 + 15 ns		10	- 1	90	180	
t <sub>TLH</sub> = (1.1 ns/pF) C <sub>L</sub> + 10 ns		15	1600	65	130	
Output Fall Time	tTHL		100		naturii - I	ns
t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns		5.0	10	100	200	
tTHL = (0.75 ns/pF) C <sub>1</sub> + 12.5 ns		10	- PP	50	100	
t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		15	50	40	80	
Propagation Delay Time; Data, Strobe to S	tPLH,		400000			ns
tpLH, tpHL = (1.7 ns/pF) CL + 465 ns	tPHL	5.0	1000-	550	1100	
tpLH, tpHL = (0.66 ns/pF) CL + 192 ns	- 100	10	-	225	450	
tpLH, tpHL = (0.5 ns/pF) CL + 125 ns	- 30	15	-12	150	300	
Inhibit Propagation Delay Times	tPLH,		11			ns
tpLH, tpHL = (1.7 ns/pF) CL + 315 ns	tPHL	5.0	-	400	800	
tpLH, tpHL = (0.66 ns/pF) CL + 117 ns		10	-	150	300	
tPLH, tPHL = (0.5 ns/pF) CL + 75 ns		15	- 1	100	200	
Setup Time	t <sub>su</sub>					ns
Data to Strobe		5.0	250	125	-	
BARD HEVARE GRAD	TRUCKERS SHOT	10	100	50	-	
		15	75	38	_	
Hold Time	th	5.0	- 20	- 100		ns
Strobe to Data		10	0	- 40	-	
		15	10	- 30	-	
Strobe Pulse Width	twH		E 5003121	41-		ns
	I E Jugrud O-	5.0	350	175	-	
	100	10	100	50		
00V	200	15	75	38	1 - 3	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### FIGURE 1 - DRAIN CHARACTERISTICS TEST CIRCUIT



For MC14515B

- 1. For P-channel: Inhibit = V<sub>DD</sub>
- For N-channel: Inhibit = VSS and D1-D4 constitute binary code for "output under test."

## MC14514B•MC14515B



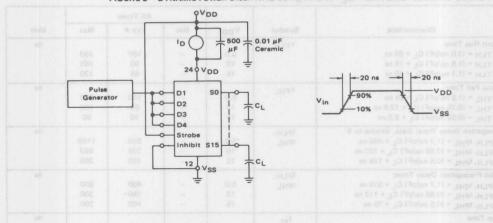
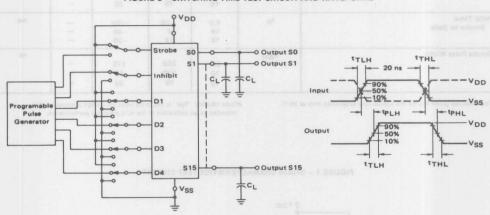
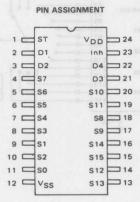
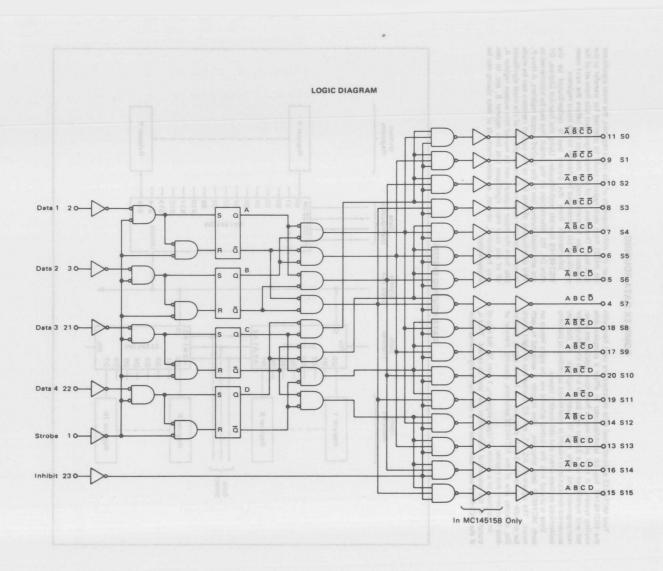


FIGURE 3 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS







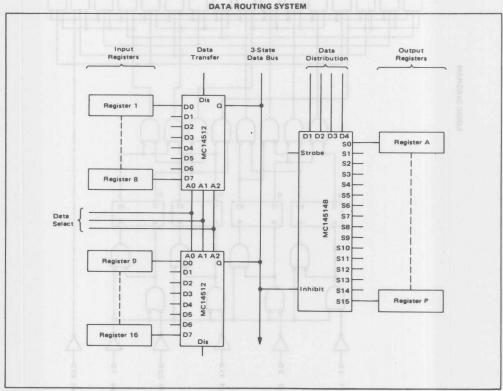
### **COMPLEX DATA ROUTING**

Two MC14512 eight-channel data selectors are used here with the MC14514B four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514B four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.





# MOTOROLA

## MC14516B

### BINARY UP/DOWN COUNTER

The MC14516B synchronous up/down binary counter is constructed with MOS P-channel and N-channel enhancement mode deivces in a monolithic structure.

This counter can be preset by applying the desired value, in binary, to the Preset inputs (P0, P1, P2, P3) and then bringing the Preset Enable (PE) high. The direction of counting is controlled by applying a high (for up counting) or a low (for down counting) to the UP/DOWN input. The state of the counter changes on the positive transition of the clock input.

Cascading can be accomplished by connecting the Carry Out to the Carry In of the next stage while clocking each counter in parallel. The outputs (Q0, Q1, Q2, Q3) can be reset to a low state by applying a high to the reset (R) pin.

This CMOS counter finds primary use in up/down and difference counting. Other applications include: (1) Frequency synthesizer applications where low power dissipation and/or high noise immunity is desired, (2) Analog-to-digital and digital-to-analog conversions, and (3) Magnitude and sign generation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design Count Occurs on Positive Going Edge of Clock
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky Load Over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter ASS D	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin-lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

### TRUTH TABLE

Carry In	Up/Down	Preset Enable	Reset	Clock	Action	
1	×	0	0	х	No Count	
0	1 0		0		Count Up	
0	0	0	0		Count Down	
X or I	X	0 15	0	×	Preset	
X	×	×	1	X	Reset	

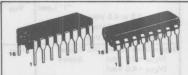
X = Don't Care

Note: When counting up, the Carry Out signal is normally high and is low only when Q0 through Q3 are high and Carry In is low. When counting down, Carry Out is low only when Q0 through Q3 and Carry In are low.

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

BINARY UP/DOWN COUNTER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

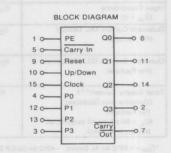
### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C

MC14XXXBCP (Plastic Package)

MC14XXXBCL (Ceramic Package)



 $V_{DD} = Pin 16$  $V_{SS} = Pin 8$ 

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

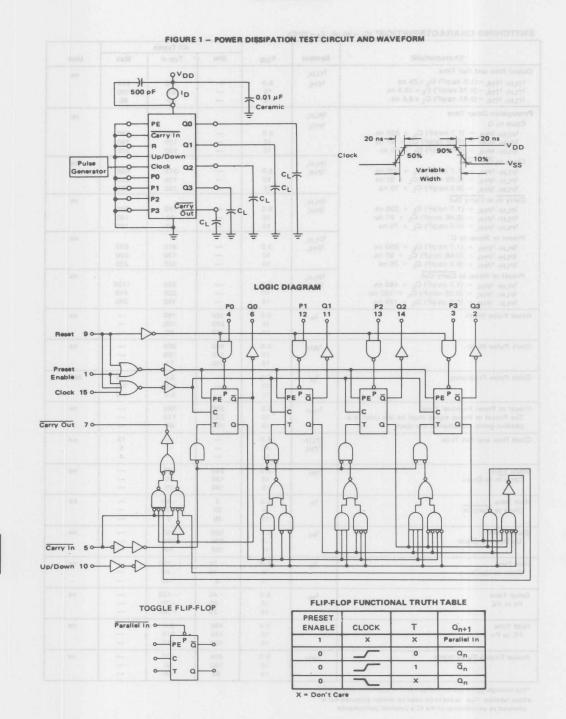
		VDD	Tic	w*		25°C		Thigh*		
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0		10		0.05	-	0	0.05		0.05	-
PERMIT TO PRIMARY	0 10 4 19	15	_	0.05	TYME	0	0.05	RABIS	0.05	
"1" Level	VOH	5.0	4.95	ni 1-1n	4.95	5.0	ou-not	4.95	105200	Vdc
Vin = 0 or VDD	· Un	10	9.95	AD-III	9.95	10	authorite	9.95	L CLOP	A SHIW
48C/10 5 F/F/ / CO 17 48C/2 F/F/	Party Company	15	14.95	II. ISHWAZIIII	14.95	15	anna an a	14.95	mala-sad	200
Input Voltage "0" Level	VIL	1 10	11100	others both	11100	- io	Of the root	14.00	100000000	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	-IL	5.0	11150 EU 25	1.5	0000 010	2.25	1.5	100	1.5	Vac
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	AUT T	10		3.0	11101-5-101	4.50	3.0	10 share	3.0	D100 000
		15	00201	4.0	Day of S	6.75	4.0	100 - 100 - 1	4.0	day.
(V <sub>O</sub> = 13.5 or 1.5 Vdc) "1" Level	V/ :	15	71-10	4.0	O Tara	0.75	4.0	10-11	4.0	1120
(VO = 0.5 or 4.5 Vdc)	VIH		CHIDNES	BAULSO.	001 00	COUNTRY	IBBINDO	0710 10 4		19865
		5.0	3.5	-	3.5	2.75		3.5	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)	2000 H	10	7.0	TUR- OU	7.0	5.50	nelleline	7.0	o belon	peu
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	1190	15	11.0	n Hein	11.0	8.25	Bh-a o	11.0	anæo n	(718.2
Output Drive Current (AL Device)	ІОН	1 .	HAIDGE	to entre	WCI S 0	10361 90	man (e	1,510		mAdc
(V <sub>OH</sub> = 2.5 Vdc) Source	1	5.0	-3.0	-	-2.4	-4.2	-	-1.7	021-011	de uisau
(V <sub>OH</sub> = 4.6 Vdc)	Circles (Applicated)	5.0	-0.64	ma_me	-0.51	-0.88	ng arbni	-0.36	200	Strift.
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	AUTOMAS A	-1.3	-2.25	oni-sno	-0.9	anit b	SHIMMO
(VOH = 13.5 Vdc)	ABBD	15	-4.2	nmi_68)(	-3.4	-8.8	SQIEUD!	-2.4	0.7007187	MODES
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	o Dorn	0.51	0.88		0.36	14 7(2)	mAdo
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.25	ASST LIBE	0.9	HIPDIN.	(\$4) tamp
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	DOM: UA	2.4	storel to	OC B
Output Drive Current (CL/CP Device)	IOH				-5.50	155 Aug - 1.1	in P	and Channel	had blee	mAdc
(VOH = 2.5 Vdc) Source	On	5.0	-2.5	-	-2.1	-4.2	0.0	-1.7	and a dead	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	_	-0.44	-0.88	में चुड़ों इस	-0.36	a yllamn	HIT III
(VOH = 9.5 Vdc)		10	-1.3	stocel re-	-1.1	-2.25	noise C	-0.9	only 2 of	10
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	_	-3.0	-8.8	-	-2.4	1540 0	
(VOL = 0.4 Vdc) Sink	la.	5.0	0.52	_	0.44	0.88	_	0.36	0.00 114 10	mAdc
(V <sub>OL</sub> = 0.5 Vdc)	IOL	10	1.3		1.1	2.25	7 <u>-</u>	0.9	I of alp	MAGC
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6		3.0	8.8	enden3	2.4	AND DELLA	10 B
			-		-			-	-	-
Input Current (AL Device)	lin	15	WO'T WOL	± 0.1	ibite. 13	±0.00001	±0.1	-	± 1.0	μAdc
nput Current (CL/CP Device)	lin	15	-	± 0.3	01-01	±0.00001	± 0.3	9457 DE	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	Cin	-	-	-	tes?	5.0	7.5	ovi ten	HITAR	pF
Quiescent Current (AL Device)	IDD	5.0	- 44	5.0	-	0.005	5.0	-	150	μAdc
(Per Package)	.00	10	0.01	10	_	0.010	10	-	300	
ti vine 5		15	11.01 4 5	20	-	0.015	20	000110	600	12
Quiescent Current (CL/CP Device)	IDD	5.0	197 198	20		0.005	20	0.000 000	150	μAdc
(Per Package)	יטטי	10	710	40	plot succ	0.003	40	11927 See	300	μAdc
ii oi i sprager		15		80		0.015	80		600	100
Total Supply Current**†	l-		- 61	00	-				600	1
	IT	5.0	921+ 6		T = (0	.58 μA/kHz	IT + IDD	greet area		μAdc
(Dynamic plus Quiescent,			71			.2 . µA/kHz)				1.5
Per Package)		15			T = (1	.7: μA/kHz)	1+100			13-
(C <sub>L</sub> = 50 pF on all outputs, all buffers switching)			money Agra-							THE DRIVE

\*T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device. PIN ASSIGNMENT #Data labelled "Typ" is not to be used for design purposes but is 1 PE VDD 16 intended as an indication of the IC's potential performance. 2 - 03 C 15 \*\*The formulas given are for the typical characteristics only at 25°C. 3 P3 02 - 14 †To calculate total supply current at loads other than 50 pF: 4 PO P2 13  $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 5 Carry In P1 12 01 - 11 6 00 where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.001.7 Carry Out U/D 10 8 - VSS R - 9

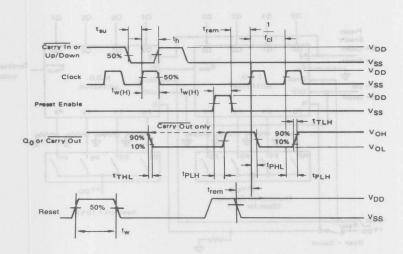
				All Types		
Characteristic	Symbol	V <sub>DD</sub>	Min	Тур #	Max	Unit
Output Rise and Fall Time	tTLH,		Links in	eavo		ns
true true = (1.5 ns/nF) Cu + 25 ns	†THL	5.0		100	200	115
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns	THE	10	_	50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		15	-	40	80	
Propagation Delay Time	tPLH,	4				ns
Clock to Q	tPHL			100 HA		
tpLH, tpHL = (1.7 ns/pF) CL + 230 ns	1112	5.0	-	315	630	
$t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$		10	_	130	260	
$t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$		15	_	100	200	
Clock to Carry Out	tPLH,					ns
tpLH, tpHL = (1.7 ns/pF) CL + 230 ns	tPHL	5.0	-	315	630	20.10/05/22
$tp_{LH}, tp_{HL} = (0.66 \text{ ns/pr}) C_L + 97 \text{ ns}$		10		130	260	
$t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$		15	9	100	200	
Carry In to Carry Out	tPLH,			1000		ns
$t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_{L} + 230 \text{ ns}$	<sup>t</sup> PHL	5.0	P. 19	180	360	
$t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$		10	1 1 Table 12	80 60	160	
$t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	-	15	1 1	60	120	
Preset or Reset to Q	tPLH,	5.0		315	630	ns
tplH, tpHL = (1.7 ns/pF) C <sub>L</sub> + 230 ns	<sup>t</sup> PHL	5.0		130	630 360	
tpLH, tpHL = (0.66 ns/pF) C <sub>L</sub> + 97 ns tpLH, tpHL = (0.5 ns/pF) C <sub>L</sub> + 75 ns		15	_	100	200	
Preset or Reset to Carry Out	tour			1		ns
tpLH, tpHL = (1.7 ns/pF) C <sub>L</sub> + 465 ns	tPLH,	5.0		550	1100	115
tpLH, tpHL = (0.66 ns/pF) C <sub>L</sub> + 192 ns	PHL	10	_	225	450	
tpLH, tpHL = (0.5 ns/pF) C <sub>L</sub> + 125 ns	100 330	15		150	300	
Reset Pulse Width	t <sub>w</sub>	5.0	380	190	_	ns
Neset i dise viidii	·w	10	200	100	_	
		15	160	80	7	0 - small
Clock Pulse Width	twH	5.0	350	200	_	ns
Olock Fallos Triatii	-VVH	10	170	100		I Eliza
	7	15	140	75		
Clock Pulse Frequency	fcl	5.0		3.0	1.5	MHz
	1	10	p-8-	6.0	3.0	
	Ludge 4 &	15	45 3 TO -	8.0	4.0	100
Preset or Reset Removal Time	trem	5.0	650	325	_	ns
The Preset or Reset signal must be low prior to a		10	230	115	_	
positive-going transition of the clock.		15	180	90		
Clock Rise and Fall Time	tTLH,	5.0	-	45	15	μS
	<sup>†</sup> THL	10		I K D.	5	
		15			4	
Setup Time	t <sub>su</sub>	5.0	260	130	-	ns
Carry In to Clock		10	120	60	-	
		15	100	50		
Hold Time	th	5.0	0	- 60	-	ns
Clock to Carry In		10	20	-20	and the second	
		15	20	0		
Setup Time	tsu	5.0	500	250	-	ns
Up/Down to Clock		10 15	200 150	100 75	<- Page 1	- 1 TO
			-		4 -4	
Hold Time	th	5.0	- 70	- 160	( ) ( )-	ns
Clock to Up/Down		10 15	-10 0	-60 -40		
			-			
Setup Time	tsu	5.0	- 40	- 120	TO THE	ns
Pn to PE	F 1742 3	10 15	-30 -25	- 70 - 50		Treat US
W. 14 7000	Thean 1		-		Control of the	
Hold Time PE to Pn	th	5.0 10	480 420	240	1.1000	ns
PE to Ph	7	15	420	210		100
Property Frankla Dudge Wildela			-			
Preset Enable Pulse Width	twH	5.0 10	100	100	_	ns
	1 10	10	100	00		

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



### FIGURE 2 - SWITCHING TIME WAVEFORMS



### PIN DESCRIPTIONS

### INPUTS

P0, P1, P2, P3, Preset Inputs (Pins 4, 12, 13, 3) — Data on these inputs is loaded into the counter when PE is taken high.

Carry In, (PIn 5) — This active-low input is used when cascading stages. Carry In is usually connected to Carry Out of the previous stage. While high, Clock is inhibited.

Clock, (Pin 15) — Binary data is incremented or decremented, depending on the direction of count, on the positive transition of this input.

### OUTPUTS

Q0, Q1, Q2, Q3, Binary outputs (Pins 6, 11, 14, 2)— Binary data is present on these outputs with Q0 corresponding to the least significant bit.

Carry Out, (PIn 7) — Used when cascading stages, Carry Out is usually connected to Carry In of the next stage. This synchronous output is active low and may also be used to indicate terminal count.

### CONTROLS

PE, Preset Enable, (PIn 1) — Asynchronously loads data on the Preset Inputs. This pin is active high and inhibits the clock when high.

R, Reset, (Pin 9) — Asynchronously resets the Q outputs to a low state. This pin is active high and inhibits the clock when high.

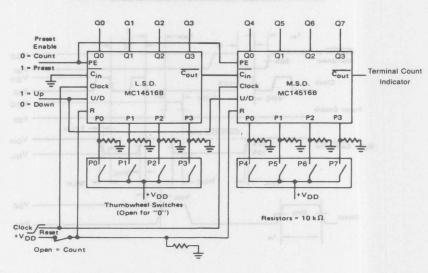
Up/Down, (Pln 10) — Controls the direction of count, high for up count, low for down count.

### SUPPLY PINS

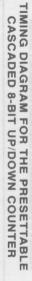
VSS, Negative Supply Voltage, (Pin 8) — This pin is usually connected to ground.

VDD, Positive Supply Voltage, (Pin 16) — This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

### FIGURE 3 - PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER



**Note:** The Least Significant Digit (L.S.D.) counts from a preset value once Preset Enable (PE) goes low. The Most Significant Digit (M.S.D.) is disabled while  $\overline{C_{in}}$  is high. When the count of the L.S.D. reaches 0 (count down mode) or reaches 15 (count up mode),  $\overline{C_{out}}$  goes low for one complete clock cycle, thus allowing the next counter to decrement/increment one count. (See Timing Diagram) The L.S.D. now counts through another cycle (15 clock pulses) and the above cycle is repeated.



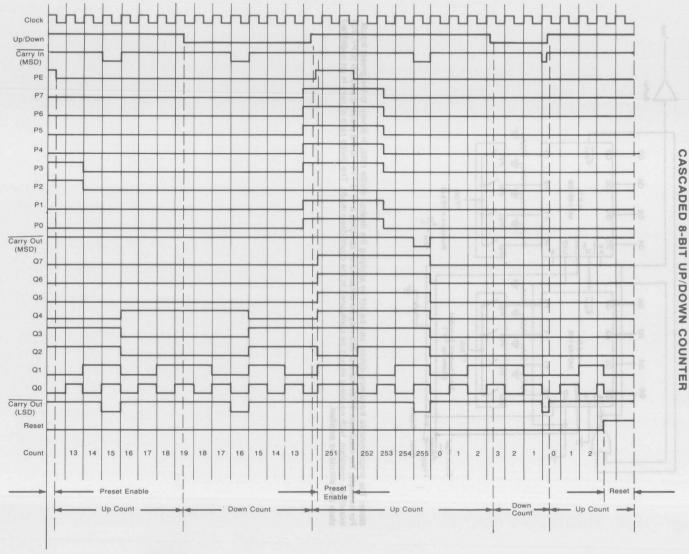
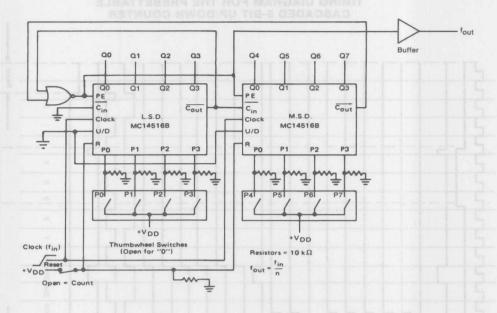


FIGURE 4 — PROGRAMMABLE CASCADED FREQUENCY DIVIDER



**Note:** The programmable frequency divider can be set by applying the desired divide ratio, in binary, to the preset inputs. For example, the maximum divide ratio of 255 may be obtained by applying a 1111 1111 to the preset inputs P0 to P7. For this divide operation, both counters should be configured in the count down mode. The divide ratio of zero is an undefined state and should be avoided.



### **DUAL 64-BIT STATIC SHIFT REGISTER**

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages referenced to VSS)

Symbol :	Parameter	Value	Unit		
VDD	DC Supply Voltage	-0.5 to +18.0	٧		
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5			
lin- lout	Input or Output Current (DC or Transient), per Pin	± 10	mA		
PD	Power Dissipation, per Package†	500	mW		
Tstg	Storage Temperature	-65 to +150	°C		
TL	Lead Temperature (8-Second Soldering)	260	°C		

\*Maximum Ratings are those values beyond which damage to the device may occur.

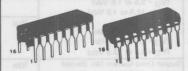
†Temperature Derating: Plastic "P" Package: -12mW°C from 65°C to 85°C

Ceramic "L" Package: -12mW°C from 100°C to 125°C

## **CMOS LSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL 64-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

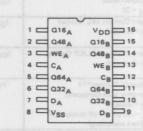
P SUFFIX PLASTIC PACKAGE CASE 648

### ORDERING INFORMATION

A Series: -55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

### PIN ASSIGNMENT



	0.7	1 10000	Ø+	8 (2 )	- ET   151	Highland 3	pedend are based t
	CLOCK	WRITE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
	0	0	×	Content of 16-Bit Displayed	Content of 32-Bit	Content of 48-Bit Displayed	Content of 64-Bit Displayed
	0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
FUNCTIONAL	1	0	×	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
TRUTH TABLE	1	1.001000	HOW X	High Impedance	High Impedance	High Impedance	High Impedance
	5	0	Date entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
	5	COOV, PL	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
	~	0	×	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-8it Displayed	Content of 64-Bit Displayed
	2	1	×	High Impedance	High Impedance	High Impedance	High Impedance
X = Don't Care							

.

### **ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

12.1 20040	Symbol	V <sub>DD</sub> Vdc	T <sub>low</sub> *		25°C			Thigh*		
Characteristic			Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	2141141	4.95	5.0	2112	4.95		Vdc
Vin = 0 or VDD	TOH	10	9.95	_	9.95	10	-0.00 miles	9.95		1
MILET RECUESER	0.000	15	14.95	telenion	14.95	15	3143-140	14.95	MCHR	111
Input Voltage "0" Level	VIL		11100		1	-	AND DO	11.00	Carrie III	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		5.0	Bh 30 ,	1.5	12/17/02/19	2.25	1.5	Hilbert	1.5	100
(VO = 9.0 or 1.0 Vdc)	The Theory	10	seafbrege endices	3.0	to we be	4.50	3.0	D 857 06	3.0	o lons
(Vo = 13.5 or 1.5 Vdc)		15	record by	4.0	Tuntiles	6.75	4.0	El TVC oriz	4.0	Hits to
"1" Level	VIH		BEYNET BUT	I Desert	J. C. (2) 15 - 17	E04578, 40	16 (16 - 64)	97 000	DOM: US	/ UCITS
(VO = 0.5 or 4.5 Vdc)		5.0	3.5	35 1H4 B	3.5	2.75	port ste	3.5	primage	Vdc
(VO = 1.0 or 9.0 Vdc)		10	7.0	s ruizmei	7.0	5.50	seed been	7.0	171-1011	Fick-810
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	To lor	15	11.0	1940	11.0	8.25	0 40 and	11.0	10-107	- spinor
Output Drive Current (AL Device)	ТОН		11.0	To beneat	11.0	0.20	DESCRIPTION	11.0	AND REAL PROPERTY.	mAdo
(VOH = 2.5 Vdc) Source	TOH	5.0	-3.0	to the same of the same	-2.4	-4.2	-	-1.7		192-y 10
(VOH = 4.6 Vdc)	8.2354	5.0	-0.64	SPACE CHARLE	-0.51	-0.88	german a	-0.36	-10-	to bos
(VOH = 9.5 Vdc)	CARRO	10	-1.6	-30	-1.3	-2.25	Dig was	-0.9	TO STATE THE	
(VOH = 13.5 Vdc)		15	-4.2		-3.4	-8.8	rugni ili	-2.4	10001 98	MID 4
(VOI = 0.4 Vdc) Sink	Lav	5.0	0.64		0.51	0.88		0.36	THE V	mAde
	IOL	10	1.6	40 arr	1.3	2.25	2020	0.36	or Line	made
(Vol = 0.5 Vdc)		15	4.2		3.4	8.8		2.4		
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	60@A-6	3.4	0.0	usiT to	2.4	vlenibet	
Output Drive Current (CL/CP Device)	ІОН				-2.1	-4.2		-1.7		mAd
(VOH = 2.5 Vdc) Source		5.0	-2.5	each blac	-0.44	-4.2	A FR B	-0.36	ou⊈ san	08 0
(V <sub>OH</sub> = 4.6 Vdc)	25	5.0	-0.52	Statement S		-2.25	and I am	-0.36	almost a	1012 F
(V <sub>OH</sub> = 9.5 Vdc)	No hard	10	-1.3	0.01200.2	-1.1	-8.8	20-1	-2.4	1	Large T
(V <sub>OH</sub> = 13.5 Vdc)	9	15	-3.6	-	-3.0		_	_	THE TAN	100
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	/ 0-1 = 4	0.36	DO - VIO	mAde
(VOL = 0.5 Vdc)		10	1.3	ent to	1.1	2.25	divoll ou	0.9	to olds	40 P
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	Toda	3.0	8.8	el Situ	2.4	Tola	102
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAdd
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	±0.3	-	±1.0	μAdd
Input Capacitance	Cin	-	-	-	-	5.0	7.5	-	1-	pF
(V <sub>in</sub> = 0)						gg V or has	description as	S. Eklolte		BEUR
Quiescent Current (AL Device)	IDD	5.0		5.0	-	0.010	5.0	-	150	μAdo
(Per Package)		10	-	10	-	0,020	10	-	300	1
at emiliaro Asso imp s		15	(3) to	20	-	0.030	20	_5000	600	09
Quiescent Current (CL/CP Device)	IDD	5.0	alle of	50	-	0.010	50	BURN N	375	⊥ μAde
(Per Package)	.00	10	-	100	1	0.020	100		750	1
		15		200	111111111111111111111111111111111111111	0.030	200	The state of the	1500	127.7
Total Supply Current**†	IT	5.0			114		1641	100	Total Control	μAde
(Dynamic plus Quiescent,		5.0 $I_T = (4.2 \ \mu A/kHz) f + I_{DD}$ 10 $I_T = (8.8 \ \mu A/kHz) f + I_{DD}$						And		
Per Package)	1911	15	- Harrison		I <sub>T</sub> = (13.7' μA/kHz) f + I <sub>DD</sub>					1.3
(C <sub>1</sub> = 50 pF on all outputs, all	8-1-19	10	-		1 (1)	, MAINIE				
buffers switching)			A/500 BH							THE PLANT
Three-State Leakage Current	ITL	15	-0.001	±0.1		±0.00001	± 0.1	T _ T	±3.0	μAdo
(AL Device)	.IL		4100	20.10	1	20.00001	10.1	2000000	13.0	µAG0
Three-State Leakage Current	l=:	15		410		+0.00004	410		475	
Times orace Fearage Chilent	ITL	10	_	±1.0	-	±0.00001	±1.0	-	± 7.5	μAdd

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated only voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

where: I  $_T$  is in  $\mu A$  (per package), C  $_L$  in pF, V = (V  $_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS\* (C1 = 50 pF, TA = 25°C)

Characteristic	Symbol	VDD	Min	Typ#	Max	Unit
Output Rise and Fall Time	tTLH.	HEN THIS				ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTHL	5.0		100	200	
$t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		10	-	50	100	
$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		15		40	80	
Propagation Delay Time	tPLH,					ns
tpLH, tpHL = (1.7 ns/pF) CL + 390 ns	tPHL	5.0		475	770	
tpLH, tpHL = (0.66 ns/pF) CL + 177 ns	-0-4	10	- 1	210	300	3-0-9
tpLH, tpHL = (0.5 ns/pF) CL + 115 ns	HOIR IN	15	-	140	215	21-0-4
Clock Pulse Width	twH	5.0	330	170	-	ns
		10	125	75		
		15	100	60	-	
Clock Pulse Frequency	fcl	5.0	9 -	3.0	1.5	MHz
		10	-0 0	6.7	4.0	3.0
	-0-9	15		8.3	5.3	The Court
Clock Pulse Rise and Fall Time	tTLH, tTHL 5.0		1111111111	-		
		10		**See Note		
		15				
Data to Clock Setup Time	t <sub>su</sub>	5.0	0	-40	0 - 0	ns
		10	10	-15	-	
yland here	agili i	15	15	0		202
Data to Clock Hold Time	th	5.0	150	75	-	ns
		10	75	25	the building arrival	S TERRITOR
		15	35	10	-	
Write Enable to Clock Setup Time	t <sub>su</sub>	5.0	400	170	-	ns
		10	200	65	-	
		15	110	50	-	
Write Enable to Clock Release Time	t <sub>rel</sub>	5.0	380	160	_	ns
		10	180	55	John -	
		15	100	40	-	

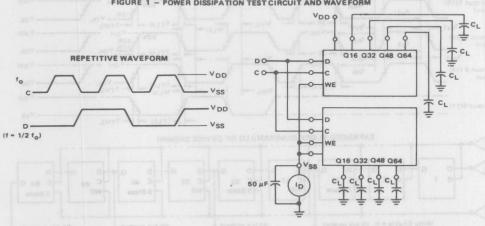
\* The formulas given are for the typical characteristics only at 25°C.

# Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\* When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and

fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



32-bit output

33-bit input

48-bit output

64-bit output

High Impedance

MC14518B



#### **DUAL UP COUNTERS**

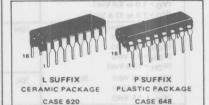
The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER (MC14518B) DUAL BINARY UP COUNTER (MC14520B)



#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

#### BLOCK DIAGRAM Clock 00-03 01 -0 4 -0 5 02 Enable 03 -0 6 Clock 00 -0 11 -0 12 01 -0 13 02 Enable 03 -0 14

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

V<sub>DD</sub> = Pin 16 V<sub>SS</sub> = Pin 8

150

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

#### TRUTH TABLE

	100000000000000000000000000000000000000		
CLOCK	ENABLE	RESET	ACTION
5	1	0	Increment Counter
0	~	0	Increment Counter
~	×	0	No Change
×	5	0	No Change
5	0	0	No Change
1	~	0	No Change
X	×	1	Q0 thru Q3 = 0

X = Don't Care

,

## MC14518B • MC14520B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tio	w		25°C		Thigh*		-
Characteristic	Symbol		Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	- 1	0.05	Vdc
Vin = VDD or 0	-	10	-	0.05	-	0	0.05	-	0.05	1
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	ULAC	4.95	-	Vdc
Vin = 0 or VDD	11	10	9.95	_	9.95	10	-	9.95	_	
		15	14.95	15 TRS	14.95	15	GOD la	14.95	FOM or	
Input Voltage "0" Level	VIL		116/13/17	Brow Year	10/10/91	33/F 107/197	DESCRIPTION	100 916	18/19/00	Vdc
(VO = 4.5 or 0.5 Vdc)		5.0	ad -800	1.5	liflo#ent	2.25	1.5	92000	1.5	prints
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	0 1	10	abentos.	3.0	non-hi	4.50	3.0	melil os	3.0	engo
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	mil-mid	4.0	it Chang	6.75	4.0	D T	4.0	pale
"1" Level	VIH			do mil	ALTERNATURE STREET	real patenti	Enable	nes mo	O aldeas	resido
(VO = 0.5 or 4.5 Vdc)		5.0	3.5	The British	3.5	2.75	nie-m	3.5	uri-	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	STY LIVE NA	7.0	5.50	-	7.0	aletalou	min
(VO = 1.5 or 13.5 Vdc)		15	11.0	Beldin Ad	11.0	8.25	110000 110	11.0		loves!
Output Drive Current (AL Device)	ІОН		1	NA MEN S			TOTAL PAR		to a collection	mAde
(V <sub>OH</sub> = 2.5 Vdc) Source	'OH	5.0	-3.0	imeg an	-2.4	-4.2	See THE	-1.7	CONTRIBUT	43.00
(VOH = 4.6 Vdc)	學	5.0	-0.64	Octyp 55	-0.51	-0.88	metal as	-0.36	neo dr	BOM
(VOH = 9.5 Vdc)	Use 1 1	10	-1.6	teglerib	-1.3	-2.25	or annua	-0.9	RIDDOS 1	998
(VOH = 13.5 Vdc)		15	-4.2	_	-3.4	-8.8	_	-2.4	mi <u>ssion</u>	rigirt
(VOL = 0.4 Vdc) Sink	lai	5.0	0.64	_	0.51	0.88	_	0.36	_	mAd
(VOL = 0.5 Vdc)	OL	10	1.6	TO N	1.3	2.25		0.9		11170
(V <sub>OL</sub> = 1.5 Vdc)	THE PARTY OF	15	4.2		3.4	8.8	200 LTD	2.4	rose2_abs	100
		13	7.2		3.4	0.0	April Street	2.4		-
Output Drive Current (CL/CP Device)	ЮН				307.5	H STORY	U.S. T. SI	1877 1017		mAde
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-2.5	lamarx.	-2.1	-4.2	107 145	-1.7	with ally	1 0
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	Swill end	-0.44	-0.88	Principle	-0.36	sole Brine	11 0
(V <sub>OH</sub> = 9.5 Vdc)		10			-1.1	-2.25	Singer T	-0.9	on denich au	10
(V <sub>OH</sub> = 13.5 Vdc)			-3.6		-3.0	-8.8	2001-017	-2.4	- n-	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	1110 to 1	0.44	0.88	O. TOW	0.36	la s <del>n</del> atta	mAde
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3	- PEGNE	1.1	2.25	BAT 384	0.9	I galled	10
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8	_	.2.4	-	
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μAdd
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	±0.3	-	±1.0	μAdd
Input Capacitance (V <sub>in</sub> = 0)	Cin	-	-	-	(Vest)	5.0	7.5	10 Table	STATE N	pF
Quiescent Current (AL Device)	lan	5.0	_0000	5.0	-	0.005	5.0	-	150	μAdo
(Per Package)	loo	10		10	_	0.010	10	opening.	300	- And
		15		20	-	0.015	20	-	600	
Outcome Comment (CL ICR Dec.)	- las	100	H HOW		-	0.005	20	1		1
Quiescent Current (CL/CP Device)	IDD	5.0	- 01	20	NA Inq	0.005	0:43750.00	1107 June	150	μAde
(Per Package)		10	1000	40	1 -	0.010	40 80	1 000 20	300	1
T-1-161 6100	- 1-		-	80	-	-			600	1
Total Supply Current**†	IT	5.0	207 4 01			).6 µA/kHz)				μAdi
(Dynamic plus Quiescent,	Marine I	10	091			.2 µA/kHz)				
Per Package)	68	15	355 3896		T = (1	.7 μA/kHz)	I + IDD			of our
(CL = 50 pF on all outputs, all			1							dual name

\*Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

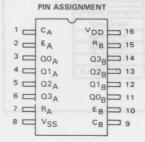
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: IT is in  $\mu$ A (per package), CL in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.002.

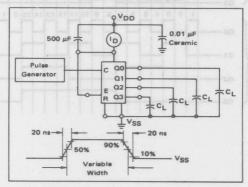
\*\*The formulas given are for the typical characteristics only at 25°C.



				All Types			
Characteristic	Symbol	VDD	Min	Typ#	Max	Unk	
Output Rise and Fall Time  **T_LH, **T_THL = (1.5 ns/pF) C_L + 25 ns  **T_LH, **T_THL = (0.75 ns/pF) C_L + 12.5 ns  **T_T_LH, **T_THL = (0.55 ns/pF) C_L + 9.5 ns	tTLH- tTHL	5.0 10 15	= 0	100 50 40	200 100 80	ns	
Propagation Delay Time Clock to Q/Enable to Q tp_H, tpHL = (1.7 ns/pF) C <sub>L</sub> + 215 ns tp_H, tpHL = (0.66 ns/pF) C <sub>L</sub> + 97 ns tp_H, tpHL = (0.5 ns/pF) C <sub>L</sub> + 75 ns	tPLH, tPHL	5.0 10 15	-000 -000 -050	280 115 80	560 230 160	ns	
Reset to Q tpHL = (1.7 ns/pF) CL + 265 ns tpHL = (0.66 ns/pF) CL + 117 ns tpHL = (0.66 ns/pF) CL + 95 ns	tpHL	5.0 10 15	1870	330 130 90	650 230 170	ns	
Clock Pulse Width	tw(H)	5.0 10 15	200 100 70	100 50 35	Ξ	ns	
Clock Pulse Frequency	fcl	5.0 10 15	-	2.5 6.0 8.0	1.5 3.0 4.0	MHa	
Clock or Enable Rise and Fall Time	THL, TLH	5.0 10 15	-	-	15 5 4	hs	
Enable Pulse Width	tWH(E)	5.0 10 15	440 200 140	220 100 70	-	ns	
Reset Pulse Width	WH(R)	5.0 10 15	280 120 90	125 55 40	=	ns	
Reset Removal Time	t <sub>rem</sub>	5.0 10 15	-5 15 20	-45 -15 -5	Ξ	ns	

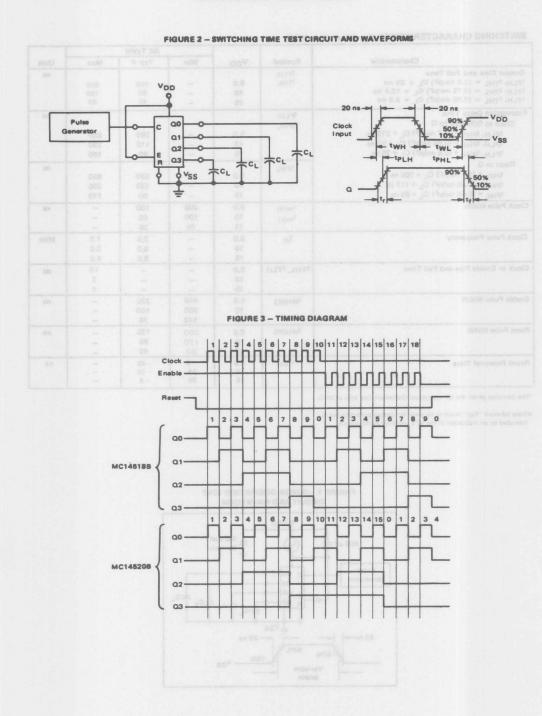
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#### FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## MC14518B•MC14520B



## MC14518B•MC14520B

FIGURE 4 - DECADE COUNTER (MC14518B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

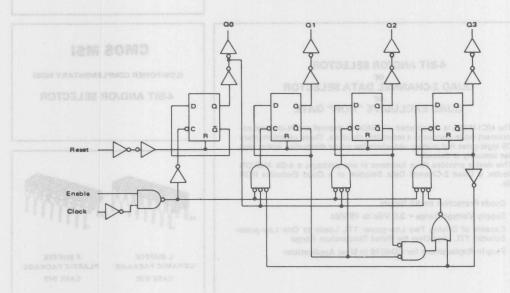
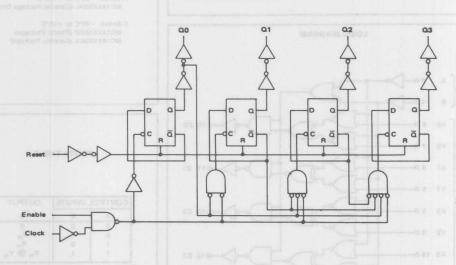


FIGURE 5 - BINARY COUNTER (MC14520B) LOGIC DIAGRAM (1/2 OF DEVICE SHOWN)





# 4-BIT AND/OR SELECTOR OF QUAD 2-CHANNEL DATA SELECTOR OF QUAD EXCLUSIVE "NOR" GATE

The MC14519B is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device provides three functions in one package; a 4-Bit AND/OR Selector, a Quad 2-Channel Data Selector, or a Quad Exclusive NOR Gate.

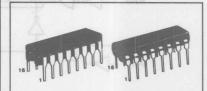
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Plug-In Replacement for CD4019 in Most Applications

# 

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

4-BIT AND/OR SELECTOR



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### TRUTH TABLE

CONTROL	OUTPUT	
A	В	Zn
0	0	0
0	1	Yn
1	0	Xn
1	1,	Xn @ Yn

Note:

Xn @ Yn meens Xn (Exclusive-NOR) Yn

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

#### PIN ASSIGNMENT 1 73 VDD 16 2 - X2 X3 15 3 - Y2 В 14 4 - X1 Z3 🗀 13 5 - Y1 Z2 12 Z1 11 6 - X0 ZO 10 7 - YO 8 = A -9 Vss

#### ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

Characteristic			VDD	Tio	w*		25°C		Thi	gh °	
		Symbol			Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	- 1	0:05	Vd
V <sub>in</sub> =V <sub>DD</sub> or 0			10	_	0.05		0	0.05	- 1	0.05	
III DD s. s	MINOS SERVICE	CHEA TILL	15	HOSTAR	0.05	1303 310	0	0.05	-	0.05	
	"1" Level	Van	5.0	4.95	-	4.95	5.0		4.95		Vd
Vin=0 or VDD	Level	VOH	10	9.95	_	9.95	10		9.95	II.	Va
			15	14.95	Out of the	14.95	15			E .	1
			15	14.95		14.95	15	-	14.95	-	-
Input Voltage	"0" Level	VIL					19				Vd
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$			5.0	-	1.5	Jud 67	2.25	1.5	- Jan. 9	1.5	1
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$			10	-	3.0	-	4.50	3.0	30500000	3.0	
$(V_0 = 13.5 \text{ or } 1.5 \text{ Vdc})$		and the second	15	-	4.0	-	6.75	4.0	-	4.0	-
	"1" Level	VIH					OV	-			Vdc
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$			5.0	3.5	di sle	3.5	2.75	4	3.5	-	
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$		CAN L	10	7.0	-	7.0	5.50	-	7.0	-	
(Vo = 1.5 or 13.5 Vdc)		anak.	15	11.0	-	11.0	8.25	14	11.0	-	
Output Drive Current (AL I	Device)	ІОН			A SE			111			mAd
	Source	OIT	5.0	-3.0	-7	-2.4	-4.2		-1.7	_	
(V <sub>OH</sub> = 4.6 Vdc)			5.0	-0.64	- 195	-0.51	-0.88		-0.36	_	
(VOH = 9.5 Vdc)			10	-1.6		-1.3	-2.25	-2	-0.9		
(V <sub>OH</sub> = 13.5 Vdc)			15	-4.2	少年	-3.4	-8.8	1	-2.4		
	0:1				-	-	-		-		1
OL	Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAd
(V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)			10	1.6	7 700	1.3	2.25	-	0.9		1
			15	4.2	-	3.4	8.8	-	2.4	-	1
Output Drive Current (CL/	CP Device)	ІОН				THE BUTTON					mAd
(V <sub>OH</sub> = 2.5 Vdc)	Source		5.0	-2.5	- 1	-2.1	-4.2	-	-1.7	-	
(VOH = 4.6 Vdc)			5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(VOH = 9.5 Vdc)	2015	<b>经济水平</b>	10	-1.3	BOAT DE	-1.1	-2.25	14 -	-0.9	-	
(VOH = 13.5 Vdc)			15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.52	_	0.44	0.88	_	0.36	_	mAd
(VOL = 0.5 Vdc)		OL	10	1.3	_	1.1	2.25	_	0.9		
(VOL = 1.5 Vdc)			15	3.6	_	3.0	8.8	_	2.4		-
Input Current (AL Device)	200 m	lin	15	_	± 0.1		±0.00001	±0.1	-	± 1.0	μAd
	, 201		15		± 0.1	-					-
nput Current (CL/CP Devi	ce)	lin		-		377-	±0.00001	± 0.3		± 1.0	μAd
Input Capacitance (V <sub>in</sub> = 0)	00	Cin	_	-	10-	92	5.0	7.5			ρF
Quiescent Current (AL Dev	ice)	IDD	5.0	- stoo	5.0	775	0.005	5.0	-	150	μAd
(Per Package)	minuted	.00	10		10	1	0.010	10		300	
	and her	100 00 10	15	-	20		0.015	20		600	1
Quiescent Current (CL/CP)	Davical	IDD	5.0	_	20	2342	0.005	20		150	μΑс
(Per Package)	Device)	יטטי	10		40	I.	0.005	40	4	300	μΑσ
(i.e. rackage)	Server 34	maiod	15		80	-	0.015	80			
Total Cupalu Curanitat				-	80					600	-
Total Supply Current**†	1	IT	5.0				.2 μA/kHz				μAd
(Dynamic plus Quiescen	it,		10				2.4 μA/kHz				
Per Package) (C <sub>L</sub> = 50 pF on all outp buffers switching)	uts, all		15			I <sub>T</sub> = (3	I.6 µA/kHz	) f + IDD			

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: I  $_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V  $_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k = 0.004.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

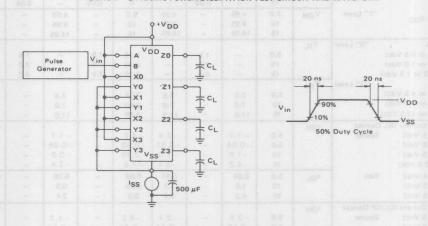
SWITCHING CHARACTERISTICS\* (C1 = 50 pF, TA = 25°C)

Characteristic	Symbol	VDD	Min	Typ#	Max	Unit
Output Rise and Fall Time t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTLH-	5.0	comtol to 5	100	200	ns
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns	656	10	-1:0053	50	100	49
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	007 - 51 (8	15	-	40	80	Yester
Propagation Delay Time	tPLH,		Noncolor De	a hard the amount	served Tempos	ns
tpLH, tpHL = (1.7 ns/pF) CL + 165 hs	tPHL	5.0	_	250	500	-
tPLH, tPHL = (0.66 ns/pF) CL + 82	Alleged water adivers	10	Mency Street	115	225	munica
tpLH, tpHL = (0.5 ns/pF) CL + 65 ns	O(19 8) O/6	15	Stxgaxa	90	165	ALIE ARE GLASS

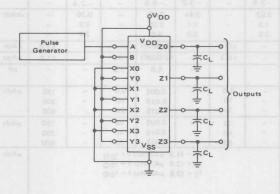
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

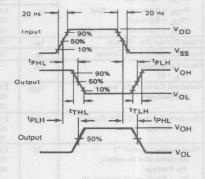
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

#### FIGURE 1 - DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



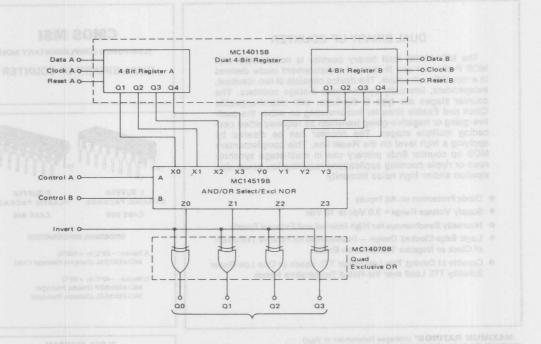
#### FIGURE 2 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





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#### DATA REGISTER SELECTION COMPARISON



CONV	/ERS	ION	TAE	LE

0	OPERATION		¥ 8	оит	FUNCTION		
Α	В	INV	0.0	Q1	02	Q3	HEREN IN VIOLENCE
0	0	0	0	0	0	0	Inhibit, all zeros
0	0	1	1	1 0	1	1	Inhibit, all ones
1	0	0	xo	X1	X2	Х3	Control A
1	0	1	Χo	X1	X2	X3	Control A and Invert
0	1	0	YO	Y1	Y2	Y3	Control B
0	1	1	Ÿ0	V1	¥2.	Ÿ3	Control B and Invert
1	1	0	X0 @ Y0	X1 @ Y1	X2 @ Y2	X3@ Y3	Exclusive NOR
1	1	1	X0 ⊕ Y0	X1⊕ Y1	X2⊕ Y2	X3⊕ Y3	Exclusive OR

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

#### MC1452UB

FOR COMPLETE DATA SEE MC14518B

#### **DUAL BINARY UP COUNTER**

The MC14520B dual binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure. The device consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. The counter can be cleared by applying a high level on the Reset line. This complementary MOS up counter finds primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

**DUAL BINARY UP COUNTER** 



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

## ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C
Ceramic "L" Package: -12mW/°C from 100°C to 125°C

#### **BLOCK DIAGRAM** 00 -0 3 01 -0 4 20 02 -0 5 Enable Q3 -0 6 Clock QO -0 11 0 12 01 100 02 -0 13 Enable 03 -0 14 150 VDD = Pin 16 VSS = Pin 8

#### TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
5	r aspitav b	0	Increment Counter
0	~	0	Increment Counter
7	X	0	No Change
×	5	0	No Change
5	0	0	No Change
1	~	0	No Change
×	х	1	Q0 thru Q3 = 0

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\rm in}$  and  $V_{\rm out}$  should be constrained to the range  $V_{\rm SS} \leqslant (V_{\rm in}$  or  $V_{\rm out}) \leqslant V_{\rm DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



## MC14521B

#### 24-STAGE FREQUENCY DIVIDER

The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to  $2^{24} = 16,777,216$ . The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- VDD' and VSS' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)
24-STAGE FREQUENCY DIVIDER



CERAMIC PACKAGE

P SUFFIX PLASTIC PACKAGE CASE 648

620

#### ORDERING INFORMATION

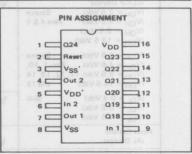
A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

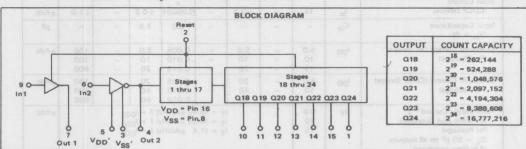
C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### MAXIMUM RATINGS\* (Voltages Referenced to Voc.)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	BV
I <sub>in</sub> . I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C





This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

#### ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

Symbol	Vdc	Min	May	Min	Typ#	May	0.01	Banu	11-14	
	A CLC	Min Ma:		141111	1 yp m	Max	Min	Max	Unit	
Voi	5.0	-	0.05	_	0	0.05	_	0.05	Vdc	
- OL	10	-	0.05	-	0	0.05	-	0.05		
	15	-	0.5	-	0	0.05	-	0.05		
Vau	5.0	4 95	0.200	4 95	5.0	RED T	4 95	_	Vdc	
HOH			-						1	
									100	
	7	1100-1130	E 808043-1	1 1.00	PH TO S	10.516	100	0.00		
VIL		prout His	Dugar E	51 1900	erson fo		PRINCIPAL PARTY	dept 1 Page	Vdc	
-		ा मिराइ		S 15:10			i tolski		D 5 28	
		in Ton		th Table			13-,10TH	1110000	119119	
	15	er tement	4.0	cu. attrie	6.75	4.0	or Vol. or	4.0	de la company	
V	4 m is	aba main	a avitant	0.600.00	180/351/0	st Thurst	ezil' 31	111081	Vdc	
, IH	5.0	3.5	- II	3.5	2.75		3.5	- In	1 4 40	
			AMPLEASY II			al and a		-	dixal	
			_			_		- 177	SZI A-GRI	
		11.0		11.0	0.20	-	11.0	1	100	
Іон									mAdo	
10 11			VC-1083			26(7 %)		A COUNTY OF	0.13	
	5.0	-0.25	ACTO N	-0.2	-0.36	O Total	-0.14	of bea	DR 4	
	10	-0.62	-	-0.5	-0.9	-	0.35	Поп	Ext	
	15	-1.8	-	-1.5	-3.5	-	-1.1	-		
	5.0	-30	_	-24	-42	1 119 1	-17	10000	mAdo	
			libert !			Beaus		those to	IIIAuc	
								de world	COT	
1 13			Mar Paris						1000	
	15	-4.2		-3.4	-0.0				NY	
IOL	5.0	0.64	-	0.51	0.88	0.5-1		15-Y 1980	mAdd	
-	10	1.6	O see all	1.3	2.25	es Foel	0.9	Tro-ulda	de Can	
1 111	15	4.2	of Tour	3.4	8.8	SALT HOLE	2.4	T-only	198	
								1		
-							100	1	mAdo	
'ОН	E 0	1.0		0.0	17		0.6		IIIAUC	
							- 0000000000000000000000000000000000000			
						to FF step		PATTAR	MULH	
1 1 1		10000		1		5510.00				
1 1 1	15	-1.4		-1.2	-3.5	_	-1.0	-		
	5.0	-2.5	-	-2.1	-4.2	_	-1.7	-Address	mAdo	
1 11	5.0	-0.52	10-5-1	-0.44	-0.88	10-00	-0.36	pro-January	logof a	
1 1 1	10	-1.3	-	-1.1	-2.25	-	-0.9	- T in	and I	
	15	-3.6	-	-3.0	-8.8		-2.4	-		
la.	State State	0.52		0.44	0.88	THE THE	0.36	1_	mAdo	
'OL			88 - 1	1				Semol se	IIIAGC	
	10	3.0		3.0	0.0		2.7		1	
		so wan e	oweb en	of season	* ± 00		samer of	delle sin si	POPE .	
lin	15	47.88	± 0.1	1000-014	0.00001	±0.1	P-anna	± 1.0	μAdc	
- property		m.ser.or	arear a	100	+	1	2 3011211	1	1	
1	15		+03	_		±03	_	±1.0	иAdc	
	120	Physicana.	+0.5							
Cin	-	-	-	-	5.0	7.5	-	-	pF	
					6		The last			
lon	5.0	_	5.0	_	0.005	5.0	_	150	μAdc	
00				_			-		1	
-			2000	_			_	600	1	
1	-						100			
'DD		101					08.		μAdc	
2000		1.0000		1			1-4	0.000	1	
1		7	80	1 -				1 000	-	
IT	5.0								μAdc	
	10			I- = (0	85 μA/kH	e) f + lo			1	
1 1		1 4 5		1 - 10.	OU HAIRI	.,	U			
6 6	15	0 1		$I_{T} = (1.$	4 μA/kH	z) f + 10	D			
	VIH  IOH  IOL  IOL  Ioh  Ioch   10	To   To   To   To   To   To   To   To	10	Voh	Voh   10   -     0.05   -   0   0   0.5       Voh   5.0   4.95   -     4.95   5.0   10   9.95   -     9.95   10   14.95   15     Vil   5.0   -     1.5   -     2.25   15   15     Vih   5.0   3.5   -     3.0   -     4.50   15   15      Vih   5.0   3.5   -     3.5   2.75   7.0   5.50   11.0   -   11.0   8.25   10   7.0   -   7.0   5.50   15   11.0   -   11.0   8.25   10   - 0.62   -   - 0.5   -   - 0.9   15   -   18   -   -   -   1.5   -   3.5     10   -   1.6   -   -   1.3   -   2.25   15   -   4.2   -   -   3.4   8.8	Voh   10   -     0.05   -     0   0.05   0.05       Voh   10   9.95   -     9.95   10   -       15   14.95   -     14.95   15   -     Vil	Voh	10		

 $<sup>^{\</sup>circ}$ Tlow = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: I  $_T$  is in  $\mu A$  (per package), C  $_L$  in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.003.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

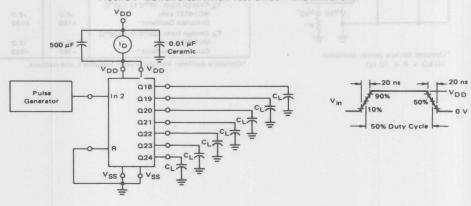
SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise and Fall Time (Counter Outputs)	tPLH,		TOUR S	Plage		ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tPHL .	5.0	= 15	100	200	-
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns		10	2 181	50	100	with
$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	10,	15	510	40	80	SEASON OF
Propagation Delay Time	tPLH.				The state of	Ms
Clock to Q18	TPHL			3		
tPHL, tPLH = (1.7 ns/pF) CL + 4415 ns	1000	5.0		4.5	9.0	
tpHL, tpLH = (0.66 ns/pF) CL + 1667 ns		10		1.7	3.5	
tpHL, tpLH = (0.5 ns/pF) CL + 1275 ns		15	I	1.3	2.7	
Clock to Q24						1
tpHL, tpLH = (1.7 ns/pF) CL + 5915 ns		5.0	The land of	6.0	12	
tpHL, tpLH = (0.66 ns/pF) CL + 2167 ns		10		2.2	4.5	1 7 6 2 4
tPHL, tPHL = (0.5 ns/pF) CL + 1675 ns		15	-	1.7	3.5	
Propagation Delay Time	tPHL			13-1-1		ns
Reset to Q <sub>n</sub>						
tpHL = (1.7 ns/pF) CL + 1215 ns		5.0	-	1300	2600	
tpHL = (0.66 ns/pF) CL + 467 ns		10	-	500	1000	
tpHL = (0.5 ns/pF) CL + 350 ns		15	_	375	750	
Clock Pulse Width	tWH(cl)	5.0	385	140	-	ns
	-68-110	10	150	55	-	
		15	120	40	-	
Clock Pulse Frequency	fcl	5.0	-	3.5	2.0	MHz
		10	-	9.0	5.0	
		15	TORES RET	12	6.5	HRL/DIT
Clock Rise and Fall Time	tTLH,	5.0	-	-	15	μs
	THL	10		-	5	
		15	- 004	-	4	
Reset Pulse Width	tWH(R)	5.0	1400	700	12	ns
	inabiliarii	10	600	300	- 1	
		15	450	225	-	
Reset Removal Time	trem	5.0	30	- 200	-	ns
	Tom	10	0	- 160	-	
	- 55	15	-40	-110	_	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



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## MC14521B

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

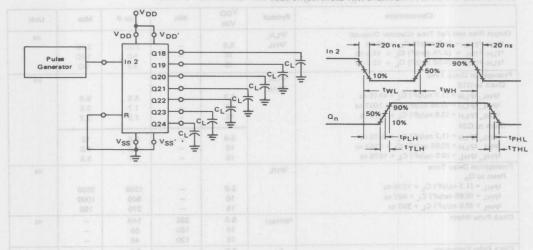


FIGURE 3 - CRYSTAL OSCILLATOR CIRCUIT

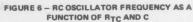
· VDD HOH ₹R. ONDOD NDD 18 M Out 1 -0 In 1 Out 2 -0-018 0 019 0 020 0 021-0 022-0 023 0 市cs 市cr ovss ovss' ₹R.

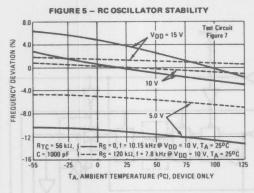
\*Optional for low power operation. 10 k $\Omega \le R \le 70 \text{ k}\Omega$ 

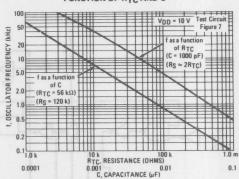
FIGURE 4 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

OGGILLATORY	,,,,,		different contracts
CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics	-	controlly make 8	esta Fil
Resonant Frequency	500	50	kHz
Equivalent Resistance, RS	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R <sub>o</sub> max	47	750	kΩ
CT	82	82	pF
CS	20	20	pF
Frequency Stability Frequency Change as a Function of V <sub>DD</sub> (T <sub>A</sub> = 25°C)	eight oill apt va	nevig salum	rent :
V <sub>DD</sub> Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V <sub>DD</sub> Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (V <sub>DD</sub> = 10 V) T <sub>A</sub> Change from -55°C to +25°C			
MC14521 only	-4.0	-2.0	ppm
Complete Oscillator®	+100	+120	ppm
TA Change from +25°C to +125°C			
MC14521 only	-2.0	-2.0	ppm
Complete Oscillator*	-160	-560	ppm

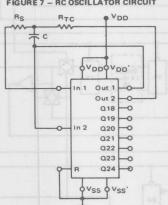
<sup>\*</sup>Complete oscillator includes crystal, capacitors, and resistors.



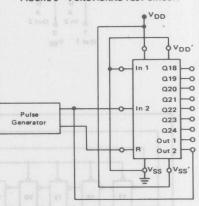




## FIGURE 7 - RC OSCILLATOR CIRCUIT



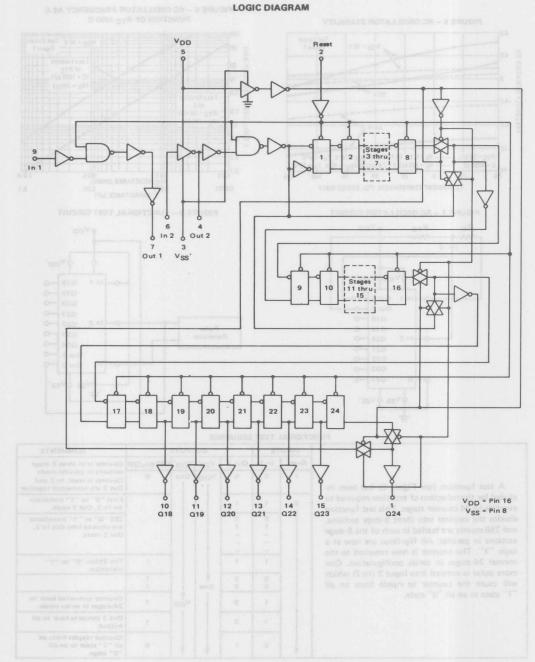




#### **FUNCTIONAL TEST SEQUENCE** INPUTS

A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.

	INPU	TS		OU	TPUTS	5	COMMENTS				
	Reset	In 2	Out 2	VSS'	VDD'	Q18 thru Q24	Counter is in three 8-stage				
	1	0	0	VDD	Gnd	0	sections in parallel mode Counter is reset. In 2 and Out 2 are connected together				
	0	1 8	1		131	O Dr	First "0" to "1" transition on In 2, Out 2 node.				
	5.65	0 1 - -	0 1 - -	92		aro	255 "0" to "1" transitions are clocked into this In 2, Out 2 node.				
		1	1			1	The 255th "0" to "1" transition.				
I		0	0	Gnd		1 1					
I		1	0		VDD	1	Counter converted back to 24-stages in series mode.				
I		1	0			1	Out 2 converts back to an output.				
	-	0	1			0	Counter ripples from an all "1" state to an all "0" stage.				



# PRESETTABLE 4-BIT DOWN COUNTERS

The MC14522B BCD counter and the MC14526B binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure.

These devices are presettable, cascadable, synchronous down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Inhibit input allows disabling of the pulse counting function. Inhibit may also be used as a negative edge clock.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Design Incremented on Positive Transition of Clock or Negative Transition of Inhibit
- Asynchronous Preset Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin. lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

#### **FUNCTION TABLE**

		Inputs		FKY IS T	Output	Resulting
Clock	Reset	Inhibit	Preset Enable	Cascade Feedback	"0"	Function
×	н	X	L	L	L	Asynchronous reset*
×	Н	X	Н	L	н	Asynchronous reset
X	H	X	X	Н	H	Asynchronous reset
Х	L	х	Н	X	L	Asynchronous preset
/	L	_ н	L	×	L	Decrement inhibited
L	L	_	L	X	L	Decrement inhibited
_	L	L_	L	L	L	No change** (inactive edge)
Н	L		L	L	L	No change** (inactive edge)
	L	L	L	L	L	Decrement**
Н	L		L	L	L	Decrement**

X = Don't Care

#### Votes:

- \* Output "0" is low when reset goes high only if PE and CF are low.
- \*\* Output "0" is high when reset is low, only if CF is high and count is 0000.

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

#### PRESETTABLE 4-BIT DOWN COUNTERS

BCD - MC14522B Binary - MC14526B



L SUFFIX
CERAMIC PACKAGE
CASE 620

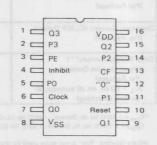
P SUFFIX PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tio	w°		25°C		Thi	gh*	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0		10	-	0.05	-	0	0.05		0.05	
		15	-	0.05	-	0	0.05		0.05	
"1" Level	VOH	5.0	4.95	100.00	4.95	5.0	-	4.95	-	Vdc
Vin = 0 or VDD	-01	10	9.95	in range	9.95	10	- T	9.95	STOR OF	1
SHORT WAS INVALUED IN	71	15	14.95	10-00	14.95	15	0 12307	14.95	unit-son	010
Input Voltage "0" Level	VIL					instruction.	sidalilani	n a ni o	enfusio Al	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	11	5.0	5 P41500	1.5	it/index	2.25	1.5	OS600	1.5	- vac
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	Con-Mar	3.0	and -unit	4.50	3.0	not-ord	3.0	000
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	ot i-sitor	4.0	- n	6.75	4.0	nei- si	4.0	icit
"1" Level	VIH	20,110	ung a grup	4.0	singuistic	0.70	CONTRACT	man a	ton A to	1996
(Vo = 0.5 or 4.5 Vdc)	- 111	5.0	3.5	number no.	3.5	2.75	ut Stile	3.5	14-ws-sh	Vdc
(Vo = 1.0 or 9.0 Vdc)		10	7.0	no Lorus	7.0	5.50	Seri No. 1	7.0	mundle t	1
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	of the state of th	11.0	8.25	8-19-11SC	11.0	sonia ad	ata
Output Drive Current (AL Device)		10	11.0	DOM:	11.0	0.20	C 355 V 15	11.0	105 5500	mAdc
	ІОН	5.01	-3.0	District to	-2.4	-4.2		-1.7	necizen	MAGC
(V <sub>OH</sub> = 2.5 Vdc) Source	Har	5.0	-0.64	Arrah Burgar	-0.51	-4.2	ig west	-0.36	220lls	ula
(V <sub>OH</sub> = 4.6 Vdc)	1		-1.6	114 - 118	-1.3	-2.25		-0.9	white	neni
(V <sub>OH</sub> = 9.5 Vdc)		10	-4.2	_	-3.4	-2.25	_	-2.4		
(V <sub>OH</sub> = 13.5 Vdc)		15	-	-	1		D 19 1000	- Historian Physics Ph	-	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdo
(VOL = 0.5 Vdc)		10	1.6	OF TIO	1.3	2.25	150m br	0.9	ud tigo.	10
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	емпари	2.4	ion <del>o</del> nei	
Output Drive Current (CL/CP Device)	ІОН									mAdo
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	Parento In	-1.7	Partition for	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	PO 10 0	-0.44	-0.88	od twi	-0.36	nti-inal	0
(V <sub>OH</sub> = 9.5 Vdc)	11	10	-1.3	RET SIL	-1.1	-2.25	5 YEVO	-0.9	yothoris	
(V <sub>OH</sub> = 13.5 Vdc)		15	j - 3.6	-	-3.0	-8.8		-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	a describ	0.36	TATI 00	mAdo
(VOL = 0.5 Vdc)	1	10	1.3	-	1.1	2.25	- 100	0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8	atamas.	2.4	-	loge
Input Current (AL Device)	lin	15	18(4) 80	±0.1	-	±0.00001	±0.1	вршкой-	±1.0	μAdc
Input Current (CL/CP Device)	lin	15	7 NOV	± 0.3	-	±0.00001	±0.3	altonia anti-	±1.0	₩Adc
Input Capacitance	Cin		1007		+	5.0			- 1.0	pF
(V <sub>in</sub> = 0)	Cin		- 87.9	-	10° Tag (	5.0	7.5	SWOTON: B	12 Millioge	pr
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdc
(Per Package)	00	10	000 0	10	-	0.010	10	heleget m	300	1 117
		15	- 005	20	-	0.015	20	NAME OF THE OWNER, OF	600	1
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	10 0-0	0.005	20	-	150	μAdo
(Per Package)	.00	10		40	- THE PARTY OF	0.010	40		300	MAGC
विद्याहर्ण । विद्याहर		15	2787 6	80	9 D-MI	0.015	80		600	
Total Supply Current**†	lт	5.0		00	1 11				000	μAdc
(Dynamic plus Quiescent,	'1	10	The property of the party of th							μAdc
Per Package)		15				5.1 μA/kHz				
(C <sub>1</sub> = 50 pF on all outputs, all		15			.1 - 4:	μ <u>Μ/ΚΠ</u> 2	יייי יטנ	,		
buffers switching)	1 1		intstunos							

 $<sup>^*</sup>T_{low} = -55^\circ\text{C}$  for AL Device,  $-40^\circ\text{C}$  for CL/CP Device.  $T_{high} = +125^\circ\text{C}$  for AL Device,  $+85^\circ\text{C}$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance. where: I

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 pF) + (C_L - 50) Vfk$ 

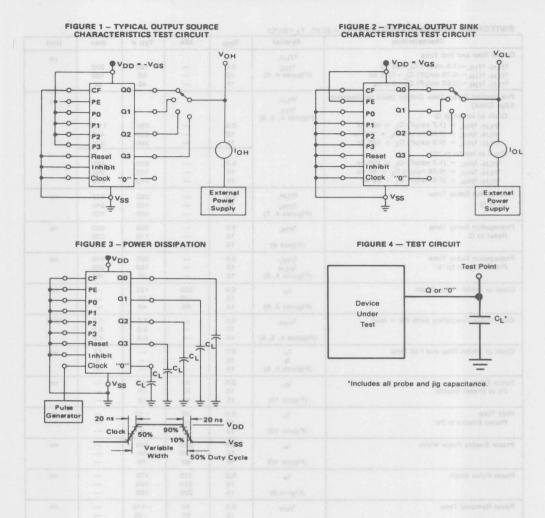
where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.001.

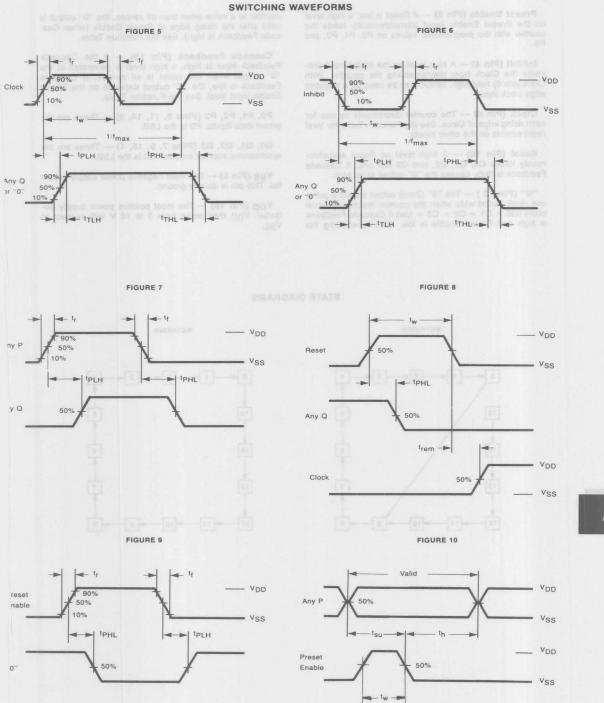
SWITCHING CHARACTERISTICS\* (CI = 50 pF. TA = 25°C

Characteristic	Symbol	VDD	Min	Тур #	Max	Unit
Output Rise and Fall Time	tTLH,	MON				ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	t <sub>THL</sub>	5.0	-	100	200	7 - 197
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns	(Figures 4, 5)	10	_	50	100	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		15	-	40	80	
Propagation Delay Time (Inhibit Used as Negative- Edge Clock)	tPLH,		-d 0	-0 E	34-	ns
Clock or Inhibit to Q	(Figures 4, 5, 6)		Q Y		0.0	
tpLH, tpHL = (1.7 ns/pF) CL + 465 ns		5.0	-	550	1100	-Dorest
tpLH, tpHL = (0.66 ns/pF) CL + 197 ns		10	-	225	450	-0-9
tpLH, tpHL = (0.5 ns/pF) C <sub>L</sub> + 135 ns	-4	15	-	160	320	-0-4-1
Clock or Inhibit to "0"				-0		-C
tpLH, tpHL = (1.7 ns/pF) CL + 155 ns		5.0	-	240	480	-Owner,
$t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$		10	-	130	260	
tpLH, tpHL = (0.5 ns/pF) C <sub>L</sub> + 65 ns		15	_	100	200	
Propagation Delay Time	tPLH,	5.0		260	520	ns
Pn to Q	<sup>t</sup> PHL	10	-	120	240	
	(Figures 4, 7)	15	-	100	200	
Propagation Delay Time	tPHL	5.0	-	250	500	ns
Reset to Q		10	_	110	220	
1000年10 TRET 本 25000円	(Figure 8)	15	NOTE VOIS	80	160	
Propagation Delay Time	tPHL,	5.0	-	220	440	ns
Preset Enable to "0"	t <sub>PLH</sub>	10	-	100	200	May 18h
9	(Figures 4, 9)	15		80	16.0	-0-3
Clock or Inhibit Pulse Width	t <sub>w</sub>	5.0	250	125		ns
Davies		10	100	50	D	
1	(Figures 5, 6)	15	80	40	-	
Clock Pulse Frequency (with PE = low)	fmax	5.0	-	2.0	1.5	MHz
		10		5.0	3.0	-0-8
	(Figures 4, 5, 6)	15	-	6.6	4.0	-
Clock or Inhibit Rise and Fall Time	t <sub>r</sub> ,	5.0	17	_	15	μS
Annales Service Servic	tf	10	1	- 1	5	
THE STATE OF THE S	(Figures 5, 6)	15	- 392	- T	4	TY
Setup Time	t <sub>su</sub>	5.0	90	40	avė -	ns
Pn to Preset Enable		10	50	15	0-	
	(Figure 10)	15	40	10	幸一 7	
Hold Time	th	5.0	30	- 15	- m 02	ns
Preset Enable to Pn	(m)	10	30	-5		
	(Figure 10)	15	30	0	0.0403 -	
Preset Enable Pulse Width	t <sub>w</sub>	5.0	250	125	_	ns
	(5)	10	100	50	_	
	(Figure 10)	15	80	40		
Reset Pulse Width	t <sub>w</sub>	5.0	350	175	-	ns
	(Figure 9)	10	250	125	_	
	(Figure 8)	15	200	100	_	
Reset Removal Time	trem	·5.0	10	-110	-	ns
	(5)	10	20	-30	HARLES TO	
	(Figure 8)	15	30	-20	-	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.





#### PIN DESCRIPTIONS

**Preset Enable (Pin 3)** — If Reset is low, a high level on the Preset Enable input asynchronously loads the counter with the programmed values on P0, P1, P2, and P3.

**Inhibit (Pin 4)** — A high level on the Inhibit input prevents the Clock from decrementing the counter. With Clock (pin 6) held high, Inhibit may be used as a negative edge clock input.

Clock (Pin 6) — The counter decrements by one for each rising edge of Clock. See the Function Table for level requirements on the other inputs.

Reset (Pin 10) — A high level on Reset asynchronously forces Q0, Q1, Q2, and Q3 low and, if Cascade Feedback is high, causes the "0" output to go high.

"0" (Pin 12) — The "0" (Zero) output issues a pulse one clock period wide when the counter reaches terminal count (Q0 = Q1 = Q2 = Q3 = low) if Cascade Feedback is high and Preset Enable is low. When presetting the

counter to a value other than all zeroes, the "0" output is valid after the rising edge of Preset Enable (when Cascade Feedback is high). See the Function Table.

Cascade Feedback (Pin 13) — If the Cascade Feedback input is high, a high level is generated at the "0" output when the count is all zeroes. If Cascade Feedback is low, the "0" output depends on the Preset Enable input level. See the Function Table.

P0, P1, P2, P3 (Pins 5, 11, 14, 2) — These are the preset data inputs. P0 is the LSB.

Q0, Q1, Q2, Q3 (Pins 7, 9, 15, 1) — These are the synchronous counter outputs. Q0 is the LSB.

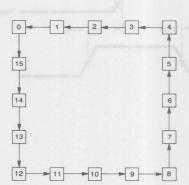
Vss (Pin 8) — The most negative power supply potential. This pin is usually ground.

 $\mbox{Vpp}$  (Pin 16) — The most positive power supply potential.  $\mbox{VpD}$  may range from 3 to 18 V with respect to  $\mbox{Vss}.$ 

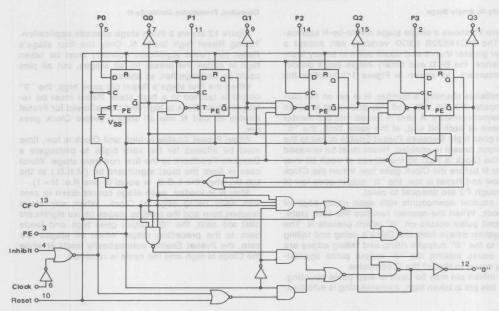
#### STATE DIAGRAMS

MC14522B

0 1 2 3 4 15 5 113 7 113 9 8 MC14526B



#### MC14522B LOGIC DIAGRAM (BCD Down Counter)



## MC14526B LOGIC DIAGRAM (Binary Down Counter)

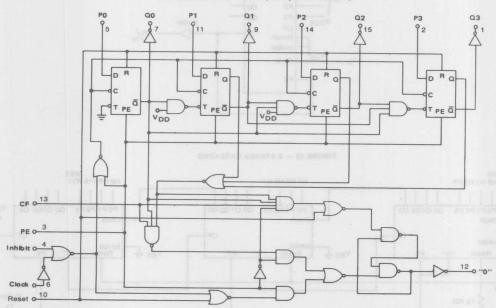


Figure 11 shows a single stage divide-by-N application. The MC14522B (BCD version) can accept a

number greater than 9 and count down in binary fashion. Hence, the BCD and binary single stage divideby-N counters (as shown in Figure 11) function the same.

same.

To initialize counting a number, N is set on the parallel inputs (P0, P1, P2, and P3) and reset is taken high asynchronously. A zero is forced into the master and slave of each bit and, at the same time, the "0" output goes high. Because Preset Enable is tied to the "0" output, preset is enabled. Reset must be released while the Clock is high so the slaves of each bit may receive N before the Clock goes low. When the Clock goes low and Reset is low, the "0" output goes low (if P0 through P3 are unequal to zero).

The counter downcounts with each rising edge of the Clock. When the counter reaches the zero state, an output pulse occurs on "0" which presets N. The propagation delays from the Clock's rising and falling edges to the "0" output's rising and falling edges are about equal, making the "0" output pulse approximately equal to that of the Clock pulse.

The Inhibit pin may be used to stop pulse counting. When this pin is taken high, decrementing is inhibited.

Cascaded, Presettable Divide-By-N

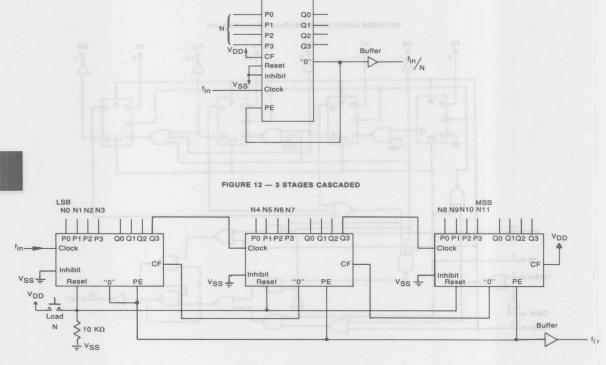
Figure 12 shows a three stage cascade application. Taking Reset high loads N. Only the first stage's Reset pin (least significant counter) must be taken high to cause the preset for all stages, but all pins could be tied together, as shown.

When the first stage's Reset pin goes high, the "0" output is latched in a high state. Reset must be released while Clock is high and time allowed for Preset Enable to load N into all stages before Clock goes low.

When Preset Enable is high and Clock is low, time must be allowed for the zero digits to propagate a Cascade Feedback to the first non-zero stage. Worst case is from the most significant bit (M.S.B.) to the L.S.B., when the L.S.B. is equal to one  $(i.e.\ N=1)$ .

After N is loaded, each stage counts down to zero with each rising edge of Clock. When any stage reaches zero and the leading stages (more significant bits) are zero, the "0" output goes high and feeds back to the preceding stage. When all stages are zero, the Preset Enable automatically loads N while the Clock is high and the cycle is renewed.

FIGURE 11 - + N COUNTER



# MC14527B

## BCD RATE MULTIPLIER

The MC14527B BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten inpu. pulses. This part may be used for arithmetic operations including multiplication and division. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- · Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin, lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

## TRUTH TABLE

											OUT	PUT	
						NUMBER OF PULSE							
D*	С	В	A	No. of Clock Pulses	Ēin	STROBE	CASCADE	CLEAR	SET	OUT	OUT	Eout	9
0	00	00	0	10	0	0	0	0	0	0	1	1 1	1
00000	0 1 1 1	1 0 0 1	0 1 0 1 0	10 10 10 10 10	0 0 0	0 0 0	0 0 0 0	0 0	0 0 0 0	2 3 4 5 6	2 3 4 5 6	1 1 1 1 1	1 1 1 1 1
0 1 1 1 1 1	10000	1 0 0 //	1 0 1 0 1	10 10 10 10 10	0 0 0 0	0 0 0	0 0 0 0	0 0 0	0 0 0 0	7 8 9 8 9	7 8 9 8 9	1 1 1	1 1 1 1 1
1 1 1 1 X	1 1 1 1 X	0 0 1 1 X	0 1 0 1 X	10 10 10 10	0 0 0 0 1	0 0 0	0 0 0 0	0 0 0	0 0 0 0	8 9 8 9	8 9 8 9	1 1 1 1	1 1 1 -
X X 1 0 X	XXXX	XXXX	XXXXX	10 10 10 10 10	0 0 0 0	1 0 0 0	0 1 0 0	0 0 1 1 1 0	0 0 0 0 1	0 1 10 0 0	1 0 10 1	1 1 1 1 0	1 1 0 0 1

X = Don't Care
\*D = Most Significant Bit

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

**BCD RATE MULTIPLIER** 



L SUFFIX CERAMIC PACKAGE CASE 620

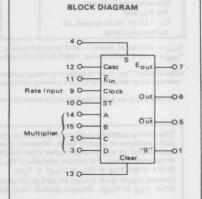


P SUFFIX PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



V<sub>DD</sub> = Pin 16 V<sub>SS</sub> = Pin 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tio	w*		25°C		Thi	gh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0		10	-	0.05	_	0	0.05	-	0.05	-
55	1	15	-	0.05	-	0	0.05	- 1	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	CATA C	4.95	_	Vdc
Vin = 0 or VDD	· OH	10	9.95		9.95	10	DAHO	9.95	_	1
- 111		15	14.95		14.95	15	-	14.95	_	
Input Voltage "0" Level	VIL	10	11.00		14.00	10	5767 G.	14.00	12/14 19/	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	AIL	5.0	8 ff elec	1.5	neground	2.25	1.5	dog bes	1.5	Vac
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	- Driesses A	3.0	Thomas and	4.50	3.0	mega 1	3.0	orti -
0		15	1 -111	4.0	their-ti-	6.75	4.0	-	4.0	James .
(V <sub>O</sub> = 13.5 or 1.5 Vdc) "1" Level	14	15	-	4.0	1200	6.75	4.0		4.0	
(VO = 0.5 or 4.5 Vdc)	VIH		100 500	DIGIT ELIES	and select	BOION I	CHARGETTS I			1
9		5.0	3.5	4-000	3.5	2.75	icin <del>t</del> orse	3.5	CO SERVICE	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	-	7.0	5.50	-	7.0	-	
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	-	11.0	_	
Output Drive Current (AL Device)	ЮН				Kin Wa	S and missist	2 C = 100	RE SUMI		mAdc
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	
(VgH = 4.6 Vdc)		5.0	-0.64	77.2	-0.51	-0.88	S 4 80	-0.36	in main	1 2
(VOH = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	nitro s	-0.9	not wilen	10
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	-	-2.4	-	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.64	1000	0.51	0.88	-	0.36	-	mAdo
(VOL = 0.5 Vdc)	1000	10	1.6	-	1.3	2.25	_	0.9	179U 530	
(VOL = 1.5 Vdc)		15	4.2	ns. worte	3.4	8.8	musit i	2.4	ered "	
Output Drive Current (CL/CP Device)	ГОН				-				SCHOOL	mAdc
(VOH = 2.5 Vdc) Source	OH	5.0	-2.5	_	-2.1	-4.2	Sund	-1.7		IIIAGC
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	_	-0.44	-0.88	- Such	-0.36	THE PERSON	
(VOH = 9.5 Vdc)		10	-1.3		-1.1	-2.25	freque às	-0.36	19/16, 1EB	0
(V <sub>OH</sub> = 13.5 Vdc)	100	15	-3.6	_	-3.0	-8.8		-2.4		
0.1					-			-		-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36		mAdc
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3	-	1.1	2.25	Negth Pa	0.9	UTAR	SENDO.
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8	-	2.4		T.
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	0.82 + 0	± 0.3	-	±0.00001	±0.3		±1.0	μAdc
Input Capacitance	Cin	-	-0 cm)	on 40	-	5.0	7.5	artes- Into	of white	pF
(V <sub>in</sub> = 0)			-			nice la con-	000			
Quiescent Current (AL Device)	IDD	5.0	_	5.0	-	0.005	5.0	-	150	μAdc
(Per Package)	יטטי	10	88	10		0.005	10	45, 200000	300	Jan de
(applied chares) 15000004 SM	100	15	084 vi 6	20	_	0.010	20	mu <u>t</u> anio	600	the same
0.:					-	-	-			
Quiescent Current (CL/CP Device)	IDD	5.0	- 08	20	-	0.005	20	-	150	μAdc
(Per Package)		10	engy Georg	40	of ut Topic	0.010	40	Jan Trees	300	St man
		15	- 77	80	-	0.015	80	100700	600	Juliany!
Total Supply Current**†	IT	5.0	Class o		IT = (0.	.85 μA/kHz	) f + Ipp	THE STATE OF		μAdc
(Dynamic plus Quiescent,		10				75 μA/kHz				
Per Package)	1 4 10 10	15			IT = (2.	.6 μA/kHz	f + IDD	)		
(C <sub>L</sub> = 50 pF on all outputs, all			FURFILL							1
buffers switching)			To the same							

 $^{\circ}$ T $_{low}$  =  $-55^{\circ}$ C for AL Device,  $-40^{\circ}$ C for CL/CP Device. T $_{high}$  =  $+125^{\circ}$ C for AL Device,  $+85^{\circ}$ C for CL/CP Device. †To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

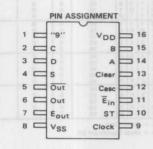
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where: IT is in  $\mu$ A (per package), CL in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.0012.

\*\*The formulas given are for the typical characteristics only at 25°C.

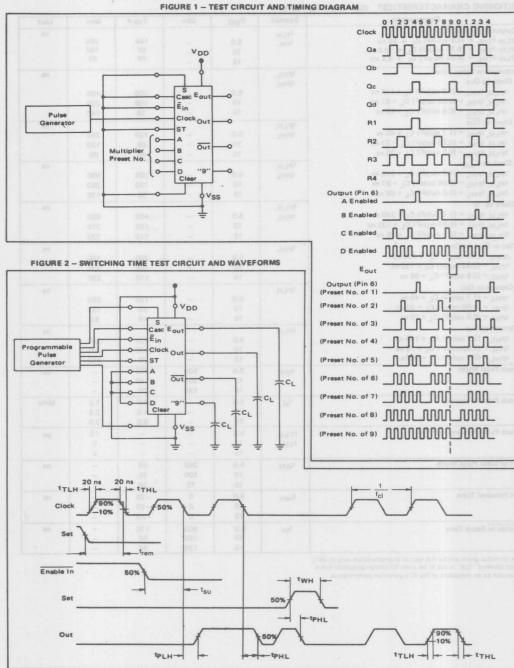
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

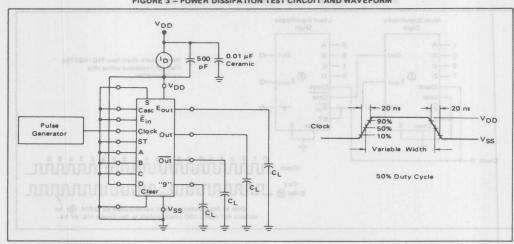


Characteristic	Symbol	VDD	Min	Тур#	Max	Unit
Output Rise and Fall Time	tTLH-	5.0		100	200	ns
TLH, tTHL = (1.5 ns/pF) C <sub>L</sub> + 25 ns	<sup>†</sup> THL	5.0		50	100	1
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		10 15	80.7-	40	80	
ropagation Delay Time	tPHL.		· proces	0		ns
Clock to Out	TPHL					
tpLH, tpHL = (1.7 ns/pF) CL + 115 ns		5.0	1 -1 -1 -1	200	400	
tpLH tpHL = (0.66 ns/pF) CL + 67 ns	10 00	10	- 1	100	200	-
tpLH tpHL = (0.5 ns/pF) CL + 45 ns	13.	15		70	140	neiu-1
Clock to Out	tPLH.	-	100			ns
tpLH, tpHL = (1.7 ns/pF) CL + 40 ns	tPHL	5.0	_198	125	250	-
tpLH tpHL = (0.66 ns/pr) CL + 32 ns	1111	10	1000 - FF	65	130	1000
tp_H tpHL = (0.5 ns/pF) CL + 20 ns		15	- 9	45	90	1 100
Clock to Equit	tPLH.	-	+	10 100 200		ns
tpLH, tpHL = (1.7 ns/pF) CL + 210 ns	tPHL	5.0	0	295	590	
tplH, tpHL = (0.66 ns/pF) CL + 97 ns	THE	10	16/03	130	260	
tp_H, tpHL = (0.5 ns/pF) CL + 60 ns		15	ded -	85	170	
Clock to "9"	*====		+	-		ns
	tPLH,	5.0		400	800	ma
tpLH, tpHL = (1.7 ns/pF) CL + 315 ns	tPHL	10		155	310	
tplH, tpHL = (0.66 ns/pF) CL + 122 ns	1	15		110	220	
tpLH, tpHL = (0.5 ns/pF) CL + 85 ns		15		110	220	-
Set or Clear to Out	tPHL					ns
*tpHL = (1.7 ns/pF) CL + 295 ns	29,576	5.0	ma vidilines s	380	760	BRUSE
tpHL' = (0.66 ns/pF) CL + 132 ns		10	-	165	330	-
tpHL = (0.5 ns/pF) CL + 85 ns		15	-	110	220	
Cascade to Out	tPLH					ns
tpHL = (1.7 ns/pF) CL + 40 ns		5.0	- 1	125	250	
tpHL = (0.66 ns/pF) CL + 32 ns		10	era A A	65	130	
tpHL = (0.5 ns/pF) C <sub>L</sub> + 20 ns		15	-	45	90	1. 5
Strobe to Out	tPLH		7.00			ns
tpHL = (1.7 ns/pF) CL + 145 ns		5.0	-	230	260	
tpHL = (0.66 ns/pF) CL + 72 ns		10	-0-THO	105	210	Portug
tpHL = (0.5 ns/pF) CL + 45 ns		15	-	70	140	10071908
Clock Pulse Width	twH	5.0	500	250	3 -	ns
	L Date	10	200	110	-	
		15	150	80	4 -	
Clock Pulse Frequency	fcl	5.0	Janes - Inge	2.0	1.2	MHz
	1	10	-	4.5	2.5	
		15	-	6.0	3.5	
Clock Pulse Rise and Fall Time	tTLH,	5.0	- E0.1	_	15	μς
Tonnering and Comments and Comm	tTHL.	10		_	5	
	I III	15	-	_	4	
Set or Clear Pulse Width	twH	5,0	240	80	_	ns
The state of the s	HW	10	100	35		110
	DE TOR	15	75	30	2000	
Set Removal Time		5.0	0	-20		-
ot namova: Time	trem			-	7007	ns
		10	0	-10	2004-1	
		-		-7.5		-
Enable In Setup Time	<sup>t</sup> su	5.0	400	175	-1	ns
	The same of	10	150	60		1 94 3
		15	120	45	-	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C. #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



## FIGURE 3 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



#### LOGIC DIAGRAM

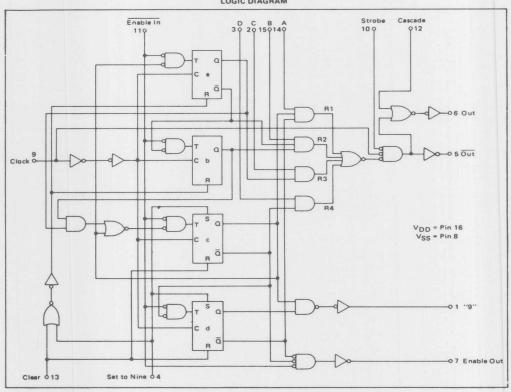
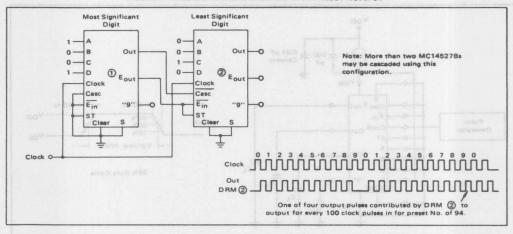
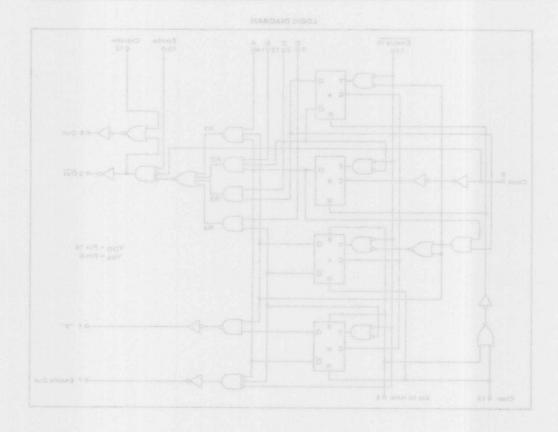


FIGURE 4 - TWO MC14527Bs IN CASCADE WITH PRESET NO. of 94





# MC14528B

## **DUAL MONOSTABLE MULTIVIBRATOR**

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C<sub>X</sub> and R<sub>X</sub>.

- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement with the MC14538B and MC14548B.

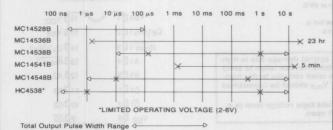
#### MAXIMUM RATINGS\* (Voltages Referenced to Voc.)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

## THE MC14528B IS NOT RECOMMENDED FOR NEW DESIGNS

# ONE-SHOT SELECTION GUIDE

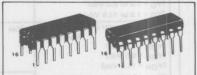


Recommended Pulse Width Range ×

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL
RETRIGGERABLE/RESETTABLE
MONOSTABLE MULTIVIBRATOR



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

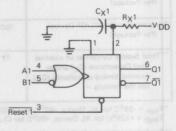
#### ORDERING INFORMATION

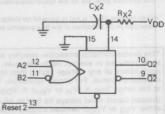
A Series: -55°C to +125°C

MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### BLOCK DIAGRAM





 $V_{DD}$  = Pin 16  $V_{SS}$  = Pin 1, Pin 8, Pin 15  $R_{\chi}$  and  $C_{\chi}$  are external components

		VDD	Tio	T <sub>low</sub> *		25°C			Thigh*	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Мах	Min	Max	Uni
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vde
V <sub>in</sub> = V <sub>DD</sub> or 0		10	-	0.05	-	0	0.05	-	0.05	
2016 001675		15	-	0.05	-	0	0.05	NA TALL	0.05	
"1" Level	VOH	5.0	4.95	1 1 1 1 1 1 1 1 1	4.95	5.0	_	4.95	_	Vde
V <sub>in</sub> =0 or V <sub>DD</sub>	OH	10	9.95	-	9.95	10	-	9.95	_	
HERMAN WHILE THE STATE STATE AND ASSESSED.	531	15	14.95	_	14.95	15	_	14.95	_	
Input Voltage "0" Level	VIL	inte	Arronam	stastis	n alo	recolsten	feub &	81 8834	argul s	Vde
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	11.	5.0	0.0200	1.5	111/20 10	2.25	1.5	ad warn t	1.5	lum
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	others a	3.0	r_ser	4.50	3.0	po lugior	3.0	DONG-
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	138	15	w/Lbne	4.0	neazoo	6.75	4.0	ra batan	4.0	Haldw-
"1" Level	VIH	10		4.0	-	0.75	1.0		4.0	+
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	VIH	5.0	3.5	1	2.5	2.75	Andrew A	3.5		Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)	-	10	7.0	-	7.0	5.50	DETERM		12 10m	V 00
(VO = 1.5 or 13.5 Vdc)		15	11.0	_	11.0	8.25	IIA non	7.0	Sinds P	10
		15	11.0		11.0	-		11.0		-
Output Drive Current (AL Device)	ЮН			neltri	abox flu	11813 10 E	19588TI	HOLI BIOL	FIRST S	mAd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-1.2	aby	-1.0	-1.7	egnsf	-0.7	Alderes	.0-
(V <sub>OH</sub> = 4.6 Vdc)	5 In 1	5.0	-0.64	S south	-0.51	-0.88	owT o	-0.36	Addina 3	0
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	SERVICE AND ADDRESS OF	-1.3	-2.25	G SESSO S	-0.9	Senatory	
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	BINELL	-3.4	-8.8	-	-2.4		-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	COF OU	0.51	0.88	A 173010	0.36	N-101-III	mAd
(V <sub>OL</sub> = 0.5 Vdc)	ARES -	10	1.6	-	1.3	2.25	-	0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	-	2.4	-	1
Output Drive Current (CL/CP Device)	ІОН	-								mAd
(VOH = 2.5 Vdc) Source		5.0	-1.0	-	-0.8	-0.7	-	-0.6	-	-
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	ori Taposi	-0.36	write 19 I	ALTERNIE
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25		-0.9	-	Too
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	V -	-3.0	-8.8	AD STATE OF	-2.4	-	100
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	2 12	0.44	0.88	_	0.36	(RD <u>D</u> UR)	mAd
(VOL = 0.5 Vdc)	OL	10	1.3	of E De-	1.1	2.25	to TOI to	0.9	Committee	
(V <sub>OL</sub> = 1.5 Vdc)	9	15	3.6	W. E. V.	3.0	8.8		2.4	_	1100
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAd
Input Current (CL/CP Device)	lin	15	- 17	± 0.3		±0.00001	± 0.3		±1.0	μAd
Input Capacitance		10	08.6 8 7	- 0.0	-	5.0	7.5			pF
(Vin = 0)	Cin			_	-	5.0	7.5	101 washing	- 1	PF
		91 1	-			- SERRIBORO	-	al arms	The same of the same	1
Quiescent Current (AL Device)	IDD	5.0	orton yair	5.0	it of oge	0.005	5.0	MINE HOOF	150	μAd
(Per Package)		10	- 02	10	Smutt Of	0.010	10	Other Park	300	Setul 8
100		15	Tage.	20	MONTH OF	0.015	20	00000	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20	-	150	μAd
(Per Package)		10	-	40	-	0.010	40	+	300	
1 2		15	-	80	m	0.015	80		600	
**Total Supply Current at an external load Capacitance (C <sub>L</sub> ) and at external timing capacitance (C <sub>X</sub> ), use the formula —	lΤ	- 00	IT(CL	, C <sub>X</sub> ) = [ here: I <sub>T</sub>	in µA (per	CX)VDDf + circuit), CL Vdc, f in kH	and CX	in pF, RX	in megohr	x 10 <sup>-1</sup>

 $^{\circ}T_{low}$  = -55 $^{\circ}$ C for AL Device, -40 $^{\circ}$ C for CL/CP Device.  $T_{high}$  = +125 $^{\circ}$ C for AL Device, +85 $^{\circ}$ C for CL/CP Device.

\*\* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

PIN ASSIGNMENT

Vss 1 16 VDD

Cx1/Rx1 2 15 Vss

Reset 1 3 14 Cx2/Rx2

A1 4 13 Reset 2

B1 5 12 A2

Q1 6 11 B2

Q1 7 10 Q2

Vss 8 9 Q2

Characteristic	Symbol	C <sub>X</sub>	R <sub>X</sub> kΩ	V <sub>DD</sub> Vdc	Min	Тур#	Max	Unit
Output Rise and Fall Time	tTLH.	-	-					ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	THL			5.0	-	100	200	
$t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$				10	-	50	100	
$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$			NI-UIN	15	-	40	80	
Turn-Off, Turn-On Delay Time − A or B to Q or Q	tPLH,	15	5.0			h-12-	0	ns
tPLH, tPHL = (1.7 ns/pF) CL + 240 ns	tPHL		m A	5.0	-	325	650	
tpLH, tpHL = (0.66 ns/pF) CL + 87 ns			June	10	-c07	120	240	EP I
tpLH, tpHL = (0.5 ns/pF) CL + 65 ns				15	-	90	180	
Turn-Off, Turn-On Delay Time - A or B to Q or Q	tPLH,	1000	10		F 9 8			ns
$t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620 \text{ ns}$	tPHL			5.0	-	705	-	
$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257 \text{ ns}$				10	-	290	-	
$t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185 \text{ ns}$				15	-	210	-	
Input Pulse Width - A or B	tWH	15	5.0	5.0	150	70	-	ns
	HOSTANI	SOLO RUNG	05 - E	10	75	30	-	
	COLUMN TO THE			15	55	30	-	
	tWL	1000	10	5.0	-	70	-	ns
			1	10	-	30	-	
		Reck	0 6	15	11-	30	-	
Ourput Pulse Width - Q or Q	tw	15	5.0	5.0	17-17	550	-	ns
(For C <sub>X</sub> < 0.01 μF use graph for appropriate V <sub>DD</sub> level.)	.44		take 1	10	1	350	-	
			1000	15	10-	300	-	
Output Pulse Width - Q or Q	tw	10,000	10	5.0	15	30	45	μs
(For C <sub>X</sub> > 0.01 μF use formula:			E-ball	10	10	50	90	
tw = 0.2 Rx Cx Ln [VDD - VSS])+				15	15	55	95	
Pulse Width Match between Circuits in the same package	t1 - t2	10,000	10	5.0	-	6.0	25	%
	11.12			10	1	8.0	35	
				15	-	8.0	35	
Reset Propagation Delay — Reset to Q or Q	tPLH.	15	5.0	5.0	-	325	600	ns
20 100 20 105	tPHL		1.00	10	100	90	225	
				15	-	60	170	
		1000	10	5.0	7-	1000	_	ns
	THE S	5.52		10	-	300	-	
		- 1-0-	4 .0	15	12	250	-	
Retrigger Time	trr	15	5.0	5.0	0		-	ns
SOS = stoyD yteD		9	1	10	0	-	-	
			88	15	0	-	-	
		1000	10	5.0	0	-	-	ns
				10	0	-	-	
				15	0	-	-	
External Timing Resistance	RX	e e e e	-	-	5.0	-	1000	kΩ
External Timing Capacitance	CX	-	_	_		lo Limits	20	μF

 $R_X$  is in Ohms,  $C_X$  is in farads,  $V_{DD}$  and  $V_{SS}$  in volts,  $PW_{out}$  in seconds. If  $C_X>$  15  $\mu F$ , Use Discharge Protection Diode  $D_X$ , per Fig. 9.

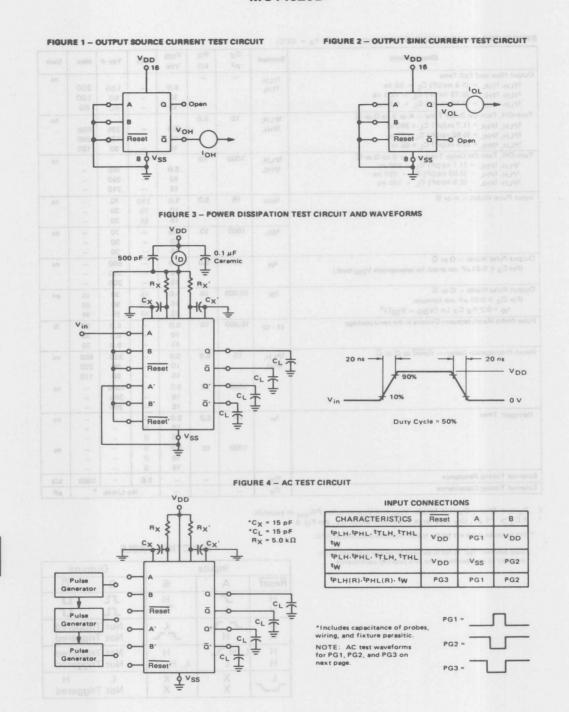
\*\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## **FUNCTION TABLE**

	Inputs	Outputs				
Reset	Α	В	Q	ā		
H	5	7	Y	T T		
H	<b>√</b> 1	2		iggered iggered		
H	L, H, <b>\</b> L	H L, H, <b>√</b>		iggered iggered		
~_~	X	X	L Not Tr	H iggered		

## MC14528B



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## MC14528B

## FIGURE 5 - AC TEST WAVEFORMS

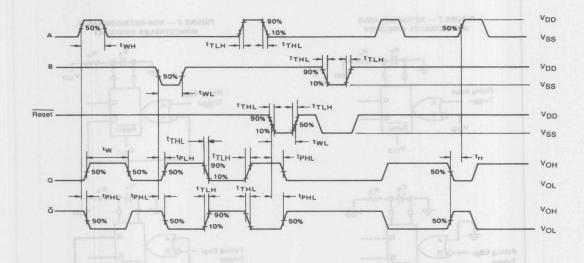


FIGURE 6 - PULSE WIDTH versus CX

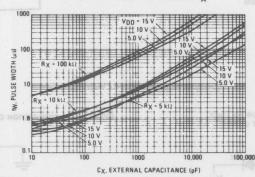
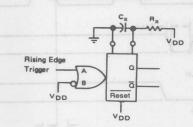


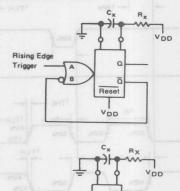
FIGURE 7 — RETRIGGERABLE MONOSTABLES CIRCUITRY



Falling Edge B Reset

VDD

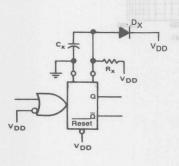
FIGURE 8 — NON-RETRIGGERABLE MONOSTABLES CIRCUITRY

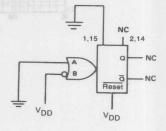


Falling Edge B G Reset

FIGURE 9 — USE OF A DIODE TO LIMIT POWER DOWN CURRENT SURGE

FIGURE 10 — CONNECTION OF UNUSED SECTIONS







### MC14529B

### **DUAL 4-CHANNEL ANALOG DATA SELECTOR**

The MC14529B analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
- 3-State Outputs
- Linear "On" Resistance
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter 0.5	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

W	Z	Α	В	STY	STX
Y	X0	0	0	1	1
Y	X1	1	0	1	1
Y	X2	0	1	1001	1
Y	Х3	1	1	_1	1
X0	)	0	0	0	.1
XT	cer ;	1	0	0	1
X2	091 3	0	1	0	1
X3	031 2	1	- 1	0	1
YO	0001	0	0	1	0
Y1	our '	1	0	1	0
Y2		0	1	1	0
Y3	081	1	1	1	0

Dual 4-Channel Mode 2 Outputs

Single 8-Channel Mode 1 Output (Z and W tied together)

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL ANALOG
DATA SELECTOR
OR
8-CHANNEL ANALOG
DATA SELECTOR



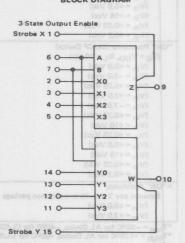
L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### BLOCK DIAGRAM



VDD = Pin 16

VSS = Pin 8

Characteristic	Figure	Symbol	VSS	VDD	Tlo	w		25°C		. h	igh °	Uni
Constructoristic	regure	бушьог	Vdc	Vdc	Min	Max	Min	Тур#	Max	Min	Max	
Output Voltage "0" Lev	el 1	VOL	0.0	5.0	-	0.05	-	0	0.05	-	0.05	Vd
$V_{in} = 0$		801	la us	10	AG !	0.05	VIA	0	0.05	346	0.05	
***			-	15	-	0.05	-	0	0.05	-	0.05	
"1" Lev	el	VOH	0.0	5.0	4.95	17. <del>4.</del> 31	4.95	5.0	124.0	4.95	0.155	1
TEOM YEAR COMPLEMENTARY MOST	die	011	eb er	10	9.95		9.95	10		9.95	A10-00	
V <sub>in</sub> = V <sub>DD</sub>		1		15	14.95	-	14.95	15	-	14.95	-	
Input Voltage "0" Lev	el 2	VIL	0.0			3		Diffe ships by		Page 2		Vd
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		1	100.00	5.0	-	1.5	-	2.25	1.5	-	1.5	
(Vo = 9.0 or 1.0 Vdo)	1011	B 16	S. Sellin	10	-	3.0	-	4.50	3.0	-	3.0	
(Vo = 12 5 or 1 5 Vdo)				15	- Tarlinak	4.0	-	6.75	4.0	-	4.0	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) "1" Lev	el	VIH	0.0	5.0	3.5	-	3.5	2.75	-	3.5	-	1
(V <sub>O</sub> = 1.0 or 9.0 Vdc)				10	7.0	-	7.0	5.50	970	7.0	1000	1
(V <sub>O</sub> = 1.5 or 13.5 Vdc)				15	11	-	11	8.25	0-0	11	24	1
Input Current (AL Device) Control		· Iin	0.0	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	MA
Input Current (CL/CP Device) Control	1	lin	0.0	15	_	±0.3	-	±0.00001	±0.3	-	±1.0	μΑ
MARKET CONTROL OF THE PROPERTY	+	-	0.0	10	No. of Street, or other Persons	20.0	W 0.5	-0.0001	20.0	17 170	- 1.0	р
Input Capacitance (V <sub>in</sub> = 0) Control	50000	Cin	0.0	2000	1 197	102200		5.0	7.5	a Links	mich.	P
Switch Input	10000	CONTRACTOR OF	L	DILECT.		Paralle S	6	8.0	7.5	inter	de D	
Switch Output		199	1	_	_	1,770	T.	20	-	-	100	
Feed Through								0.3		_		
01 .0 .101011	3	1		5.0		1.0	-	0.001 -	1.0		60	шА
(D Dt)	3	IDD	aparticus.	10	_	1.0	-	0.001	1.0	-	60	MA
(Per Package)				15	nok o	2.0	the state of	0.002	2.0	STAR	120	RIS:
0:	-	-	-	-		-	-	-	-	-		-
Quiescent Current (CL/CP Device)	3	IDD	-	5.0	_	5.0	-460	0.001	5.0	-	70	μΑ
(Per Package)		87 + 9	8.0 -	10	_	5.0	_	0.002	10	Arching	140	10
	1.00	-		10		10	-	0.003	10	-	140	-
"ON" Resistance (AL Device)	4,5,6	RON			in marks							0
(V <sub>C</sub> = V <sub>DD</sub> , R <sub>L</sub> = 10 kΩ) (V <sub>in</sub> = +5.0 Vdc)		100	-5.0	5.0	1814	400		200	480	10 10	640	Hal
(V <sub>in</sub> = +5.0 Vdc) (V <sub>in</sub> = -5.0 Vdc)	10 28	904	-5.0	5.0		400	1900	200	480	100	640	.0
(Vin = ±0.25 Vdc)	1	D 1-150	89 -			400		190	480	1	640	10.5
(V <sub>in</sub> = +7.5 Vdc)		- 68	-7.5	7.5	_	240	100 E	160	270	-	400	
(V <sub>in</sub> = -7.5 Vdc)	-		1	1.0	-	240	-	160	270	-	400	
(Vin = ±0.25 Vdc)		DO VAIN	MAN DA	1	-	240	9 000	120	270	976 95	400	77,225
(Vin = +10 Vdc)		- 17 TO -	0	10		400	100000	180	480	-	640	100
(Vin = +0.25 Vdc)		1	1		-	400	-	180	480	-	640	
(Vin = +5.6 Vdc)	-	-		-	-	400	-	220	480	-	640	-
(Vin = +15 Vdc)			0	15		250	PATE I	180	270	-	400	
(Vin = +0.25 Vdc)					-	250	-	180	270	-	400	
(V <sub>in</sub> = +9.3 Vdc)					-	250	-	215	270	2-	400	(Ta
"ON" Resistance (CL/CP Device)	4,5,6	RON				1	1	1500	0	0	7.1	1 5
(V <sub>C</sub> = V <sub>DD</sub> , R <sub>L</sub> = 10 kΩ)		2000 F	10050	THE PARTY		1 3		130	1	0		18
(Vin = +5.0 Vdc)			-5.0	5.0	-	410	-	200	480	1 -	560	15
(Vin = -5.0 Vdc)					-	410	- DX	200	480	5	560	1
(V <sub>in</sub> = +0.25 Vdc)					-	410	Tex	190	480	9-	560	1 5
(V <sub>in</sub> = +7.5 Vdc)		eboth le	-7.5	7.5	8 - 1	250	TX	160	270	-	350	1
(V <sub>in</sub> = -7.5 Vdc)	1			rafeO.	-	250	-	160	270	3 -	350	
(V <sub>in</sub> = ±0.25 Vdc)	1000	POSET DE	0	10	-	250 410	27	120	270 480	0 -	350 560	10
(V <sub>in</sub> = +10 Vdc) (V <sub>in</sub> = +0.25 Vdc)			0	10	-	410	BY	180	480	-	560	0
(V <sub>in</sub> = +5.6 Vdc)						410	EY	220	480		560	10
(Vin = +15 Vdc)			0	15		250	(50)	180	270	× ]	350	0
(Vin = +0.25 Vdc)			0	15		250	10000	180	270		350	-
(Vin = +9.3 Vdc)						250		215	270		350	
△"ON" Resistance		AP-	-	-		200		210	270	-	300	. 5
Between any 2 circuits in a common package		ARON										1 2
			-5.0	5.0				15			- The same of	
(Vin = ±5.0 Vdc)						0 OT V						

<sup>&</sup>quot;Tlow = -55°C for AL Device, -40°C for CL/CP Device
"Tloy = -125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### SWITCHING CHARACTERISTICS (TA = 25°C)

Characteristic	Flavor	Combal	W	M	0.01-	Tree 4	80	Uni
	Figure	Symbol	VSS	VDD	Min	Тур #	Max	Uni
Vin to Vout Propagation Delay Time	7	tPLH, tPHL	0.0	5.0	-	20	40	ns
$(C_L = 50 \text{ pF}, R_L = 1.0 \text{ k}\Omega)$				10	- 1	10	20	
				15	-	8.0	15	
Propagation Delay Time, Control to	8		0.0	5.0		140	400	ns
	0	tPLZ, tPZL,	0.0				160	ns
Output, Vin = VDD or VSS	profite of the	tPHZ, tPZH		10	_	70		1
$(C_L = 50 \text{ pF}, R_L = 1.0 \text{ k}\Omega)$				15	- 1	50	120	
Crosstalk, Control to Output	9	_	0.0	5.0	-	5.0	-	m\
$(C_L = 50 \text{ pF}, R_L = 1.0 \text{ k}\Omega$	-			10	1-0	5.0	_	
$R_{out} = 10 k\Omega$ )	(within )		100	15	-	5.0	-	
	9 10						0.5	1
Control Input Pulse Frequency	10	fin	0.0	5.0	-	5.0	2.5	МН
$(C_L = 50 \text{ pF}, R_L = 1.0 \text{ k}\Omega)$				10	-	10	6.2	100
Cont.	Comments.			15	_	12	8.3	
Noise Voltage	11,12	_	0.0	5.0	_	24	_	nV
(f = 100 Hz)				10		25	_	
100 127 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2				15	_	30	_	Cyc
						-		
				5.0	_	12	_	
				10		12		
	a 360034		- Sur	15	P. DEVID	15	- C SYBLIGH	
The state of the s					-	CHARLES THE STATE OF		-
Sine Wave Distortion	-	-	-5.0	5.0	-	0.36	-	%
(Vin = 1.77 Vdc RMS							W-VIB-	715
Centered @ 0.0 Vdc,				1.16.79	001 5	100	a a Area	
$R_L = 10 \text{ k}\Omega, f = 1.0 \text{ kHz}$				and the same of	1			
Off-Channel Leakage Current		loff						n/
		1011	-5.0	5.0	1	± 0.001	±125	1 "
(V <sub>in</sub> = +5.0 Vdc, V <sub>out</sub> = -5.0 Vdc)			-5.0	5.0	(4)	± 0.001	± 125	1
$(V_{in} = -5.0 \text{ Vdc}, V_{out} = +5.0 \text{ Vdc})$				100000	-	The Control of the Co	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
$(V_{in} = +7.5 \text{ Vdc}, V_{out} = -7.5 \text{ Vdc})$	LI LEWIS		-7.5	7.5	-	±0.0015	± 250	1
$(V_{in} = -7.5 \text{ Vdc}, V_{out} = +7.5 \text{ Vdc})$			-7.5	7.5		±0.0015	± 250	-
Insertion Loss	13	_	-5.0	5.0			planter.	dB
(Vin = 1.77 Vdc			2012					
RMS centered @ 0.0 Vdc,			1		1	June -		Court
f = 1.0 MHz)						TABLE OF		
	188.5.9		1		reinterio		A DESTRUCTION	1
I <sub>loss</sub> = 20 Log <sub>10</sub> Vout Vin					WE B	No.V		
V <sub>in</sub>				1			NE AND	- 9
	1 1 1 1 1 1 1	the last through the					1	
$(R_L = 1.0 \text{ k}\Omega)$				(E )	-	2.0	-	
$(R_L = 10 \text{ k}\Omega)$					-	0.8	_	
$(R_L = 100 \text{ k}\Omega)$	1600,00000	NAME OF PERSONS ASSESSED.	Same Di	interpret	-	0.25	_	1000
$(R_L = 1.0 M\Omega)$	THE PARTY	A F CONTRACTOR	1 BULLET 1-04		_	0.01	_	
Bandwidth (-3 dB)	_	BW	-5.0	5.0		BEIGHE -		МН
(V <sub>in</sub> = 1.77 Vdc	1 1 1 1 1 1 1 1 1							
RMS centered @ 0.0 Vdc)	1	755						
$(R_1 = 1.0 \text{ k}\Omega)$	1 1			-		35		
$(R_L = 10 \text{ k}\Omega)$				a Lange	Lateral Control	28		
	San Language		1	2014	1 7 %	27		1
	1	3		1		26		-
$(R_L = 100 \text{ k}\Omega)$ $(R_L = 1.0 \text{ M}\Omega)$		100 12 100 100 100 100 100 100 100 100 1	1025	1	1	20		
(R <sub>L</sub> = 1.0 MΩ)	1		-5.0	5.0	199			MH
(R <sub>L</sub> = 1.0 MΩ)	1-4	Oit #	3.0					1
(R <sub>L</sub> = 1.0 MΩ) Feedthrough and Crosstalk	77	Con V	5.0		15000		- Hard and replaced	177779
(R <sub>L</sub> = 1.0 MΩ) Feedthrough and Crosstalk	A	Cit ¥	3.0		1			
$(R_L = 1.0 \text{ M}\Omega)$ Feedthrough and Crosstalk $20 \text{ Log}_{10}  \frac{V_{out}}{V_{in}} = -50 \text{ dB}$	A	On E	3.0					
$(R_L = 1.0 \text{ M}\Omega)$ Feedthrough and Crosstalk $20 \text{ Log}_{10}  \frac{\text{Yout}}{\text{Vin}} = -50 \text{ dB}$ $(R_L = 1.0 \text{ k}\Omega)$	4	Charles Services	3.0		1	850	_	
$(R_L = 1.0 \text{ M}\Omega)$ Feedthrough and Crosstalk $20 \text{ Log}_{10}  \frac{V_{out}}{V_{in}} = -50 \text{ dB}$	A	City No.	3.0			850 100	E	
$(R_L = 1.0 \text{ M}\Omega)$ Feedthrough and Crosstalk $20 \text{ Log}_{10}  \frac{\text{Yout}}{\text{Vin}} = -50 \text{ dB}$ $(R_L = 1.0 \text{ k}\Omega)$	4	1025 N	3.0				-	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

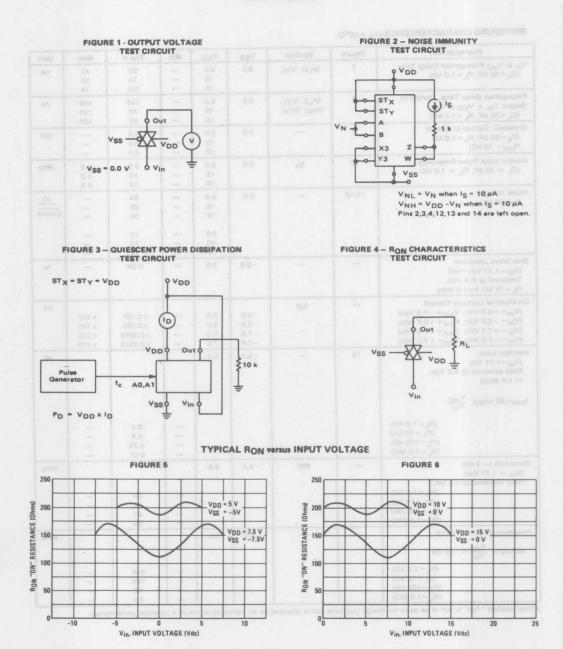


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

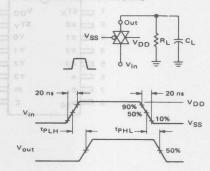


FIGURE 9 - CROSSTALK TEST CIRCUIT

# FIGURE 8 - TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

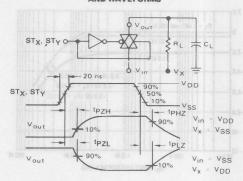


FIGURE 10 - FREQUENCY RESPONSE TEST CIRCUIT

X,Y Input

+2.5 Vdc 0.0 Vdc -2.5 Vdc X,Y Input

\$ RL

VFeedthrough

I Vss

VDD

VSS

VDD

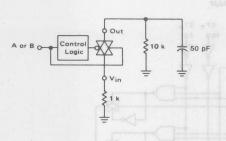
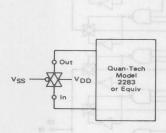
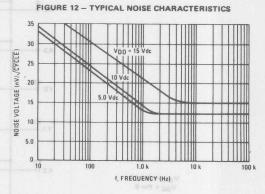


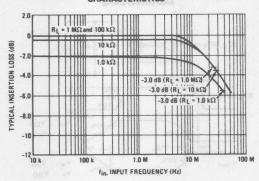
FIGURE 11 - NOISE VOLTAGE TEST CIRCUIT

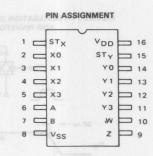




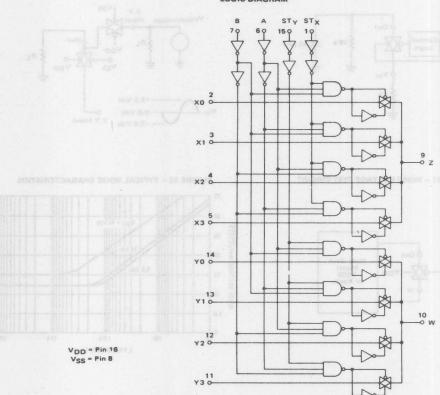
### MC14529B

FIGURE 13 - TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS





LOGIC DIAGRAM



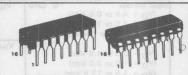


## MC14530B

### **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL 5-INPUT MAJORITY LOGIC GATE



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### **DUAL 5-INPUT MAJORITY LOGIC GATE**

The MC14530B dual five-input majority logic gate is constructed with P-channel and N-channel enhancement mode devices in a single monolithic structure. Combinational and sequential logic expressions are easily implemented with the majority logic gate, often resulting in fewer components than obtainable with the more basic gates. This device can also provide numerous logic functions by using the W and some of the logic (A thru E) inputs as control inputs.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

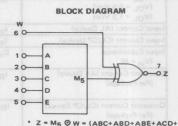
Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin. lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

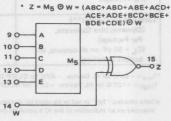
\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

### LOGIC TABLE

INPUTS A B C D E	W	Z
For all combinations of inputs where three	0	1
or more inputs are logical "0".	1	0
For all combinations of inputs where three	0	0
or more inputs are logical "1".	1	1

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{Out}) \leqslant V_{DD}.$  Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.





\*M5 is a logical "1" if any three or more inputs are logical "1".

⊚ ≡ Exclusive NOR ≡ Exclusive OR

#### TRUTH TABLE

	1110		
ſ	M <sub>5</sub>	W	Z
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

V<sub>DD</sub> = Pin 16 V<sub>SS</sub> = Pin 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

	313	VDD	Tio	w°		25°C		Thi	gh °	1
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Un
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vd
Vin = VDD or 0	02	10		0.05	_	0	0.05	_	0.05	-
1111 1 000 51 5		15	-	0.05	_	0	0.05	_	0.05	
"1" Level	VOH	5.0	4.95		4.95	5.0		4.95	110-	Vd
Vin = 0 or VDD	TOH	10	9.95	LAT U	9.95	10	M TUP	9.95	UU.	1
TIM COLUMN		15	14.95		14.95	15		14.95		
Input Voltage "0" Level	VIL	0	111111111111111111111111111111111111111	St. extend	1901 VIII	Marie 199	didnit is	14.00	PECINI, BIL	Vd
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	11.	5.0	mizz ni	1.2	north_Inter	2.25	1.25	M tights lit	1.15	Vo
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	NAME OF TAXABLE PARTY.	2.5	THE REAL PROPERTY.	4.50	2.5	nuctures.	2.4	iom:
$(V_0 = 13.5 \text{ or } 1.5 \text{ Vdc})$	8	15		3.0	signif v		3.0	ation made	2.9	518
"1" Level	M	15	712-11	3.0	300-110	6.75	0.0		2.5	2 22
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	VIH		3.85	A SULL OF A SULL	101 State 195	0.75	SOO THES			1
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		5.0		DATE: NO	3.75	2.75	nor-un s	3.75	10 1=1 01	Vd
	3 1	10	7.6	HOUSE SEED	7.5	5.50	13 TOTAL	7.5	8012-10 1	LICE
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	12.1	-	12	8.25	-	12	-	
Output Drive Current (AL Device)	ОН			ak sin						mA
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2		-1.7	ale To also	50
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	CARGOLI III	-0.36		1
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	0.8-10	-0.9	pV+log	8 0
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	-	-2.4	-	100
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	DITTED TO	0.51	0.88	0.00	0.36	T Stitled	mA
(VOI = 0.5 Vdc)	0-	10	1.6	offices:	1.3	2.25	- ALS TO 1	0.9	- Contact	
(VOL = 1.5 Vdc)		15	4.2	-	3.4	8.8	-	2.4		
Output Drive Current (CL/CP Device)	ІОН									mAd
(VOH = 2.5 Vdc) Source	·UH	5.0	-2.5		-2.1	-4.2		-1.7	_	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	_	-0.44	-0.88	_	-0.36		
(VOH = 9.5 Vdc)		10	-1.3		-1.1	-2.25	n enot	-0.9	HTAR S	1,000
(VOH = 13.5 Vdc)		15	-3.6		-3.0	-8.8	The second	-2.4		1
011	1	5.0	0.52		0.44	0.88	- Adultabia	0.36		mA
OL .	OL	400	10.000	2.5-			_	0.701271.53	Viogoti O	mA
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3		1.1	2.25		0.9		
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	of 2-0 -	3.0	8.8	10 (21) 60	2.4	port at Oct	1,340
nput Current (AL Device)	lin	15	- 07	± 0.1	483-jag	±0.00001	± 0.1	mu2-tug	±1.0	μА
nput Current (CL/CP Device)	lin	15	- 00	± 0.3	-	±0.00001	± 0.3	eg "Todare	±1.0	μА
nput Capacitance (V <sub>in</sub> = 0)	Cin	57	087 + 6	as =	-	5.0	7.5	envimon	of Space	pF
Quiescent Current (AL Device)	IDD	5.0		0.25		0.0005	0.25	-	7.5	μΑ
(Per Package)		10	100 - STOR	0.50	nege to	0.0010	0.50	rinty_based	15	R my
0-		15	- 3.8	1.00	ment_Ship	0.0015	1.00	Pleate	30	RUBBY
Quiescent Current (CL/CP Device)	IDD	5.0	O'227 5	1.0	200 57,000	0.0005	1.0	CONTRACT.	7.5	μА
(Per Package)		10	-	2.0		0.0010	2.0		15	-
A-BEA-DRA-DRA-W BE-A		15	-	4.0	-	0.0015	4.0	-	30	
Total Supply Current**†	IT	5.0			1 10	.75 µA/kHz	1641			μА
(Dynamic plus Quiescent,		10								MA
Per Package)	*	15				.50 µA/kHz				
(C <sub>L</sub> = 50 pF on all outputs, all	01	10			T = (2	.25 µA/kHz	מסי + דונ			
buffers switching)	20 1		1 3							

\*Tlow = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

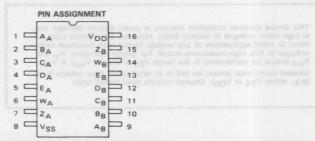
\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: I  $_T$  is in  $\mu A$  (per package), C  $_L$  in pF, V = (V  $_{DD}$  – V  $_{SS}$ ) in volts, f in kHz is input frequency, and k = 0.002.

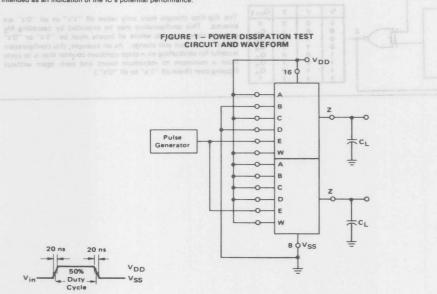




Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH.					ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTHL	5.0	-	100	200	
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns		10	_	50	100	ining.
$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		15	- 1	40	80	
Propagation Delay Time	tPLH	T Contract	2.1	1	F 1	ns
A, C, W = VDD; B, E = Gnd; D = Pulse Generator		0 1 0	81 -	10		
tpLH = (1.7 ns/pF) CL + 290 ns	4-07 A	5.0	0 -	375	960	1
tplH = (0.66 ns/pF) CL + 127 ns		10	1 -	160	400	4
tpLH = (0.5 ns/pF) CL + 85 ns		15		110	300	317
tpHL = (1.7 ns/pF) CL + 345 ns	tPHL	5.0	-	430	1200	ns
tpHL = (0.66 ns/pF) CL + 162 ns		10	-	195	540	
tpHL = (0.5 ns/pF) CL + 95 ns	100 PM T 20 20 20	15	-	120	410	
A, B, C, D, E = Pulse Generator; W = VDD	tPLH			-		ns
tpLH = (1.7 ns/pF) CL + 170 ns		5.0	-	255	640	
tpLH = (0.66 ns/pF) CL + 87 ns		10	-	120	300	-
tpLH = (0.5 ns/pF) CL + 60 ns		15	-	85	210	-
tpHL = (1.7 ns/pF) CL + 195 ns	tPHL	5.0	-	280	750	ns
tpHL = (0.66 ns/pF) CL + 92 ns	A flip-fe	10	Commercial Contraction	125	330	70
tpHL = (0.5 ns/pF) CL + 75 ns	plitago ni	15		100	250	
A, B, C, D, E = Gnd; W = Pulse Generator	tPLH,	10 0				ns
tpHL, tpLH = (1.7 ns/pF) CL + 145 ns	tPHL	5.0		230	575	
tpHL, tpLH = (0.66 ns/pF) CL + 72 ns		10	-	105	265	
tpHL, tpLH = (0.5 ns/pF) CL + 50 ns		15	-	75	190	

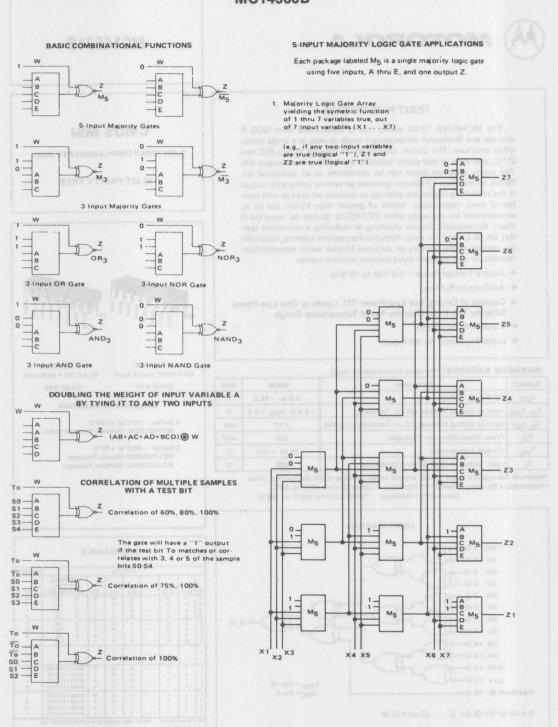
\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



### MC14530B

#### SEQUENTIAL LOGIC APPLICATIONS COINCIDENT FLIP-FLOP W Q<sub>n+1</sub> В 0 0 0 1 0 1 0 0 A flip-flop that will change only when both inputs agree. C D E ASTABLE MULTIVIBRATOR W 0 0 -Q<sub>n+1</sub> A flip-flop with three output conditions, where the third state is C 0 0 in oscillation between "1" and "0". The period of oscillation 2T 2T 1 is twice the delay of the gate and the feedback element. D COINCIDENT FLIP-FLOP The flip-flop changes state only when all "1's" or all "0's" are 0 0 entered. This configuration may be extended by cascading $M_5$ gates to cover n-inputs where all inputs must be "1's" or "0's" before the output will change. As an example, this configuration an an an an an an 0 0 0 1 0 1 1 0 0 1 0 1 0 1 C is useful for controlling an n-stage up/down counter that is to cycle from a minimum to maximum count and back again without flipping over (from all "1's" to all "0's".) 0



### MC14531B

#### 12-BIT PARITY TREE

The MC14531B 12-bit parity tree is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data-bit inputs (D0 thru D11), and even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12-bits can be accommodated by cascading other MC14531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

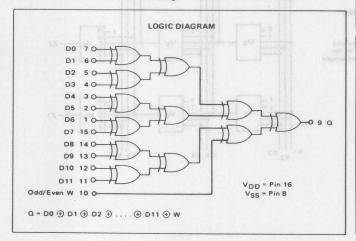
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Variable Word Length
- Diode Protection on All Inputs

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin, lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

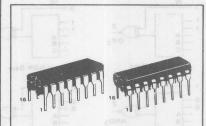
Ceramic "L" Package: -12mW/°C from 100°C to 125°C



### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

12-BIT PARITY TREE



L SUFFIX CERAMIC PACKAGE P SUFFIX
PLASTIC PACKAGE
CASE 648

**CASE 620** 

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### TRUTH TABLE

				INP	JTS				OUTPUT
w	D11	D10	to no	D2	D1	DO	10	CIMAL CTAL) VALENT	a.
0	0	0		0	0	0	0	(0)	0
0	0	0		0	0	1	1	(1)	1
0	0	0		0	1	0	2	(2)	1
0	0	0		0	1	1	3	(3)	0
0	0	0		1	0	0	4	(4)	1
0	0	0		1	0	1	5	(5)	0
0	0	0		1	1	0	6	(6)	0
0	0	0		1	1	1	7	(7)	1
:	:	arios	to n	oranie in	110.0				
1	1	1		0	0	0	8184	(17770)	0
1	1	1		0	0	1	8185	(17771)	1
1	1	1		0	1	0	8186	(17772)	1
1	1	1		0	1	1	8187	(17773)	0
1	1	1		1	0	0	8188	(17774)	1
1	1	1		1	0	1	8189	(17775)	0
1	1	1		- 1	1	0	8190	(17776)	0
1	1	1		1	1	1	8191	(17777)	1

FLECTRICAL CHARACTERISTICS (Voltages Referenced to Voc.)

	ARIM!	VDD	Ti	ow *		25°C		Thi	gh *	-
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	+	0.05	-	0	0.05	DESCRIPTION BY	0.05	Vdc
$V_{in} = V_{DD}$ or 0	0.2	10	1	0.05	-	0	0.05	COLUMN BOX	0.05	20,000
v <sub>in</sub> = v <sub>DD</sub> or o		15	1	0.05		0	0.05	-1-	0.05	274273
"1" Level	VOH	5.0	4.95	1019_	4.95	5.0	_	4.95	TO of	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>		10	9.95	19197	9.95	10	10 - 31	9.95	e inter o	e-Gi
Vin = 0 or VDD		15	14.95	-	14.95	15	5 5 19	14.95	n nation a	100
Input Voltage "0" Level	VIL	the .				- and	10 + 10 (	(0.5 mip	5 13/197 H	Vdc
$(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$	15 155	5.0	-	1.5	-	2.25	1.5	-	1.5	Dieso.
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	1	3.0	-	4.50	3.0	ONAFS. 17	3.0	101
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	-	4.0		6.75	4.0	han 50.01	4.0	Day
"1" Level	VIH	251				£13 ·	15 + 10 1	also 8,0)		295
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$		5.0	3.5	- 1	3.5	2.75	distributions	3.5	nulge of year	Vdc
$(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$		10	7.0	-	7.0	5.50	-	7.0	-	
$(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$		15	11.0	-	11.0	8.25	of trees of	11.0	y/" belied	al hadde
Output Drive Current (AL Device)	10Н		THE STATE OF THE S		,eomis	atched letter	log s'Ol el	I la egitesi	den an ind	mAdo
(VOH = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	
(VOH = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	-
(VOH = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	-	-0.9	-	
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	-	-2.4	_	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	_	0.51	0.88	MUNIOS ST	0.36		mAdo
(V <sub>OL</sub> = 0.5 Vdc)	0.	10	1.6	-	1.3	2.25	MINTO 2 3 1	0.9		
(V <sub>OL</sub> = 1.5 Vdc)	20.10	15	4.2	-	3.4	8.8	-	2.4	- 1	
Output Drive Current (CL/CP Device)	ГОН					111 9		25.EV	DC -my (	mAdo
(VOH = 2.5 Vdc) Source	0	5.0	-2.5	COV.	-2.1	-4.2		-1.7	2000	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	-1/8	-0.36	- 1	
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	-ssV	-1.1	-2.25	29	-0.9	1501 4	35
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	_ locates	-2.4		
(VOI = 0.4 Vdc) Sink	loL	5.0	0.52	-	0.44	0.88	_	0.36	-	mAdo
(VOL = 0.5 Vdc)	00	10	1.3	-	1.1	2.25	_	0.9	40	
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8	Roote must	2.4	1 1 m etc.	
Input Current (AL Device)	1 <sub>in</sub>	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	± 1.0	μAdc
Input Capacitance	Cin	_		-	-	5.0	7.5	-	-	pF
(V <sub>in</sub> = 0)	-in									
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdo
(Per Package)	.00	10	-	10	-	0.010	10	-	300	
		15		20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	<u> </u>	0.005	20	-	150	μAdo
(Per Package)	.00	10		40	_	0.010	40		300	
.,		15	_	80	-	0.015	80	_	600	
Total Supply Current**†	I <sub>T</sub>	5.0		- 00	l= : 10	.25 µA/kHz			000	μAdo
(Dynamic plus Quiescent,		10	S N III			.25 μΑ/κΗ2				I MAGE
Per Package)		15				.75 µA/kHz				
(C <sub>1</sub> - 50 pF on all outputs, all					1 10	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,				1
buffers switching)	100									

 $<sup>^*</sup>T_{low}$  =  $-55^\circ$ C for AL Device,  $-40^\circ$ C for CL/CP Device.  $T_{high}$  =  $+125^\circ$ C for AL Device,  $+85^\circ$ C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I  $_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD - V\_SS) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C. †To calculate total supply current at loads other than 50 pF:

SWITCHING CHARACTERISTICS\* (C1 = 50 pF. TA = 25°C)

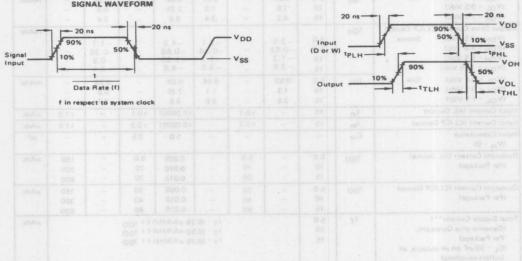
Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH-	M. I shall	Someon	2	Character co	ns
tTLH, tTHL = (1.5 ns/pF) CL + 25 ns	tTHL	5.0		100	200	Salar Barretan
tTLH, tTHL = (0.75 ns/pF) CL + 12.5 ns		10	F JoV	50	100	A STATE OF THE PARTY OF
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	1 80 0	15	- 1	40	80	N S NEW
Propagation Delay Time	tPLH.	N 7.3		Toronto & Prignal		ns
Data to Q	tPHL		1			
tpLH, tpHL = (1.7 ns/pF) CL + 355 ns		5.0	-	440	1320	A 1934
tpLH tpHL = (0.66 ns/pF) CL + 142 ns	251	10	J	175	525	- 10 King
tPLH, tPHL = (0.5 ns/pF) CL + 95 ns		15	11 12 1	120	360	William Indi
Odd/Even to Q	61 4 . 1			Male Class	1007 8 0 10 e	- OW
tPLH, tPHL = (1.7 ns/pF) CL + 165 ns	1 22	5.0	1 - 1	250	750	0.40
tPLH, tPHL = (0.66 ns/pF) CL + 67 ns	1 24 1	10		100	300	E = 0x)
tPLH, tPHL = (0.5 ns/pF) CL + 45 ns		15	1 <u>0</u> 9	70	210	5 -1 -30

\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORM





# MC14532B

#### 8-BIT PRIORITY ENCODER

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input ( $E_{in}$ ) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output ( $E_{out}$ ).

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
VDD	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
Ti	Lead Temperature (8-Second Soldering)	260	°C

"Maximum Ratings are those values beyond which damage to the device may occur †Temperature Derating: Plastic "P" Package: — 12mW/"C from 65°C to 85°C Ceramic "L" Package: — 12mW/"C from 100°C to 125°C

#### TRUTH TABLE

-		No.	1	NPUT		2 100			OUTPUT				
Ein	D7,	D6	D5	D4	D3	D2	D1	DO	GS	02	Q1	00	Eout
0	X	X	×	X	×	X	×	×	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	×	×	×	×	×	×	1	1	1	1	0
1	0	1	×	X	×	X	X	X	1	1	1	0	0
1	0	0	1	×	×	×	×	X	1	1	0	1	0
1	0	0	0	1	×	×	X	×	1	1	0	0	0
1	0	0	0	0	- 1-	×	×	×	1	0	- 11	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	. 1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

8-BIT PRIORITY ENCODER



CERAMIC PACKAGE

CASE 620

P SUFFIX PLASTIC PACKAGE

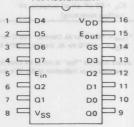
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to Voc)

	12 17 17	VDD	Tic	w*		25°C		Thi	gh *	1
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	- 1	0.05	Vdc
Vin= VDD or 0		10	-	0.05	-	0	0.05	_	0.05	
55		15	-	0.05	-	0	0.05	-	0.05	
Vin = 0 or VDD "1" Level	VOH	5.0	4.95	-	4.95	5.0	_	4 95		Vdc
TIM COLUDD . Sector	· OH	10	9.95	_ 78	9.95	10	T Part	9.95	_	***
EDING DATEMAN		15	14.95		14.95	15	_	14.95		
Input Voltage "0" Level	VIL	- 21	Tel Arrest	SEPTIMINE	Ten Jeriu	barouna	mon al	14.50	DM MC	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	VIL	5.0		1.5		2.25	1.5		1.5	Vac
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10		3.0	STATE OF THE PARTY	4.50	3.0		3.0	
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	W A STATE	4.0	20 (752)	6.75	4.0	17 172 GF	4.0	1110
"1" Level	V	15	-	4.0	10.311	0.75	4.0	MEGG	4.0	-
(VO = 0.5 or 4.5 Vdc)	VIH		1005 916	Spall an	Shieve o	a struction		DIVOTO S		144
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		5.0	3.5	ns ona t	3.5	2.75	10 Eno .	3.5	DOT ziu	Vdc
		10	7.0	-	7.0	5.50	-	7.0	- de	(8)
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	-	11.0		-
Output Drive Current (AL Device)	ЮН					200	n l BA n	and the same		mAdd
(VOH = 2.5 Vdc) Source	10.1	5.0	-3.0	-	-2.4	-4.2	1 32 1 3	-1.7	2000	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88	E = spr	-0.36	V ylqqu	-0-
(VOH = 9.5 Vdc)		10	-1.6		-1.3	-2.25	-	-0.9	_	
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	10 ID 81	-3.4	-8.8	Two Li	-2.4	eldsqu	0
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	DEPT BUT	0.51	0.88	IL FRACE	0.36	ASINTESAND	mAde
(VOL = 0.5 Vdc)		10	1.6	-	1.3	2.25	-	0.9	-	
(VOL = 1.5 Vdc)		15	4.2	-	3.4	8.8	-	2.4	_	
Output Drive Current (CL/CP Device)	ІОН					100				mAde
(VOH = 2.5 Vdc) Source	0.1	5.0	-2.5	_	-2.1	-2.4	_	-1.7		
(VOH = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	_	-0.36	_	-
(VOH = 9.5 Vdc)		10	-1.3	_	-1.1	-2.25	a destruction	-0.9	TAR RE	BEST
(VOH = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	Authority	-2.4	-	1000
(VOI = 0.4 Vdc) Sink	loL	5.0	0.52		0.44	0.88	demana.	0.36		mAdo
(VOL = 0.5 Vdc)	.OL	10	1.3	0-1	1.1	2.25	_	0.9	qquB Do	TO A
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	2.0-2	3.0	8.8	36 <del>-</del> 868	2:4	to the same	
Input Current (AL Device)	1.	15	-	±0.1	0.0	±0.00001	±0.1	-		μAdo
	lin				-		ALTERNATION.		± 1.0	10000
Input Current (CL/CP Device)	lin	15	- 006	± 0.3	-	±0.00001	± 0.3	-	± 1.0	μAdd
Input Capacitance (V <sub>in</sub> = 0)	Cin	9-	187 + 01	10 -	-	5.0	7.5	uns expens	T egstoff	pF
Quiescent Current (AL Device)	IDD	5.0		5.0		0.005	5.0	2 -2 194	150	μAdd
(Per Package)	00	10	to reduce	10	o seeme	0.010	10	ov emocilia	300	i krymu
		15	-Ones	20	00 25W	0.015	20	MI - 9 10	600	denage
Quiescent Current (CL/CP Device)	IDD	5.0	DEST OF	20	1 1/2 1/2/20	0.005	20	10.22	150	μAdo
(Per Package)	.00	10	-	40		0.010	40		300	μΑσσ
		15		80	1 3	0.015	80		600	
Total Supply Current**†	IT	5.0	1079 13	1 00				AJ STORY	600	1
(Dynamic plus Quiescent,	'T	10	0 10		T = (1	.74 µA/kHz	TH DD	ad 1 ag		μAdd
Per Package)			120			.65 µA/kHz				-13
(CL = 50 pF on all outputs, all buffers switching)		15	1 6		T = (5	.73 μA/kHz	, , , , DD	0 0		6

<sup>\*</sup>Tlow = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

g (= 02 2 (= 01 0 (= v<sub>SS</sub>

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance. \*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: IT is in  $\mu$ A (per package), CL in pF, V = (VDD – VSS) in volts, f in kHz is input frequency, and k = 0.005.

SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH,					ns
$t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$	THL	5.0	-	100	200	
$t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		10	-	50	100	
$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	. 1	15	-	40	80	
Progagation Delay Time - Ein to Eout	tPLH,					ns
tPLH, tPHL = (1.7 ns/pF) CL + 120 ns	tPHL	5.0	1 seconds	205	410	
tpLH, tpHL = (0.66 ns/pF) CL + 77 ns	0-10 0	10	- 6015	110	220	
tpLH, tpHL = (0.5 ns/pF) CL + 55 ns	A A	15	100000	80	160	
Propagation Delay Time ( Ein to GS	tPLH,	1 0				ns
tPLH, tPHL = (1.7 ns/pF) CL + 90 ns	tPHL 1	5.0	44 -	175	350	
tPLH, tPHL = (0.66 ns/pF) CL 57 ns	and a	10	-	90	180	
tpLH, tpHL - (0.5 ns/pF) CL + 40 ns	0	15	L	65	130	
Propagation Delay Time - Ein to Qn	tPHL.					ns
tPLH, tPHL = (1.7 ns/pF) CL + 195 ns	tPLH	5.0	-	280	560	1138
tPLH, tPHL = (0.66 ns/pF) CL + 107 ns		10	-	140	280	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns		15	10 -	100	200	
Propagation Delay Time - D <sub>n</sub> to Q <sub>n</sub>	tPLH,		Toronto and		January D.1	ns
tPLH, tPHL = (1.7 ns/pF) CL + 265 ns	tPHL	5.0	-	300	600	M.Sha Sha
tPLH, tPHL = (0.66 ns/pF) CL + 137 ns		10	Marine Sanda	170	340	ro
tpLH, tpHL = (0.5 ns/pF) CL + 85 ns		15	-	110	220	
Propagation Delay Time - Dn to GS	tPLH,	National Control		1	1	so ns
tpLH, tpHL = (1.7 ns/pF) CL + 195 ns	tPHL	5.0	-	280	560	
tPLH, tPHL = (0.66 ns/pF) CL + 107 ns	wos A	10	-	140	280	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns	No.	15		100	200	100

\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL SINK AND SOURCE CURRENT CHARACTERISTICS

0

0

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0

0

X

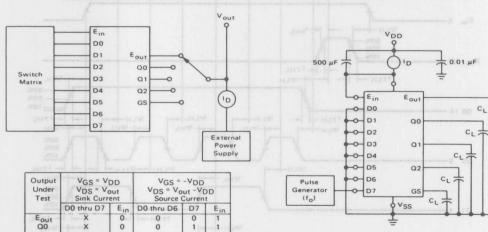
X

Q1

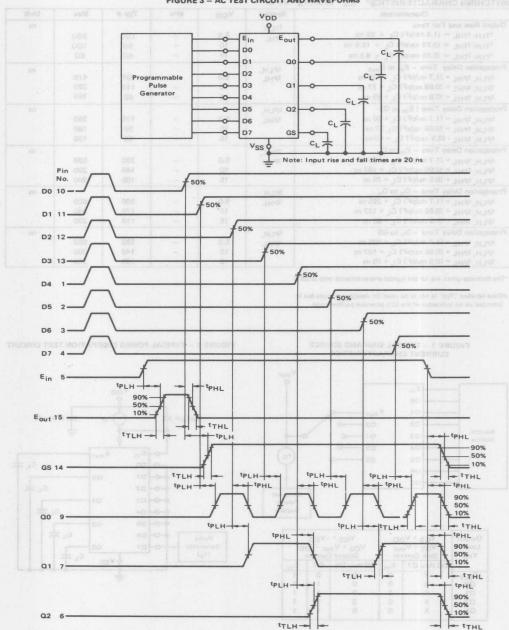
02

GS

FIGURE 2 - TYPICAL POWER DISSIPATION TEST CIRCUIT







### MC14532B

# (Positive Logic)

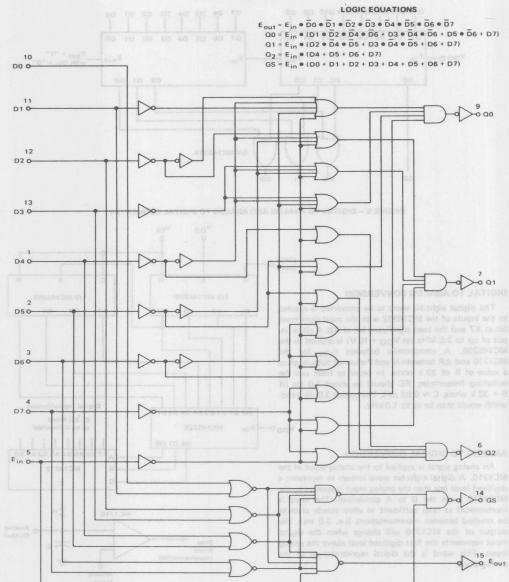


FIGURE 4 - TWO MC14532B's CASCADED FOR 4-BIT OUTPUT

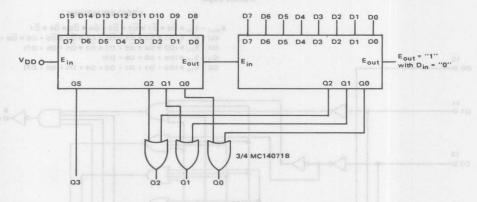


FIGURE 5 - DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTER

VDD

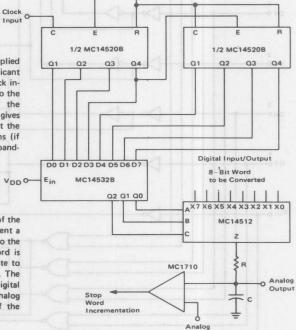
Ves



The digital eight-bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at  $V_{DD}$  = 10 V) is applied to the MC14520B. A compromise between  $I_{Dias}$  for the MC1710 and  $\Delta R$  between N and P-channel outputs gives a value of R of 33 k ohms. In order to filter out the switching frequencies, RC should be about 1.0 ms (if R = 33 k ohms,  $C\approx0.03~\mu F$ ). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

### ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight-bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.



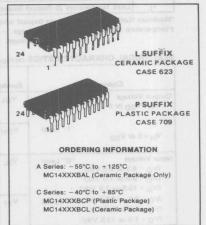
Input



### **CMOS LSI**

(LOW-POWER COMPLEMENTARY MOS)

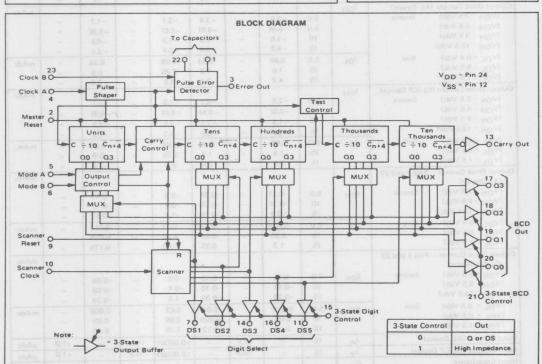
**5 CASCADED BCD COUNTERS** 



#### 5 CASCADED BCD COUNTERS

The MC14534B is composed of five BCD ripple counters that have their respective outputs multiplexed using an internal scanner. Outputs of each counter are selected by the scanner and appear on four (BCD) pins. Selection is indicated by a logic high on the appropriate digit select pin. Both BCD and digit select outputs have three-state controls providing an "open-circuit" when these controls are high and allowing multiplexing. Cascading may be accomplished by using the carry-out pin. The counters and scanner can be independently reset by applying a high to the counter master reset (MR) and the scanner reset (SR). The MC14534B was specifically designed for application in real time or event counters where continual updating and multiplexed displays are used.

- Four Operating Modes (See truth table)
- Input Error Detection Circuit
- Clock Conditioning Circuits for Slow Transition Inputs
- Counter Sequences on Positive Transition of Clock A
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



#### MAXIMUM RATINGS (Voltages referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin, lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precauvoltages of electric liefds. Nowever, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range Vss < (Vin or Val) < Vos  $V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

#### ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	TI	ow*	HT (H2)	25°C		Th	Thigh*	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	_	0.05	-	0	0.05	-	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	0.	10	-	0.05	-	0	0.05		0.05	
MARK DITER IT SHEET FACE	188 F 1	15		0.05	(800	0	0.05	N-BUCKERO	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	ac goal	4.95	St PROMI	Vdc
Vin=0 or VDD	*OH	10	9.95	non-hadi	9.95	10 21	HOT-1 or	9.95	Clasic C	100
uncertain bladtenic		15	14.95		14.95	15		14.95	enter-AT	
Input Voltage "0" Level	VIL	D 19		II. M301. 2	1		111111111111111111111111111111111111111			Vdc
(VO = 4.5 or 0.5 Vdc)	VIL	5.0		1.0	20 A 81	1.5	1.0	9.00000	1.0	1
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	control in	2.0	151 4TT	3.0	2.0	PSY 16 TO	2.0	(S)
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	-	3.0	user-uni	4.5	3.0	negu-im	3.0	No.
(VO = 0.5 or 4.5 Vdc) "1" Level	VIH	5.0	4.0	_	4.0	3.5	_	4.0	_	Vdc
(VO = 1.0 or 9.0 Vdc)	1111	10	8.0	1000	8.0	7.0		8.0		1
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	12	_	12	11	_	12	-	
Output Drive Current (AL Device)	ІОН				-					mAdo
(VOH 2.5 Vdc) Source	HO	5.0	-3.0	-	-2.4	-3.1		-1.7	_	11100
(VOH 4.6 Vdc)		5.0	-0.64	SOJS.	-0.51	-0.67		-0.36		
(VOH 9.5 Vdc)		10	-1.6		-0.5	-1.3		-0.9		1
(VOH = 13.5 Vdc)		15	-4.2	-	-3.4	-5.4	142	-2.4		
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64		0.51	0.88	_	0.36	_	mAde
(VOI = 0.5 Vdc)	,OL	10	1.6		1.3	2.25		0.9	203	
(VOI = 1.5 Vdc)		15	4.2	_ 5	3.4	8.8		2.4		(India)
Output Drive Current (CL/CP Device)	1		7.2		10101	0.0		2.7	CE CE	mAde
(VOH = 2.5 Vdc) Source	ІОН	5.0	-2.5		-2.1	-3.0		-1.7		mAdd
(VOH = 4.6 Vdc)		5.0	-0.52	Silver - Talebase	-0.44	-0.64		-0.36	10	1
(VOH = 9.5 Vdc)		10	-1.3		-1.1	-1.6		-0.9		thought south
(VOH = 13.5 Vdc)	NEW YORK	15	-3.6	7	-3.0	-5.3	TE I	-2.4		
(V <sub>OI</sub> = 0.4 Vdc) Sink	1.	5.0	0.52		0.44	-		-	01-6	1
(VOL = 0.5 Vdc)	OL	10	1.3		1.1	0.88	no FT	0.36		mAdd
(V <sub>OL</sub> = 1.5 Vdc)	913	15	3.6		3.0	8.8	med la	2.4	-	
Output Drive Current - Pins 1 and 22		- 13	3.0		3.0	0.0	4	2.4	1	1
(AL Device)	Ruth Jo-	1-1-1		Les Tool	X UNA			Towns		mAde
(VOH = 2.5 Vdc) Source	Іон	5.0	-0.31		-0.25	-0.8		-0.17		
(VOH = 9.5 Vdc)	1 OH	10	-0.31		-0.25	-0.4		-0.17		
(VOH = 13.5 Vdc)	1111 7	15	-0.9		-0.75	-1.6		-0.51	MAG (A)	
(VOI = 0.4 Vdc) Sink	la	5.0	0.024	-	0.02	0.03		0.014		
(VOL = 0.5 Vdc)	OL	10	0.024		0.02	0.09		0.014	-	mAdd
(V <sub>OL</sub> = 1.5 Vdc)		15	1.3		0.25	1.63		0.175		20,07
Output Drive Current - Pins 1 and 22					0.20	1.00		0.170		
(CL/CP Device)					5					mAdd
(V <sub>OH</sub> = 2.5 Vdc) Source	ІОН	5.0	-0.11	1	-0.10	-0.8	-	-0.08		10013
(V <sub>OH</sub> = 9.5 Vdc)	'OH	10	-0.11		-0.10	-0.4	are.	-0.08		1 = 1
(V <sub>OH</sub> = 13.5 Vdc)		15	-0.33		-0.10	-1.6		-0.08	PIZ IN	1-100
(VOL = 0.4 Vdc) Sink	la.	5.0		202 4		0.02		-		-
(VOL = 0.5 Vdc)	OL	10	0.012	E.V.	0.01	0.02		0.008	-	mAdd
(VOL = 1.5 Vdc)	mainte	15	0.03	031	0.025	1.35	-	0.02	-	
Input Current (AL Device)		-	0.14	-0.1	0.12		-		bTbM.	-
	lin	15		±0.1	-	±0.00001	•0.1		±1.0	μAdo
Input Current (CL/CP Device)	lin	15	-	±0.3	-	±0.00001	±0.3	- 1	± 1.0	μAdo
Input Capacitance	Cin		_	-	-	5.0	7.5	_		DF

\*T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>) (continued)

		VDD	T	ow*		25°C		T	nigh "	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Quiescent Current (AL Device)	IDD	5.0	- 1	5.0	-	0.010	5.0	1000	150	μAdc
(Per Package)	00	10	0.5-	10	-	0.020	10	-	300	
		15	01_	20	-	0.030	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0		50		0.010	50	_	375	μAdc
(Per Package)		10	-	100	-	0.020	100	200	750	000019
		15		200	-	0.030	200	-	1500	Chool
Total Supply Current**†	I <sub>T</sub>	5.0	151	IT	= (0.5 µ	A/kHz) f + I	00	or graphier de.	77 515 4	μAdc
(Dynamic plus Quiescent,		10				A/kHz) f + I		Scan O	scillator	1
Per Package)		15				A/kHz) f + I		Frequenc	y = 1 kHz	
(C <sub>L</sub> = 50 pF on all outputs, all buffers switching)			9.0	47.54			4 = D.	8+ 10 FR	en birj = j	191
Three-State Leakage Current (AL Device)	ITL	15	B.	± 0.1		0.00001	± 0.1	D- 12 (9)	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	ITL	15	0.6. Or	±1.0		•0.00001	± 1.0	(F) (Q) (F)	± 7.5	μAdc

*Tlow = -55°C for AL Device,	- 40°C for CL/CP Device.
------------------------------	--------------------------

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_{\mbox{\scriptsize T}}$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (VDD-VSS) in volts, f in kHz is input frequency, and k = 0.001.

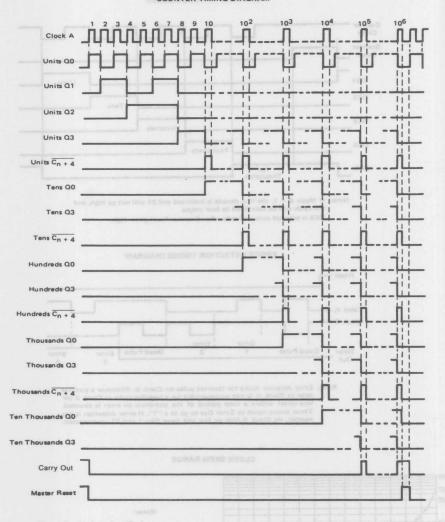
| Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part | Part |

SWITCHING CHARACTERISTICS\* (C<sub>1</sub> = 50 pF, T<sub>A</sub> = 25°C, See Figure 1)

Characteristic Characteristic	Symbol	V <sub>DD</sub> Vdc	Min.	Тур#	Max	Unit
Output Rise and Fall Time	t <sub>TLH</sub> , t <sub>THL</sub>	5.0 10 15	91 - 001	100 50 40	200 100 80	ns ins
Propagation Delay Time,	tPLH,	-	OF US			μS
tpLH, tpHL = (1.8 ns/pF) C <sub>L</sub> + 4.0 μs tpLH, tpHL = (0.8 ns/pF) C <sub>L</sub> + 1.5 μs tpLH, tpHL = (0.6 ns/pF) C <sub>L</sub> + 1.0 μs	20) = pt	5.0 10 15	0.8 YI	4.0 1.5 1.0	8.0 3.0 2.25	apply Cu
Clock to Carry Out tpLH = (1.8 ns/pF) CL+3.3 μs	tPLH	5.0	81.	3.3	6.6	μs
tp <sub>LH</sub> = (0.8 ns/pF) C <sub>L</sub> + 1.1 μs tp <sub>LH</sub> = (0.6 ns/pF) C <sub>L</sub> + 0.8 μs	I rest	10 15	37 - 141	1.1 0.8	2.2 1.7	ofina enti- us I obci
Master Reset to Q tpHL = (1.8 ns/pF) · CL + 1.8 μs	†PHL	5.0		1.8	3.6	μs
tpHL = (0.8 ns/pF) CL + 0.6 µs tpHL = (0.6 ns/pF) CL + 0.5 µs		10 15	= -	0.6 0.5	1.2 0.9	eved 50
Master Reset to Error Out  tpHL = (1.8 ns/pF) C <sub>L</sub> +0.57 μs  tpHL = (0.8 ns/pF) C <sub>L</sub> +0.19 μs	<sup>t</sup> PHL	5.0 10	SOLVED.	0.6 0.2	1.5 .5	μs
tpHL = (0.6 ns/pF) C <sub>L</sub> + 0.11 μs	A tij e ekteretio	15	Little action and	0.12	0.38	olied "Tyr
Scanner Clock to Q  tp_H, tpH_ = (1.8 ns/pF) C_L + 1.8 µs  tp_H, tpHL = (0.8 ns/pF) C_L + 0.6 µs  tp_H, tpHL = (0.6 ns/pF) C_L + 0.5 µs	tPLH, tPHL	5.0 10 15	TS to you early	1.8 0.6 0.5	3.6 1.2 0.9	μS
Scanner Clock to Digit Select  tpHL, tpLH = (1.8 ns/pF) C <sub>L</sub> + 1.5 µs  tpHL, tpLH = (0.8 ns/pF) C <sub>L</sub> + 0.5 µs  tpHL, tpLH = (0.6 ns/pF) C <sub>L</sub> + 0.4 µs	<sup>†</sup> PLH, <sup>†</sup> PLH	5.0 10 15	=	1.5 0.5 0.4	3.0 1.0 0.75	μs
Propagation Delay Time 3-State Control to Q	<sup>†</sup> PHZ	5.0 10 15	Ξ	75 45 40	150 90 80	ns
	<sup>t</sup> PZH	5.0 10 15	Ξ	120 55 40	240 110 80	ns
	tPLZ	5.0 10 15	Ξ	120 55 45	240 110 90	ns
	tPZL	5.0 10 15	=	160 70 45	320 140 90	ns
Clock Pulse Frequency	fcI	5.0 10 15	=	1.0 3.0 5.0	0.5 1.0 1.2	MH
Clock or Scanner Clock Pulse Width	tWH	5.0 10 15	1000 500 375	500 190 125		ns
Scanner Reset Pulse Width	t <sub>w</sub>	5.0 10 15	320 130 80	160 65 40	Ξ	ns
Scanner Reset Removal Time	<sup>t</sup> rem	5.0 10 15	900 150 100	270 80 50	Ξ	ns
Master Reset Pulse Width	tWH(R)	5.0 10 15	2000 600 450	900 300 250	=	ns
Master Reset Removal Time	t <sub>rem</sub>	5.0 10 15	1060 350 250	550 205 140	Ξ	ns

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C. #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

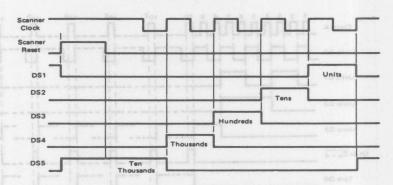
#### COUNTER TIMING DIAGRAM



### MODE CONTROL TRUTH TABLE

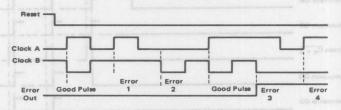
Mode A	Mode B	First Stage Output	Carry to Second Stage	Application
0	0	Normal Count and Display	At 9 to 0 transition of first stage	5-digit Counter
0	of graft says	Inhibited	Input Clock	Test Mode: Clock directly into stages 1, 2, and 4
1	1	Inhibited	At 4 to 5 transition of first stage	4-digit counter with ÷ 10 and roundoff at front end
1	0	Counts 3, 4, 5, 6, 7 = 5 Counts 8, 9, 0, 1, 2 = 0	At 7 to 8 transition of first stage	4-digit counter with 1/2 pence capability.

#### SCANNER TIMING DIAGRAM



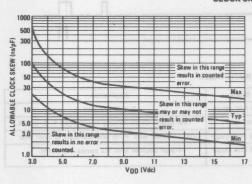
Note: If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages. DS5 is selected automatically when Scanner Reset goes high.

#### **ERROR DETECTION TIMING DIAGRAM**



Note: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-versa) within a time period of the one-shots an error is counted. Three errors result in Error Out to go to a "1". If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.

#### **CLOCK SKEW RANGE**



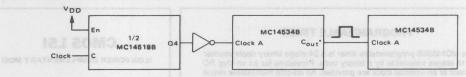
### Notes:

- 1. The skew is the time difference between the low-to-high transition of C<sub>A</sub> to the high-to-low transition of C<sub>B</sub> or vice-verse. Capacitors C1 = C22 tied from pins 1 and 22 to V<sub>SS</sub>.

  2. This graph is accurate for C1 = C22 ≥ 100 pF.
- 3. When the error detection circuitry is not used, pins 1 and 22 are left open.

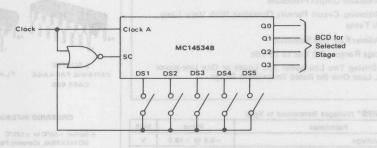
#### APPLICATIONS INFORMATION

#### FIGURE 1 - CASCADE OPERATION



\*Carry Out is high for a single clock period when all five BCD stages go to zero. (Carry Out also goes high when MR is applied.)

#### FIGURE 2 — FORCING A BCD STAGE TO THE Q OUTPUTS



When the Q outputs of a given stage are required, this configuration will lock up the selected stage within four clock cycles. The select line feedback may be hardwired or switched.

#### PIN ASSIGNMENT



### MC14536B

#### PROGRAMMABLE TIMER

The MC14536B programmable timer is a 24-stage binary ripple counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has been included. By selecting the appropriate counter stage in conjunction with the appropriate input clock frequency, a variety of timing can be achieved.

- 24 Flip-Flop Stages -- Will Count From 20 to 224
- Last 16 Stages Selectable By Four-Bit Select Code
- 8-Bypass Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit and Oscillator Inhibit Inputs
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

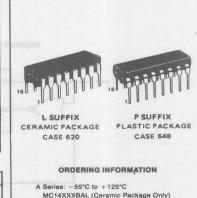
Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin. lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: – 12mW/°C from 65°C to 85°C. Ceramic "L" Package: – 12mW/°C from 100°C to 125°C

### **CMOS LSI**

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE TIMER



C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

**BLOCK DIAGRAM** Clock Inh Reset Set 8-Bypass Osc. Inhibit 14 0 Stages 9 thru 24 Stages Q Q Q 0 0 Q 1 thru 8 A 90 Out 1 Out 2 В 100 Decoder C 110-D 120 VDD = Pin 16 VSS = Pin 8 -0 13 Decode Monostable Mono-In 15 0-

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		V <sub>DD</sub> T <sub>low</sub> * 25°C				Thigh *			-		
Character	istic	Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage	"O" Level	VOL	5.0	12.0	0.05	-	0	0.05	fuelies e	0.05	Vdd
Vin = VDD or O		- 02	10	-	0.05	-	0	0.05	riquan evi	0.05	SHIP
"" 00			15	-	0.05	-	0	0.05	70/20 80.	0.05	HIT
	"1" Level	VOH	5.0	4.95	349	4.95	5.0	-	4.95	Majett n	Vdd
Vin = O or VDD		On	10	9.95	(0)	9.95	10	IBIH III	9.95	B-8 _ CD	M XOO
III DO		- 1	15	14.95	_	14.95	15	1000	14.95	D = 489	31,197
9063	0300		- 07		-			101 10	39km 311	2159	
Input Voltage	"O" Level	VIL	81				200	000 + y	(Sqlan it	N. W. JING	Vdd
$(V_0 = 4.5 \text{ or } 0.5)$			5.0	- 54	1.5	_	2.25	1.5	Local man	1.5	no scot
$(V_0 = 9.0 \text{ or } 1.0)$		-	10	1- 7	3.0	_	4.50	3.0	13glan V	3.0	10 197
$(V_0 = 13.5 \text{ or } 1.$		-	15	-	4.0	_	6.75	4.0	Salan SS	4.0	
	"1" Level	-VIH			5-11		10.7		(Figlian 8.	DE # 1120	Vdd
$(V_0 = 0.5 \text{ or } 4.5)$	Vdc)		5.0	3.5	100	3.5	2.75	-	3.5	3rp	or about
$(V_0 = 1.0 \text{ or } 9.0)$	Vdc)	-	10	7.0	-	7.0	5.50	1007	7.0	1	hege
$(V_0 = 1.5 \text{ or } 13.$	5 Vdc)		15	11.0	- 1	11.0	8.25	80 F 30	11.0	N - Time	f-Safada
Output Drive Curren	t (Al Device)	-lau	15				201.78	110 4 2	(Fatan d	N TO VE	mAd
(V <sub>OH</sub> = 2.5 Vdc)	Source	ПОН	5.0	-1.2	-	-1.0	-1.7	-	-0.7	2397.0	IIIAO
$(V_{OH} = 4.6 \text{ Vdc})$	Pins 4 & 5		5.0	-0.25	130	-0.2	-0.36	-	-0.14	1967	1 1000
$(V_{OH} = 9.5 \text{ Vdc})$			10	-0.62		-0.5	-0.9	an car	-0.14		THAI
(V <sub>OH</sub> = 13.5 Vd			15	-1.8	_	-1.5	-3.5	APP ARE	-1.1		PHL
		100	92.7	-	-	-	-	W 41		100 0.00	1000
$(V_{OH} = 2.5 \text{ Vdc})$	Source	308	5.0	-3.0	100 - 1	-2.4	-4.2	-	-1.7	DE-14 0	mAd
$(V_{OH} = 4.6 \text{ Vdc})$	Pin 13	200	5.0	-0.64	-	-0.51	-0.88		-0.36	-	
$(V_{OH} = 9.5 \text{ Vdc})$		170	1.0	-1.6	_	-1.3	-2.25	-	-0.9		
$(V_{OH} = 13.5 \text{ Vdc})$			15	-4.2	1 -	-3.4	-8.8	_	-2.4	export 7 a	ER Put
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.64	-	0.51	0.88	_	0.36	baya van	mAd
$(V_{OL} = 0.5 \text{ Vdc})$			10	1.6	-	1.3	2.25	_	0.9	-	. 111
$(V_{OL} = 1.5 \text{ Vdc})$			15	4.2	777-	3.4	8.8	_	2.4	Dall-Ans	diff da
Output Drive Curren	Alterial digit	la.		.37	72						
(CL/CP Device)		Іон	92								mAd
(V <sub>OH</sub> = 2.5 Vdc)	Source	0007	5.0	-1.0	102 _	-0.8	-1.7	_	-0.6	data Wife	Das tur
(V <sub>OH</sub> = 4.6 Vdc)	Pins 4 & 5	335	5.0	-0.2	_	-0.16	-0.36	_	-0.12	_	
(V <sub>OH</sub> = 9.5 Vdc)		DEE	10	-0.5	_	-0.4	-0.9		-0.3	_	
(VOH = 13.5 Vds	5)		15	-1.4	- 57	-1.2	-3.5	arto <del>- c</del> ato	-1.0	710.00 aug	ethod 6
				-	-	-		191 SOUR	-	tier bin	100 540
$(V_{OH} = 2.5 \text{ Vdc})$	Source		5.0	-2.5	-	-2.1	-4.2	eron altil	-1.7	Morri Ton as	mAd
$(V_{OH} = 4.6 \text{ Vdc})$	Pin 13		5.0	-0.52	_	-0.44	-0.88		-0.36	-	
$(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$			10 15	-1.3 -3.6	-	-1.1	-2.25 -8.8		-0.9	_	
The state of the s	F 1 1 1		15	-3.0	_	-3.0	-0.0		-2.4		
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	IOL	5.0	0.52	-	0.44	0.88	00204	0.36	no activi	mAd
$(V_{OL} = 0.5 \text{ Vdc})$			10	1.3	_	1.1	2.25	Q7_Bub	0.9	led[sps	10.68.01
$(V_{OL} = 1.5 \text{ Vdc})$			15	3.6	-	3.0	8.8	THE PARTY	2.4	0.00 70 0	garay
Input Current	m r	1.	15		±0.1	169	ter ± tur	±0.1	self Jorde	±1.0	μAd
(AL Device)		lin	10		10.1	3. 383	0.00001	10.1	ami-dola	11.0	μΑσ
appased in this t				-		-	±	1	- W.	-	-
Input Current		lin	15	-	±0.3	- 10	0.00001	±0.3	Uner-renu	±1.0	μAd
(CL/CP Device)	-1.4						0.00001			-day n	Stard 9
Input Capacitance		Cin	_	-	_	- 19	5.0	7.5	SOUR BEAUT	SQUARE .	pF
$(V_{in} = 0)$			14.			8	A THEOTHER		elizatio	propol as	The second
Quiescent Current (/	Al Device)	la-	5.0		E O		0.010	EO	DESCRIPTION OF	150	
(Per Package)	AL DEVICE/	IDD	10		5.0	-	0.010	5.0		150	μAd
, or rackage,			15		20		0.020	20		600	
Ouissant Course to	CL/CR Desires									-	
Quiescent Current (C	L/CP Device)	DD	5.0	_	50	-	0.010	50	-	375	μAd
(Per Package)			10	-	100	-	0.020	100	-	750	
			15	-	200		0.030	200	_	1500	
Total Supply Current		IT	5.0			$I_{T} = (1.$	15 μA/kH	z) f + 1D	D		μAd
(Dynamic plus Qui	escent,		10	100		$I_T = (2.$	3 μA/kH:	z) f + 1D	D		
Per Package)			15			$I_T = (3.$	55 μA/kH	z) f + 1D	D		
	l outputs,										

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.003.

 $<sup>^{*}</sup>T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

Characteristic	3-88		Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time (Pin 13) tTLH, tTHL = (1.5 ns/pF) CL + tTLH, tTHL = (0.75 ns/pF) CL tTLH, tTHL = (0.55 ns/pF) CL	t <sub>TLH</sub> , t <sub>THL</sub>	5.0 10 15	odenya. _goVlas	100 50 40	200 100 80	ns incomes		
Propagation Delay Time Clock to Q1, 8-Bypass (Pin 6) the tpLH, tpHL = (1.7 ns/pF) CL + tpLH, tpHL = (0.66 ns/pF) CL + tpLH, tpHL = (0.5 ns/pF) CL +	tPLH, tPHL	5.0 10 15	80 <sup>V</sup> = 50	1800 650 450	3600 1300 1000	ns re <sup>V</sup>		
Clock to O1, 8-Bypess (Pin 6) Low tpLH, tpHL = (1.7 ns/pF) CL + 3715 ns tpLH, tpHL = (0.66 ns/pF) CL + 1467 ns tpLH, tpHL = (0.5 ns/pF) CL + 1075 ns			tPLH,	5.0 10 15		3.8 1.5 1.1	7.6 3.0 2.3	μs
Clock to Q16  tpHL, tpLH = (1.7 ns/pF) CL + tpHL, tpLH = (0.66 ns/pF) CL + tpHL, tpLH = (0.5 ns/pF) CL +		tPLH, tPHL	5.0 10 15	-	7.0 3.0 2.2	14 6.0 4.5	μѕ	
Reset to Q <sub>n</sub> tpHL = (1.7 ns/pF) C <sub>L</sub> + 1415 r tpHL = (0.66 ns/pF) C <sub>L</sub> + 567 r tpHL = (0.5 ns/pF) C <sub>L</sub> + 425 ns	80.0- 15 0.0-		tPHL SAO	5.0 10 15	- 8	1500 600 450	3000 1200 900	ns
Clock Pulse Width	-4.2 -0.65 -3.25	-2.4 -0.61 -1.3	tWH	5.0 10 15	600 200 170	300 100 85		ns
Clock Pulse Frequency (50% Duty Cycle)			fcl	5.0 10 15	30 <sup>2</sup> = str	1.2 3.0 5.0	0.4 1.5 2.0	MHz
Clock Rise and Fall Time	9.8	I NE	tTLH, tTHL	5.0 10 15	HQ	No Limit	laby 8,1 × laby 8,1 × laby 8,1 ×	NoteG
Reset Pulse Width	85.0-	8.0- 91.0-	tWH	5.0 10 15	1000 400 300	500 200 150	SOVER -	ns

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C. #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\text{in}}$  and  $V_{\text{out}}$  should be constrained to the range  $V_{\text{SS}} \leqslant (V_{\text{in}} \text{ or } V_{\text{out}}) \leqslant V_{\text{DD}}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



#### PIN DESCRIPTIONS

#### INPUTS

**SET (Pin 1)** — A high on Set asynchronously forces Decode Out to a high level. This is accomplished by setting an output conditioning latch to a high level while at the same time resetting the 24 flip-flop stages. After Set goes low (inactive), the occurrence of the first negative clock transition on IN<sub>1</sub> causes Decode Out to go low. The counter's flip-flop stages begin counting on the second negative clock transition of IN<sub>1</sub>. When Set is high, the on-chip RC oscillator is disabled. This allows for very low-power standby operation.

RESET (Pin 2) — A high on Reset asynchronously forces Decode Out to a low level; all 24 flip-flop stages are also reset to a low level. Like the Set input, Reset disables the on-chip RC oscillator for standby operation.

IN<sub>1</sub> (Pin 3) — The device's internal counters advance on the negative-going edge of this input. IN<sub>1</sub> may be used as an external clock input or used in conjunction with OUT<sub>1</sub> and OUT<sub>2</sub> to form an RC oscillator. When an external clock is used, both OUT<sub>1</sub> and OUT<sub>2</sub> may be left unconnected or used to drive 1 LSTTL or several CMOS loads.

8-BYPASS (PIn 6) — A high on this input causes the first 8 flip-flop stages to be bypassed. This device essentially becomes a 16-stage counter with all 16 stages selectable. Selection is accomplished by the A, B, C, and D inputs. (See the truth tables.)

CLOCK INHIBIT (PIn 7) — A high on this input disconnects the first counter stage from the clocking source. This holds the present count and inhibits further counting. However, the clocking source may continue to run. Therefore, when Clock Inhibit is brought low, no oscillator start-up time is required. When Clock Inhibit is low, the counter will start counting on the occurrence of the first negative edge of the clocking source at IN<sub>1</sub>.

OSC INHIBIT (Pin 14) — A high level on this pin stops the RC oscillator which allows for very low-power

standby operation. May also be used, in conjunction with an external clock, with essentially the same results as the Clock Inhibit input.

MONO-IN (Pin 15) — Used as the timing pin for the on-chip monostable multivibrator. If the Mono-In input is connected to VSS, the monstable circuit is disabled, and Decode Out is directly connected to the selected O output. The monostable circuit is enabled if a resistor is connected between Mono-In and VDD. This resistor and the device's internal capacitance will determine the minimum output pulse widths. With the addition of an external capacitor to VSS, the pulse width range may be extended. For reliable operation the resistor value should be limited to the range of 5 kΩ to 100 kΩ and the capacitor value should be limited to a maximum of 1000 pf. (See figures 3, 4, 5, and 10).

A, B, C, D (Pins 9, 10, 11, 12) — These inputs select the flip-flop stage to be connected to Decode Out. (See the truth tables.)

#### OUTPUTS

OUT<sub>1</sub>, OUT<sub>2</sub> (Pin 4, 5) — Outputs used in conjunction with IN<sub>1</sub> to form an RC oscillator. These outputs are buffered and may be used for 2<sup>0</sup> frequency division of an external clock.

DECODE OUT (Pin 13) — Output function depends on configuration. When the monostable circuit is disabled, this output is a 50% duty cycle square wave during free run.

#### **TEST MODE**

The test mode configuration divides the 24 flip-flop stages into three 8-stage sections to facilitate a fast test sequence. The test mode is enabled when 8-Bypass, Set and Reset are at a high level. (See Figure 8.)



### TRUTH TABLES VIRT Solution May also be used, in conjunction with an outernal clock, with essentially the same results

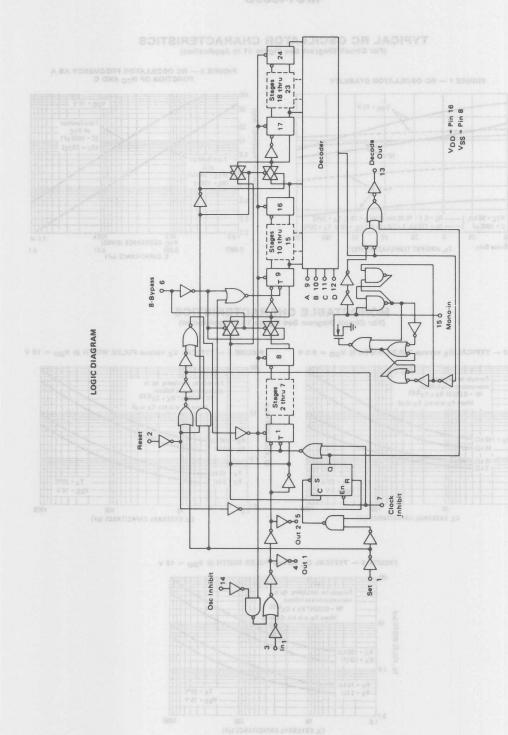
rila pnimit	Input	Stage Selected			
8-Bypass	D	С	В	A	For Decode Out
0	0	0	0	0	9
0 447	0	0	0	1	10
0	0	0	1	0	11
0.00	0	0	1	1	of 1010 12 10 lan
0	0	1	0	0	13
0	0	1	0	1	arta autis <b>14</b> atlusa
0	0	1	1	0	15
0	0	1	51	1	16
0	1	0	0	0	17
0	1	0	0	1	18
0	1	0	1	0	19
0	1	0	1	1	20
0	1	1	0	0	21
0	1.1	1	0	.1	22
10000	dalgo	1	1	0	23
0	1	1	1	1	24

day layer, d	Input	Stage Selected			
8-Bypass	D	С	В	A	For Decode Out
ect to ani	0	0	0	0	ion dili a'tainuos
al Alg up	0	0	0	1	2
1	0	0	1	0	3
adlijonje:	0	0	1	1	ess med THEE
1	0	1	0	0	5
rieq <b>ı</b> ydbr	0	13	0	1	grido-no 6 m kelo
1	0	1	1	0	7
sujeto ni	0	1	11	1	leaveled 8 a 86
1	1	0	0	0	9
G lateves	1	0	0	010	10
1	1	0	1	0	11
one1s and	1	0	10	1	12 011
1 18.0	1	1	0	0	13
1	1	1	0	1	mes2) 14 rad 0
nigra sint	1	1	1	0	15
or affected	1	1	1	1	16

### FUNCTION TABLE

got too			Clock		TABLE	1 25 00 13 (10 )	Decode	w, the counter will start country to the negative edge of the clot OSC INTRIT (PIn 14) — A TOPE IN RC oxcil ster which at
In <sub>1</sub>	Set	Reset		Inh	Out 1	Out 2	Out	
	0	0	0	0	_	~	No Change	
~	0	0	0	0	~		Advance to next state	
Х	1	0	0	0	0	1	1	
Х	0	1	0	0	0	1	0	
х	0	0	1	0	_	-	No Change	
x	0	0	0	1	0	1	No Change	
0	0	0	0	x	0	1	No Change	
1	0	0	0	5	~	5	Advance to next state	

X = Don't Care

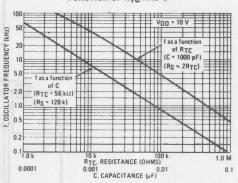


### TYPICAL RC OSCILLATOR CHARACTERISTICS

(For Circuit Diagram See Figure 11 in Application)

FIGURE 1 — RC OSCILLATOR STABILITY 8.0 VDD = 15 V (%) FREQUENCY DEVIATION 10 V -8.0 -12 RTC = 56 kΩ, RS = 0, f = 10.15 kHz @ VDD = 10 V, TA = 250C -16 -55 Device Only. C = 1000 pF --- RS = 120 ks2, f = 7.8 kHz @ VDD = 10 V, TA = 25°C 50 -25 25 75 TA, AMBIENT TEMPERATURE (°C)\*

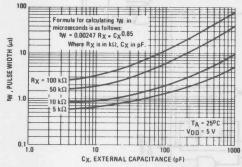
FIGURE 2 — RC OSCILLATOR FREQUENCY AS A FUNCTION OF RTC AND C



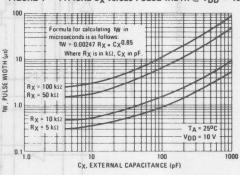
### MONOSTABLE CHARACTERISTICS

(For Circuit Diagram See Figure 10 in Application)

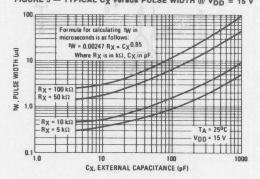




### FIGURE 4 — TYPICAL CX versus PULSE WIDTH @ VDD = 10 V

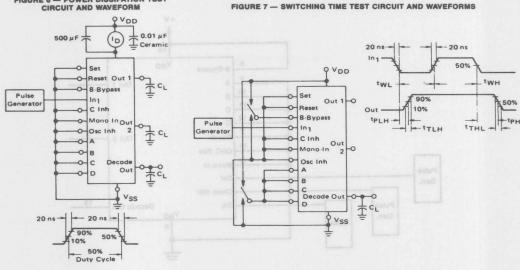


# FIGURE 5 — TYPICAL CX versus PULSE WIDTH @ VDD = 15 V



### MC14536B

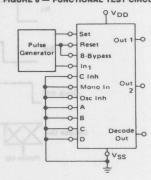
# FIGURE 6 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



#### **FUNCTIONAL TEST SEQUENCE**

Test function (Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24stages in series configuration. One more pulse is entered into In1 which will cause the counter to ripple from an all "1" state to an all "0" state.

### FIGURE 8 — FUNCTIONAL TEST CIRCUIT

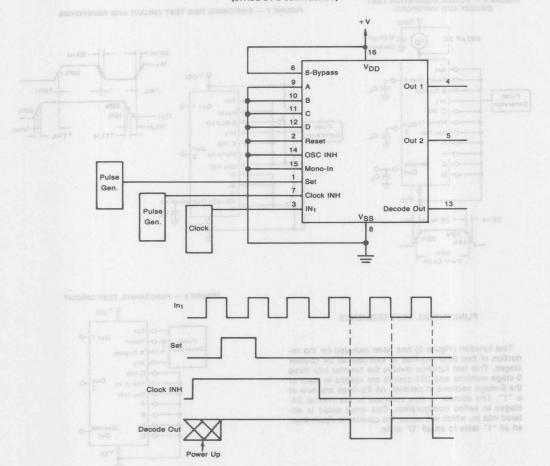


### **FUNCTIONAL TEST SEQUENCE**

INPUTS				OUTPUTS	TO OUT THE SEAL OF COMMENTS I BOOK TROUBLE OF THE				
In <sub>1</sub>	Set	Reset	8-Bypass	Decade Out Q1 thru Q24	All 24 stages are in Reset mode.				
1	0	mout 5510	1 Stagt & August 1	0	n esente) noisivith yensupart A 2A believ (where n				
1	1	1	21 Ut bns	0	Counter is in three 8 stage sections in parallel mode.				
0	1	1	1	0	First "1" to "0" transition of clock.				
1 0 - -	1	1	1		255 "1" to "0" transitions are clocked in the counter.				
0	1	.1	1	1	The 255 "1" to "0" transition.				
0	0	0	0	1	Counter converted back to 24 stages in series mode.  Set and Reset must be connected together and simultaneously go from "1" to "0".				
1	0	0	0	1	In 1 Switches to a "1".				
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state.				

## MC14536B

FIGURE 9 — TIME INTERVAL CONFIGURATION USING AN EXTERNAL CLOCK, SET, AND CLOCK INHIBIT FUNCTIONS (DIVIDE-BY-2 CONFIGURED)



Note: When power is first applied to the device, Decode Out can be either at a high or low state. On the rising edge of a Set pulse the output goes high if initially at a low state. The output remains high if initially at a high state. Because Clock Inh is held high, the clock source on the input pin has no effect on the output. Once Clock Inh is taken low, the output goes low on the first negative clock transition. The output returns high depending on the 8-Bypass, A, B, C, and D inputs, and the clock input period. A 2<sup>n</sup> frequency division (where n = the number of stages selected from the truth table) is obtainable at Decode Out. A 2<sup>n</sup> -divided output of iN<sub>1</sub> can be obtained at OUT<sub>1</sub> and OUT<sub>2</sub>.

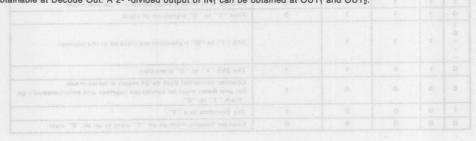
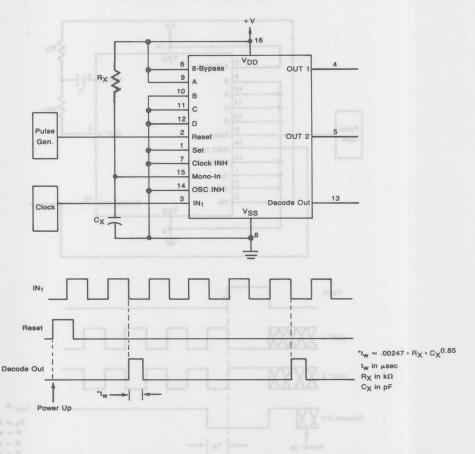
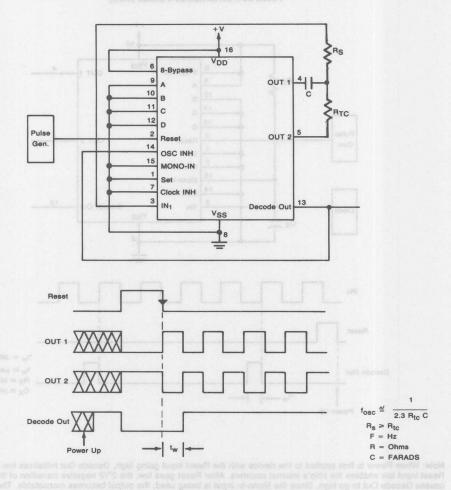


FIGURE 10 — TIME INTERVAL CONFIGURATION USING AN EXTERNAL CLOCK, RESET, AND OUTPUT MONOSTABLE TO ACHIEVE A PULSE OUTPUT. (DIVIDE-BY-4 CONGIFURED).



Note: When Power is first applied to the device with the Reset input going high, Decode Out initializes low. Bringing the Reset input low enables the chip's internal counters. After Reset goes low, the  $2^{n}/2$  negative transition of the clock input causes Decode Out to go high. Since the Mono-In input is being used, the output becomes monostable. The pulse width of the output is dependent on the external timing components. The second and all subsequent pulses occur at  $2^{n} \times$  (the clock period) intervals where n=th number of stages selected from the truth table.

FIGURE 11 — TIME INTERVAL CONFIGURATION USING ON-CHIP RC OSCILLATOR AND.RESET INPUT TO INITIATE TIME INTERVAL (DIVIDE-BY-2 CONFIGURED)



Note: This circuit is designed to use the on-chip oscillation function. The oscillator frequency is determined by the external R and C components. When power is first applied to the device, Decode Out initializes to a high state. Because this output is tied directly to the Osc-Inh input, the oscillator is disabled. This puts the device in a low-current standby condition. The rising edge of the Reset pulse will cause the output to go low. This in turn causes Osc-Inh to go low. However, while Reset is high, the oscillator is still disabled (i.e.: standy condition). After Reset goes low, the output remains low for 2<sup>n</sup>/2 of the oscillator's period. After the part times out, the output again goes high.



## MC14538B

# DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

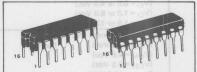
The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components,  $C_X$  and  $R_X$ .

- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10 μs to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive (A Input) or Negative-Going Edge (B-Input)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- Use the MC54/74HC4538 for Pulse Widths Less Than 10 μs with Supplies Up to 6 V.

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL PRECISION
RETRIGGERABLE/RESETTABLE
MONOSTABLE MULTIVIBRATOR



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

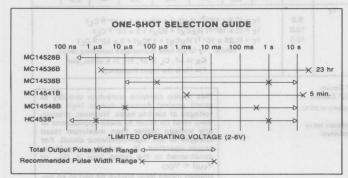
A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

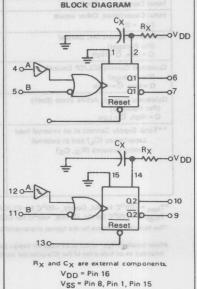
C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	No
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin. lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TI	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C





## **ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$ )

		VDD		w*		25°C		Thi	gh°	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level Vin = VDD or 0	VOL	5.0 10	-	0.05 0.05	Ξ	0 0	0.05	-	0.05	Vdc
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	BELL	4.95	5.0	R HO	4.95	9.40	Vdo
V <sub>in</sub> = 0 or V <sub>DD</sub>		10 15	9.95 14.95	TABLE	9.95 14.95	10	ATRO	9.95	Ξ	
nput Voltage "0" Level	VIL		A TA							Vdd
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		5.0	-	1.5	-	2.25	1.5	-	1.5	
(V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)		10	om Teld.	3.0 4.0	, el Cente	4.50 6.75	3.0	CH CO	3.0	and T
"1" Level	VIH	15	dufficion.	4.0	redike s	0.75	4.0	Market and	4.0	Vde
(VO = 0.5 or 4.5 Vdc)	VIH	5.0	3.5	100000	3.5	2.75	is ruith	3.5	goog b	3 00
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	-	7.0	5.50	_	7.0	Cy_see	olne
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (AL Device)	Іон		andar s	AREIN N	DIESCHAL	September 2	1112	man severa	C SPORTER	mAd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	91-	-1.7	COUNT ST	Hard .
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	- Tallia	-0.36	of made	ged i
(V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)		10 15	-1.6 -4.2		-1.3 -3.4	-2.25 -8.8	ni texel	-0.9 -2.4	1 65516	800
4의 공개를 된 게 된 것으로 보고 있는 다른 사람들이 되었다면 다른 것으로 되었다.	la:	5.0	0.64	-	0.51	0.88	azaneg c	0.36	CU COV	mAd
(V <sub>OL</sub> = 0.4 Vdc) Sink (V <sub>OL</sub> = 0.5 Vdc)	IOL	10	1.6	ninte-Dank	1.3	2.25	V or wise	0.36	aldwan	MAC
(VOL = 1.5 Vdc)		15	4.2		3.4	8.8	_	2.4	_	-
Output Drive Current (CL/CP Device)	Іон		917	ne Ren	15:79-0001	E betell a	Over th	seo.i Fi	T vybic	mAd
(VOH = 2.5 Vdc) Source	0	5.0	-2.5		-2.1	-4.2	-	-1.7	with Total	oto
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	102000	-0.44	-0.88	_	-0.36	-	Last I
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	BRT EN	-1.1	-2.25	00294	-0.9	700 BOL	DOU.
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4		
(VOL = 0.4 Vdc) Sink	IOL.	5.0	0.52	-	0.44	0.88	-	0.36	-	mAc
(V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)		10	1.3		1.1	2.25 8.8		0.9	I	
Input Current, Pin 2 or 14	lin	15	-	±0.05	-	±0.00001	±.05	-	±0.5	μAc
Input Current, Other Inputs (AL Device)	lin	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μΑσ
Input Current, Other Inputs (CL/CP Device)	lin	15	_	±0.3	SA THE	±0.00001	±0.3	-	±1.0	μΑσ
Input Capacitance, Pin 2 or 14	Cin	-	189_	_	_	25	CONT.	-	-	pF
Input Capacitance, Other Inputs (Vin = 0)	Cin	0.81	01 20	-	-	5.0	7.5	992.7	addīna.	pF
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μΑσ
(Per Package)	00	10	-	10	and day	0.010	10	0 10010	300	
Q=Low, Q=High	Win	15	- 500	20	_	0.015	20	noltegii	600	19
Quiescent Current (CL/CP Device)	IDD	5.0	DI #3-	20	-	0.005	20	darw.ro	150	μАс
(Per Package) Q = Low, Q = High	10	10	388	40	- 0	0.010	40	B15378 100	300	101
	- Supermonth	15	76 00150	80	0000000	0.015	80	-	600	
Quiescent Current, Active State (Both)  (Per Package)  Q = High, Q = Low	IDD	5 10 15	rea <u>a</u> r 3	2.0 2.0 2.0	OFTENS OF STREET	.04 .08 .13	.20 .45 .70	01E	2.0 2.0 2.0	mAd
**Total Supply Current at an external load capacitance (CL) and at external timing network (R <sub>X</sub> , C <sub>X</sub> )	ΙΤ	5.0 10.0 15.0	17	r = (3.5 x r = (8 x 1 r = (1.25	0 <sup>-2</sup> ) R <sub>X</sub> × 10 <sup>-1</sup> ) ere: I <sub>T</sub> i C <sub>X</sub>	R <sub>X</sub> C <sub>X</sub> f + 4C C <sub>X</sub> f + 9C <sub>X</sub> R <sub>X</sub> C <sub>X</sub> f + 1: n µA (one m in µF, C <sub>L</sub> in Hz is the in	xf + 1 x f + 2 x 1 2Cxf + 3 nonostab pF, Rx	0-5 CLf 3 x 10-5 le switch in k ohn	f CLf ing only	). 

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub>  $\leq$  (V<sub>in</sub> or V<sub>out</sub>)  $\leq$  V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Output Rise Time         tTLH         (1.35 ns/pF) CL + 33 ns         tTLH         (5.0         —         100         200           tTLH = (0.40 ns/pF) CL + 20 ns         tTLH         (5.0         —         100         200           tTLH = (0.40 ns/pF) CL + 20 ns         tTHL         5.0         —         40         80           Output Fall Time         tTHL         (1.35 ns/pF) CL + 33 ns         tTHL         (1.04 ns/pF) CL + 20 ns         10         —         50         100         200           tTHL = (0.40 ns/pF) CL + 20 ns         tPL, tPL         5.0         —         100         200         100         40         80           Propagation Delay Time         40         80         15         —         40         80           Propagation Delay Time         40         80         15         —         40         80           Propagation Delay Time         40         80         15         —         40         80           repl. thyll = (0.26 ns/pF) CL + 255 ns         tpLH, tPHL = (0.26 ns/pF) CL + 255 ns         15         —         300         600         600         600         600         600         600         600         600         600         600         600         600			.,		All Types		- 8	
Title	Characteristic	Symbol		Min	Тур#	Max	Unit	
tTLH = (0.60 ns/pF) CL + 20 ns         10         -         50         100           Output Fall Time         tTHL = (0.40 ns/pF) CL + 20 ns         15         -         40         80           tTHL = (1.35 ns/pF) CL + 20 ns         tTHL = (0.60 ns/pF) CL + 20 ns         10         -         50         100           tTHL = (0.60 ns/pF) CL + 20 ns         10         -         50         100 <td>Output Rise Time</td> <td>tTLH</td> <td></td> <td>- 17 - A-</td> <td></td> <td></td> <td>ns</td>	Output Rise Time	tTLH		- 17 - A-			ns	
tTLH = (0.40 ns/pF) CL + 20 ns         15         — 40         80           Output Fall Time tTHL = (1.35 ns/pF) CL + 33 ns tTHL = (0.60 ns/pF) CL + 20 ns tTHL = (0.60 ns/pF) CL + 20 ns tTHL = (0.40 ns/pF) CL + 20 ns tTHL = (0.40 ns/pF) CL + 20 ns tTHL = (0.40 ns/pF) CL + 20 ns tTHL = (0.40 ns/pF) CL + 20 ns tTHL = (0.40 ns/pF) CL + 20 ns tTHL = (0.40 ns/pF) CL + 20 ns tTHL = (0.40 ns/pF) CL + 255 ns tTHL = (0.36 ns/pF) CL + 132 ns tTHL = (0.36 ns/pF) CL + 132 ns tTHL = (0.36 ns/pF) CL + 87 ns tTHL = (0.26 ns/pF) CL + 87 ns tTHL = (0.90 ns/pF) CL + 205 ns tTHL = (0.90 ns/pF) CL + 205 ns tTHL = (0.90 ns/pF) CL + 205 ns tTHL = (0.90 ns/pF) CL + 82 ns tTHL = (0.	tTLH = (1.35 ns/pF) CL + 33 ns	59	77,000	14-	The second second		. 25	
Output Fall Time         tTHL         5.0         -         100         200           tTHL = (1.35 ns/F) C <sub>L</sub> + 20 ns         10         -         5.0         -         100         200           tTHL = (0.40 ns/F) C <sub>L</sub> + 20 ns         10         -         50         100         80           Propagation Delay Time         tpLH.         40         80         80         80           Propagation Delay Time         tpLH. tpL = (0.90 ns/F) C <sub>L</sub> + 255 ns         10         -         150         300         600           tpLH. tpHL = (0.90 ns/F) C <sub>L</sub> + 255 ns         10         -         150         300         600         150         300         600         150         300         600         150         300         600         150         300         600         150         300         600         150         300         600         150         300         600         150         300         600         150         300         600         150         300         150         300         150         300         150         300         150         300         150         300         150         150         300         150         300         150         300         150 <td></td> <td>P. Carrier</td> <td></td> <td>-</td> <td></td> <td></td> <td></td>		P. Carrier		-				
THL = (1.35 ns/pF) CL + 33 ns tTHL = (0.60 ns/pF) CL + 20 ns tTHL = (0.60 ns/pF) CL + 20 ns tTHL = (0.60 ns/pF) CL + 20 ns tTHL = (0.60 ns/pF) CL + 20 ns tTHL = (0.60 ns/pF) CL + 255 ns tpLH tpHL = (0.36 ns/pF) CL + 132 ns tpLH tpHL = (0.36 ns/pF) CL + 132 ns tpLH tpHL = (0.36 ns/pF) CL + 87 ns Reset to O or Q tpLH tpHL = (0.90 ns/pF) CL + 205 ns tpLH tpHL = (0.90 ns/pF) CL + 207 ns tpLH tpHL = (0.90 ns/pF) CL + 2	<sup>t</sup> TLH = (0.40 ns/pF) C <sub>L</sub> + 20 ns		15	-		80		
1THL = (0.60 ns/pF) CL + 20 ns     10     -     50     100       Propagation Delay Time     tpLH,     -     40     80       Propagation Delay Time     tpLH, tpHL = (0.36 ns/pF) CL + 255 ns     tpLH, tpHL = (0.36 ns/pF) CL + 255 ns     10     -     150     300       tpLH, tpHL = (0.36 ns/pF) CL + 87 ns     10     -     150     300       tpLH, tpHL = (0.26 ns/pF) CL + 87 ns     15     -     100     220       Reset to Q or Q     tpLH, tpHL = (0.36 ns/pF) CL + 205 ns     10     -     125     250       tpLH, tpHL = (0.36 ns/pF) CL + 82 ns     15     -     95     190       Input Filse and Fall Times     1r, ty     5     -     -     15       Reset     10     -     15     -     -     15       B Input     5     -     300     1.0		tTHL			1000	1	ns	
tTHL = (0.40 ns/pF) C <sub>L</sub> + 20 ns         15         -         40         80           Propagation Delay Time         tpLH, tpHL = 0.90 ns/pF) C <sub>L</sub> + 255 ns         tpLH, tpHL = (0.36 ns/pF) C <sub>L</sub> + 255 ns         -         300         600           tpLH, tpHL = (0.36 ns/pF) C <sub>L</sub> + 132 ns         10         -         150         300         600           tpLH, tpHL = (0.36 ns/pF) C <sub>L</sub> + 132 ns         15         -         100         220           Reset to Q or Q         tpLH, tpHL = (0.90 ns/pF) C <sub>L</sub> + 205 ns         10         -         125         250           tpLH, tpHL = (0.36 ns/pF) C <sub>L</sub> + 82 ns         15         -         95         190           Input Rise and Fall Times         tr, ty         5         -         -         15           Reset         tr, ty         5         -         -         15           B input         5         -         -         -         5           B input         5         -         -         -         -         15           A input         5         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -			100,000	17	the state of the s	1000000	1	
Propagation Delay Time		101100		1	L 1997 T 211	Delta de la constantina della		
A or B to Q or Q  \$tp.H. tpHL = (0.90 ns/pF) CL + 255 ns \$tp.H. tpHL = (0.36 ns/pF) CL + 255 ns \$tp.H. tpHL = (0.26 ns/pF) CL + 132 ns \$tp.H. tpHL = (0.26 ns/pF) CL + 87 ns  Reset to Q or Q  \$tp.H. tpHL = (0.90 ns/pF) CL + 205 ns \$tp.H. tpHL = (0.90 ns/pF) CL + 205 ns \$tp.H. tpHL = (0.36 ns/pF) CL + 107 ns \$tp.H. tpHL = (0.36 ns/pF) CL + 107 ns \$tp.H. tpHL = (0.26 ns/pF) CL + 82 ns  \$tp.H. tpHL = (0.26 n			15		40	80		
tpl.H. tph.L = (0.90 ns/pF) CL + 255 ns     5.0     —     300     600       tpl.H. tph.L = (0.36 ns/pF) CL + 132 ns     10     —     150     300       tpl.H. tph.L = (0.06 ns/pF) CL + 132 ns     15     —     100     220       Reset to Q or Q     —     250     500     —     250     500       tpl.H. tph.L = (0.36 ns/pF) CL + 107 ns     10     —     125     250     190       Input. Rise and Fall Times     tr., tr.     5     —     —     15     —     95     190       Input Rise and Fall Times     tr., tr.     5     —     —     —     15     —     —     15     —     —     15     —     —     15     —     —     15     —     —     15     —     —     —     15     —     —     —     15     —     —     —     15     —     —     —     15     —     —     —     —     —     15     —     —     —     15     —     <			1.50		1-00	0 B	ns	
tpLH. tpHL = (0.36 ns/pF) CL + 132 ns tpLH. tpHL = (0.26 ns/pF) CL + 87 ns         10         -         150         300         220         15         -         100         220         15         -         100         220         250         500         -         -         15         -         -         -         15         -         -         -         -         -         -         -         -         -         -         -         -         -         -         - </td <td></td> <td>tPHL</td> <td></td> <td></td> <td></td> <td>0110</td> <td></td>		tPHL				0110		
TPLH. TPHL = (0.26 ns/pF) CL + 87 ns           Reset to Q or Q         15         -         100         220           TPLH. TPHL = (0.90 ns/pF) CL + 205 ns         5.0         -         250         500           TPLH. TPHL = (0.36 ns/pF) CL + 107 ns         10         -         125         250           TPLH. TPHL = (0.26 ns/pF) CL + 82 ns         15         -         95         190           Input Rise and Fall Times         10         -         -         5           Reset         10         -         -         5           B Input         5         -         -         -         5           B Input         5         -         -         -         -         5           A Input         5         -		of recent Planser to	10000	-		2700012		
Reset to Q or Q   tp LH, tp HL = (0.90 ns/pF) CL + 205 ns tp LH, tp HL = (0.36 ns/pF) CL + 107 ns tp LH, tp HL = (0.36 ns/pF) CL + 82 ns   15	tpLH, tpHL = (0.36 ns/pF) CL + 132 ns			-			1	
tp_H, tpHL = (0.90 ns/pF) CL + 205 ns tp_H, tpHL = (0.36 ns/pF) CL + 107 ns tp_H, tpHL = (0.26 ns/pF) CL + 107 ns tp_H, tpHL = (0.26 ns/pF) CL + 82 ns     5.0			15	-	100	220		
tpLH, tpHL = (0.36 ns/pF) CL + 107 ns tpLH, tpHL = (0.26 ns/pF) CL + 82 ns         10         —         125 250 190           Input Rise and Fall Times Reset         15         —							ns	
tp_H, tpHL = (0.26 ns/pF) CL + 82 ns     15     — 95     190       Input Rise and Fall Times Reset     t <sub>r</sub> , t <sub>f</sub> 5     — — 15     — 4       B Input     5     — 300     1.0     — 1.2     0.1       A Input     5     — 300     1.0     — 1.2     0.1       A Input     5     — 0.4     0.05       A Input Pulse Width     TuWH     10     90     45     — 10       A, B, or Reset     t <sub>WL</sub> 10     90     45     — 10       Retrigger Time     t <sub>rr</sub> 5.0     0     — — — — 10       Refer in Figures 8 and 9     T     T     T       C <sub>X</sub> = 0.002 μF, R <sub>X</sub> = 100 kΩ     5.0     198     210     230       10     200     212     232       15     202     214     234       C <sub>X</sub> = 0.01 μF, R <sub>X</sub> = 100 kΩ     5.0     9.4     10     10.6       10     9.4     10     10.6     15     9.5     10.14     10.7       C <sub>X</sub> = 10 μF, R <sub>X</sub> = 100 kΩ     5.0     0.91     0.995     1.04       10     0.992     0.988     1.04       10     0.992     0.998     1.04       10     0.993     0.999     1.06       10				-	77.74		13.44	
Input Rise and Fall Times   Test   Times	tpLH, tpHL = (0.36 ns/pF) CL + 107 ns	STREET BOATS	CONTRACTOR SET TO UNIO	dunt Joue	1 222		1	
Reset       10       —       —       5         B Input       5       —       300       1.0         10       —       1.2       0.1         15       —       0.4       0.05         A Input         Input Pulse Width         A, B, or Reset       10       170       85       —         15       80       40       —       —         Retrigger Time       15       80       40       —       —         Retrigger Time       10       0       — </td <td>tpLH, tpHL = (0.26 ns/pF) CL + 82 ns</td> <td></td> <td>15</td> <td>-</td> <td>95</td> <td>190</td> <td></td>	tpLH, tpHL = (0.26 ns/pF) CL + 82 ns		15	-	95	190		
Reset   10	Input Rise and Fall Times	tr. te	5		_	15	μs	
			10	- 00	_	5	1	
A Input A Input Pulse Width A, B, or Reset $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			15			4		
A Input Pulse Width A, B, or Reset $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	B Input		5	1 = -0	300	1.0	ms	
A Input Pulse Width A, B, or Reset $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			0.50	11-4				
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				-	0.4	0.05		
Input Pulse Width A, B, or Reset	A Input			Hu &			-	
Input Pulse Width A, B, or Reset				4 1 1	No Limit			
A, B, or Reset			and the second	Lalf-h L				
Retrigger Time $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			7-350	And the second second second second	The second secon	-	ns	
Retrigger Time $t_{rr}$ 5.0         0         - <td>A, B, or Reset</td> <td>TWL</td> <td></td> <td></td> <td></td> <td>1</td> <td></td>	A, B, or Reset	TWL				1		
		-			40		-	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Retrigger Time	trr	10000		8	-6	ns	
Output Pulse Width $-$ Q or $\bar{\Omega}$ T       Refer to Figures 8 and 9     5.0     198     210     230 $C_X = 0.002  \mu\text{F}$ , $R_X = 100  k\Omega$ 10     200     212     232       15     202     214     234 $C_X = 0.1  \mu\text{F}$ , $R_X = 100  k\Omega$ 5.0     9.3     9.86     10.5       10     9.4     10     10.6       15     9.5     10.14     10.7 $C_X = 10  \mu\text{F}$ , $R_X = 100  k\Omega$ 5.0     0.91     0.965     1.03       10     0.92     0.98     1.04       15     0.93     0.99     1.06       Pulse Width Match between circuits in     100(T1 - T2)     5.0     -     ±1.0     ±5.0		1 10000	1000			-		
Refer to Figures 8 and 9 $ C_X = 0.002  \mu\text{F},  R_X = 100  k\Omega $ 5.0 198 210 230 212 232 15 202 214 234 $ C_X = 0.1  \mu\text{F},  R_X = 100  k\Omega $ 5.0 9.3 9.86 10.5 10 9.4 10 10.6 15 9.5 10.14 10.7 $ C_X = 10  \mu\text{F},  R_X = 100  k\Omega $ 5.0 0.91 0.965 1.03 10 0.92 0.98 1.04 15 0.93 0.99 1.06 $ Pulse  \text{Width Match between circuits in} $ 100(T1 – T2) 5.0 – ±1.0 ±5.0		-	15	0	BIGGET - D	-	-	
$\begin{array}{c} \text{C}_{\text{X}} = 0.002\mu\text{F},\text{R}_{\text{X}} = 100\text{k}\Omega \\ \text{C}_{\text{X}} = 0.002\mu\text{F},\text{R}_{\text{X}} = 100\text{k}\Omega \\ \text{C}_{\text{X}} = 0.1\mu\text{F},\text{R}_{\text{X}} = 100\text{k}\Omega \\ \text{C}_{\text{X}} = 0.1\mu\text{F},\text{R}_{\text{X}} = 100\text{k}\Omega \\ \text{C}_{\text{X}} = 10\mu\text{F},\text{R}_{\text{X}} = 100\text{k}\Omega \\ \text{C}_{\text{X}} = 10\mu\text{F},\text{R}_{\text{X}} = 100\text{k}\Omega \\ \text{E}_{\text{X}} = 100\mu\text{F},\text{R}_{\text{X}} = 100\mu\text{F},$		- 1	12		A		μs	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			5.0	198				
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$C_X = 0.002 \mu\text{F}, R_X = 100 k\Omega$		F-12-12-15					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			1000					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	0 -0.1 5 0 100.0			+	Control of the Control		ms	
$C_{X} = 10 \ \mu\text{F}, \ R_{X} = 100 \ k\Omega \\ \hline \\ C_{X} = 10 \ \mu\text{F}, \ R_{X} = 100 \ \mu\text{F}, \ R_{X} = 100 \ \mu\text{F}$	CX = 0.1 μF, HX = 100 kΩ				200000		ITIS	
$C_X = 10  \mu\text{F},  R_X = 100  k\Omega$ 5.0 0.91 0.965 1.03 10 0.92 0.98 1.04 15 0.93 0.99 1.06 Pulse Width Match between circuits in 100 $(T_1 - T_2)$ 5.0 - $\pm 1.0 \pm 5.0$			7.7		1.00			
10	Cu = 10 "F Ru = 100 kg			0.04	-	-	s	
15 0.93 0.99 1.06		A THE PARTY OF THE					,	
Pulse Width Match between circuits in $100(T_1 - T_2)$ 5.0 - $\pm 1.0$ $\pm 5.0$		market level - K	The second second second		(State)			
100111-127	Pulse Width Match between circuits in	100(Ta - Ta)		- 401		-	%	
	the same package.	T.	10	8	±1.0		1 0	
the same package. T1 10 - $\pm 1.0$ $\pm 5.0$ Cx = 0.1 $\mu$ F, Rx = 100 $k\Omega$ 2347344434 15 - $\pm 5.0$				1 51				

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

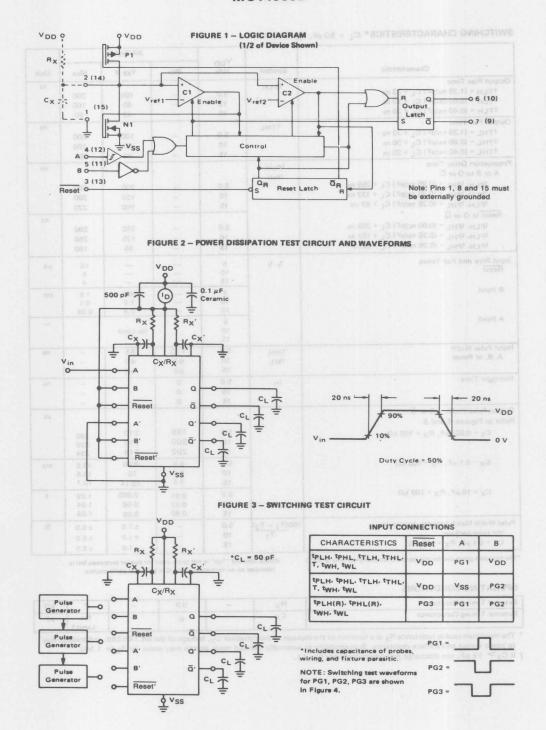
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

#### **OPERATING CONDITIONS**

External Timing Resistance	RX	-	5.0	-	0-1	kΩ
External Timing Capacitance	CX		0	-	No Limit†	μF

The maximum usable resistance R<sub>X</sub> is a function of the leakage of the capacitor C<sub>X</sub>, leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptability to externally induced noise signals may occur for R<sub>X</sub> > 1 MΩ.
 † If C<sub>X</sub> > 15 μF, use discharge protection diode per Fig. 11.

## MC14538B



## MC14538B

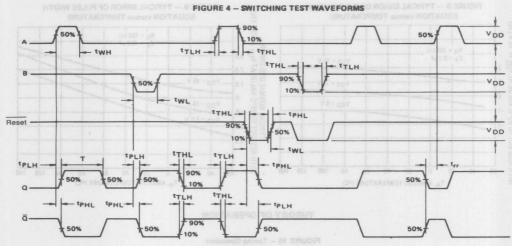


FIGURE 5 - TYPICAL NORMALIZED DISTRIBUTION OF UNITS FOR OUTPUT PULSE WIDTH

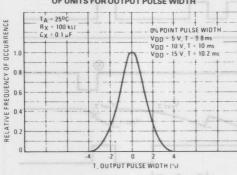


FIGURE 6 - TYPICAL PULSE WIDTH VARIATION AS A FUNCTION OF SUPPLY VOLTAGE VDD

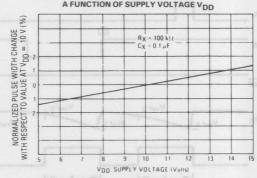
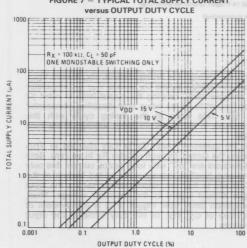
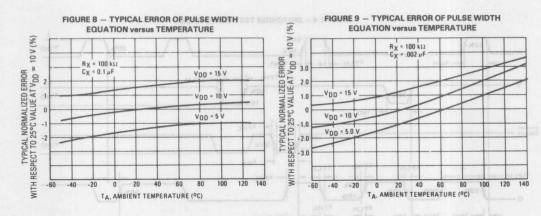


FIGURE 7 - TYPICAL TOTAL SUPPLY CURRENT



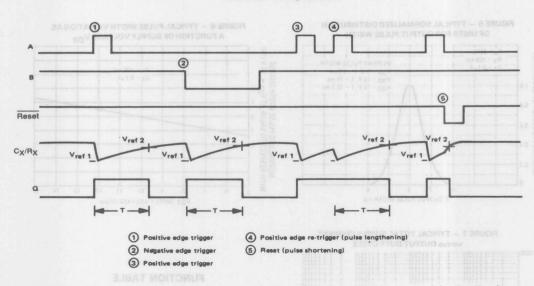
**FUNCTION TABLE** 

	Inputs		Outp	outs
Reset	A	В	Q	ā
H 19	-	7	Y T	7
H	√ V H	27	Not Tri	
H	L, H, <b>\</b> L	H L, H, <b>√</b>	Not Tri	
25	X	X	L Not Tri	H ggered



#### THEORY OF OPERATION

FIGURE 10 - Timing Operation



#### TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C<sub>X</sub> completely charged to V<sub>DD</sub>. When the trigger input A goes from V<sub>SS</sub> to V<sub>DD</sub> (while inputs B and Reset are held to V<sub>DD</sub>) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C<sub>X</sub> rapidly discharges toward V<sub>SS</sub> until V<sub>ref1</sub> is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C<sub>X</sub> begins

to charge through the timing resistor, R $\chi$ , toward V<sub>DD</sub>. When the voltage across C $\chi$  equals V<sub>ref.2</sub>, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 ②. This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state,  $C_X$  is fully charged to  $V_{DD}$  causing the current through resistor  $R_X$  to be zero. Both comparators are "off" with total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of  $C_X$ ,  $R_X$ , or the duty cycle of the input waveform.

#### RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs 3 followed by another valid trigger 4 before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V<sub>ref.1</sub>, but has not yet reached V<sub>ref.2</sub>, will cause an increase in output pulse width T. When a valid retrigger is initiated (4), the voltage at Cx/Rx will again drop to Vref 1 before progressing along the RC charging curve toward VDD. The Q output will remain high until time T, after the last valid retrigger.

#### RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on Reset sets the reset latch and causes the capacitor to be fast charged to VDD by turning on transistor P1 (5). When the voltage on the capacitor reaches Vref 2, the reset latch will clear, and will then be ready to accept another pulse. If the Reset input is held low, any trigger inputs that occur will be inhibited and the Q and Q outputs of the output latch will not change. Since the Q output is reset when an input low level is

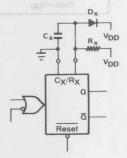
detected on the Reset input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

#### **POWER-DOWN CONSIDERATIONS**

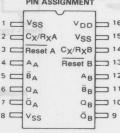
Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B is powered down, the capacitor voltage may discharge from VDD through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the VDD supply must not be faster than (VDD). (C)/(10 mA). For example, if VDD = 10 V and CX = 10  $\mu$ F, the VDD supply should discharge no faster than (10 V)  $\times$  (10  $\mu$ F)/(10 mA) = 10 ms. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of VDD to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode, Dx, connected as shown in Fig. 11.

FIGURE 11 - USE OF A DIODE TO LIMIT **POWER DOWN CURRENT SURGE** 



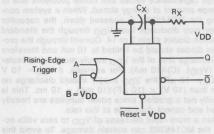




## MC14538B

## TYPICAL APPLICATIONS

FIGURE 12 — RETRIGGERABLE MONOSTABLES CIRCUITRY



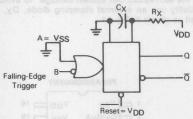


FIGURE 13 — NON-RETRIGGERABLE MONOSTABLES CIRCUITRY

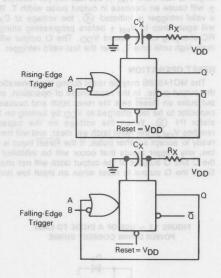
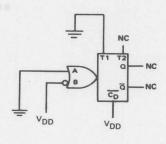


FIGURE 14 — CONNECTION OF UNUSED SECTIONS





MC14539B

#### **DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER**

The MC14539B data selector/multiplexer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of two sections of four inputs each. One input from each section is selected by the address inputs A and B. A "high" on the Strobe input will cause the output to remain "low"

This device finds primary application in signal multiplexing functions. It permits multiplexing from N-lines to I-line, and can also perform parallel-to-serial conversion. The Strobe input allows cascading of n-lines to n-lines.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter 000000	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
In. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

#### TRUTH TABLE

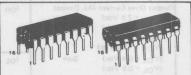
	RESS	D	ATA I	NPUTS	;			
INP	NPUTS X3 X2		X1 X0		Aug of stry	OUTPUTS		
В	A	Y3	Y2 Y1 Y		YO	ST,ST'	Z, W	
X	X	X	×	X	Х	1	0	
0	0	X	X	X	0	0	0	
0	0	X	X	X	1	0	1	
0	1	X	X	0	X	0	0	
0	1	X	X	1	X	0	1	
1	0	X	0	X	X	0	0	
1	0	X	100	X	X	0	ment of the	
1	1	0	X	X	X	0	0	
1	1	1	X	X	X	0	1	

X = Don't Care

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

**DUAL 4-CHANNEL** DATA SELECTOR/MULTIPLEXER



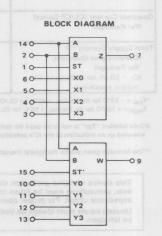
CERAMIC PACKAGE PLASTIC PACKAGE CASE 620

**CASE 648** 

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



VDD = Pin 16 VSS = Pin 8

#### ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tic	w*		25°C		Thi	gh *	1
Characteristic	Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	- 1	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	-	10		0.05	-	0	0.05	- 1	0.05	-
111 00		15	-	0.05		0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	_	4.95	-	Vdc
Vin = 0 or VDD	- OH	10	9.95	_	9.95	10	_	9.95	_	
Vin - O OI VDD		15	14.95		14.95	15	-	14.95	_	
nput Voltage "0" Level	VIL		1		-					Vdd
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	-11	5.0	3368.7	1.5	ARRIT	2.25	1.5	MAZAN	1.5	10
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10		3.0	-	4.50	3.0	-	3.0	
The state of the s		15		4.0		6.75	4.0	64001	4.0	+
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	VIH			4.0		0.70			P-ciram	OSS.
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	TH	5.0	3.5	SHOHVARD S	3.5	2.75	entresen	3.5	erianije s Iz o <del>lit</del> itilo	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	TOO TOO	7.0	5.50	DANCE BULL	7.0		1,433
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	and I	15	11.0	1 vg 1995	11.0	8.25	a most	11.0	еасп. О	String.
Output Drive Current (AL Device)		13	11.0	ASSESS III	11.0	0.25	no de	11.0	1888 A 20	mAd
	ЮН	5.0	-3.0		-2.4	-4.2		-1.7	al' nism	MAG
(V <sub>OH</sub> = 2.5 Vdc) Source	110	5.0	-0.64	on Blagi	-0.51	-0.88	primar	-0.36	lyeli ziri	
(V <sub>OH</sub> = 4.6 Vdc)		10	-1.6	is soul-l	-0.51 $-1.3$	-2.25	Malourin	-0.36	#1 anoi:	fun
(VOH = 9.5 Vdc)	89 1	15	-4.2	sugni s	-3.4	-8.8	reros fei	-2.4	ned and	nsq.
(V <sub>OH</sub> = 13.5 Vdc)	Mark .		-		-	-	-		Har to gr	1
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36		mAd
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.25	J.C. = 30	0.9	V Flags	0
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	-	2.4	محمارته م	
Output Drive Current (CL/CP Device)	ОН			and some		hotes o	Over ut	SHELL ST		mAd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	- 7	-1.7	P 10 -77	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	-	-0.36	- 11	
(V <sub>OH</sub> = 9.5 Vdc)	W. H	10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6		-3.0	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc) Sink	OL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAde
(V <sub>OL</sub> = 0.5 Vdc)		10	1.3	-	1.1	2.25	-	0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)	3	15	3.6	-	3.0	8.8		2.4	-	
nput Current (AL Device)	lin	15	-	± 0.1	(p=)V-1	± 0.00001	± 0.1		± 1.0	μAdo
nput Current (CL/CP Device)	lin	15	accto	±03	-	±0.00001	± 0.3	-	± 1.0	μAde
nout Capacitance	Cin	-			-	5.0	7.5	0.07 0.00	deaths to	pF.
(V <sub>in</sub> 0)	-111		0.404 7 50							1
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAd
(Per Package)	,00	10	_ 07	10	mili yaq	0.010	10	stpor_Gues	300	Jug
		15	- 083	20	-	0.015	20	1 1 1 1 1	600	
Quiescent Current (CL/CP Device)	1	5.0	-	20	-	0.005	20		150	μAd
(Per Package)	l DD	10	00T = -61	40	_	0.005	40	TELEGRACION .		ДАО
(rerrackage)		15	108	80		0.015	80	anutara	300 600	1 3
Total Supply Courses * * *	l-		2000	00		-		MOV ROOM	600	1 .
Total Supply Current**†	IT	5.0	1			).85 µA/kHz				μAd
(Dynamic plus Quiescent,			OF 881 N			1.7 µA/kHz				
Per Package)		15			IT = (	2.6 µA/kHz	101 + T	,		
(CL 50 pF on all outputs, all			In the second							1

<sup>\*</sup>Tlow = -55°C for AL Device, -40°C for CL/CP Device. Thigh = + 125°C for AL Device, +85°C for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_{\mbox{\scriptsize T}}$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

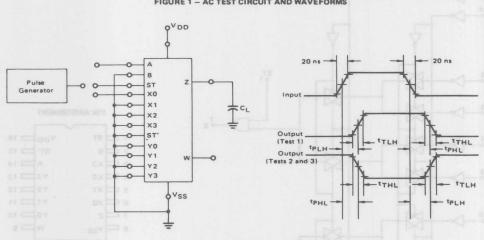
<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time tTLH. tTHL = (1.5 ns/pF) C <sub>L</sub> + 25 ns tTLH. tTHL = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns tTLH. tTHL = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	tTLH- tTHL	5.0 10 15	5	100 50 40	200 100 80	ns
Propagation Delay Time  X, Y Input to Output  tp_H, tpHL = (1.7 ns/pF) C <sub>L</sub> + 125 ns  tp_H, tpHL = (0.66 ns/pF) C <sub>L</sub> + 57 ns  tp_H, tpHL = (0.55 ns/pF) C <sub>L</sub> + 45 ns	<sup>t</sup> PLH, <sup>t</sup> PHL	5.0 10 15	-	210 90 70	420 180 140	ns
A Input to Output  tp_H = (1.7 ns/pF) C <sub>L</sub> + 140 ns  tp_H = (0.66 ns/pF) C <sub>L</sub> + 77 ns  tp_H = (0.5 ns/pF) C <sub>L</sub> + 60 ns	†PLH	5.0 10 15	180- 070- 170-	225 110 85	450 220 170	ns Putter Outstand
tpHL = (1.7 ns/pF) C <sub>L</sub> + 160 ns tpHL = (0.66 ns/pF) C <sub>L</sub> + 82 ns tpHL = (0.5 ns/pF) C <sub>L</sub> + 65 ns	tPHL.	5.0 10 15	0F-0-	245 115 90	490 230 180	ns
Strobe Input to Output  tp_LH, tpHL = (1.7 ns/pF) C <sub>L</sub> + 60 ns  tp_LH, tpHL = (0.56 ns/pF) C <sub>L</sub> + 42 ns  tp_LH, tpHL = (0.5 ns/pF) C <sub>L</sub> + 35 ns	tPLH, tPHL	5.0 10 15	17 -0- -0- -0- -0-	145 75 60	290 150 120	ns

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

FIGURE 1 - AC TEST CIRCUIT AND WAVEFORMS

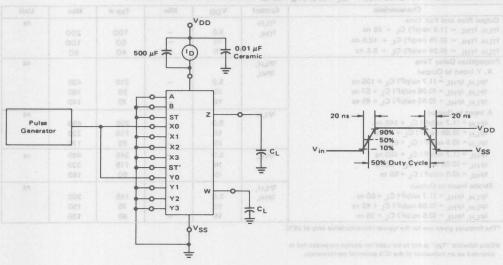


Input Connections for tTLH, tTHL, tPHL, tPLH

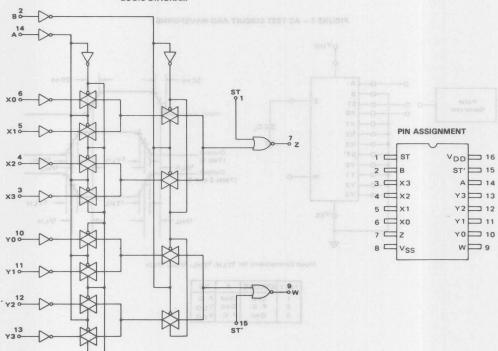
TEST	STROBE	A	XO
1	Gnd	Gnd	P. G
2	P.G.	Gnd	VDD
3	Gnd	P. G.	VDD

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 2 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM







## MC14541B

#### PROGRAMMABLE TIMER

The MC14541B programmable timer consists of a 16-stage bihary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified  $V_{DD}$  range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency ( $f_{OSC}$ ) with the  $n^{th}$  stage frequency being  $f_{OSC}/2^n$ .

- Available Outputs 28, 210, 213 or 216
- Increments on Positive Edge Clock Transitions
- Built-in Low Power RC Oscillator
   (± 2% accuracy over temperature range and ± 20% supply and ± 3% over processing at < 10 kHz)</li>
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2<sup>n</sup> Frequency Divider or Single Transition Timer
- Q/Q Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow CLock Rise and Fall Times
- Automatic Reset Initializes All Counters On Power Up
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disabled (Pin 5 = V<sub>DD</sub>)
  - = 8.5 Vdc to 18 Vdc with Auto Reset Enabled (Pin 5 = VSS)

#### MAXIMIM PATINGS\* (Voltages Referenced to Voc)

MIXAIM	UM HATINGS" (Voltages Heterenced to VSS	5)	101
Symbol	Parameter Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
lin	Input Current (DC or Transient), per Pin	± 10	mA
lout	Output Current (DC or Transient), per Pin	± 45	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
Tied	Lead Temperature (8-Second Soldering)	260	°C

"Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

OSCILLATOR/TIMER





CERAMIC PACKAGE
CASE 632

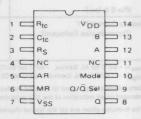
P SUFFIX
PLASTIC PACKAGE
CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



NC = No Connection

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tic	w*		25°C		Thi	gh"	
Characteristic	Symbol		Min	Max	Min	Typ#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0		0.05	_	0	0.05	-	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	·OL	10	-	0.05	-	0	0.05	- 1	0.05	
VIII VDD SI S		15	_	0.05		0	0.05	no-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	_	Vdc
Vin = 0 or VDD	*OH	10	9.95		9.95	10		9.95		100
AIW - O OL ADD		15	14.95	_	14.95	15	_	14.95	_	May 7
LEUS 3314 LESME J 1912 C.2013 1 3	Contract of the Contract of th	10	14.00		14.00	-		14.00	H. 1 153.1 -	17
Input Voltage "0" Level	VIL		Ligare of	MS-OF II	D Ellerene	a numin sld	Element of	2014 - 62 1 PM		Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		5.0	ODO <del>D</del> Q63	1.5	106 -010	2.25	1.5	001-121	1.5	nuos
(AQ = 8.0 ot 1.0 Agc)		10	ndino p	3.0	13521	4.50	3.0	BE-210	3.0	bna
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	-	4.0	-	6.75	4.0	-	4.0	nines
"1" Level	VIH		nevigo 91	I notina	Series Tank	ing an pa	nuz vd	\$2371B1314		Vdc
(V <sub>O</sub> = 0.5 or 4.5 Vdc)		5.0	3.5	arti Tridi	3.5	2.75	Indiana I	3.5	TES 27 780	m no
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	Inag) las	7.0	5.50	§ 78970	7.0	V spost	ag¥
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	edi Dina	11.0	8.25	21.70.8	11.0	Died. U.	36.30
Output Drive Current (AL Device)	ІОН		sen OR i	externa	m ve b	determin	egerangs	eith a rhie	spillate	mAd
(VOH = 2.5 Vdc) Source		5.0	-7.96	terror in the	-6.42	-12.83	b Table	-4.49	N THE	shrow
(VOH = 9.5 Vdc)		10	-4.19	-	-3.38	-6.75	S.tons	-2.37	e film set	drive
(VOH = 13.5 Vdc)	The last	15	-16.3	-	-13.2	-26.33	-	-9.24	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	1.93	-	1.56	3.12	-	1.09	-	mAd
(VOL = 0.5 Vdc)		10	4.96	-	4.0	8.0	5-02	2.8	uld4hav	A 0
(VOL = 1.5 Vdc)		15	19.3	- 200	15.6	31.2	9 Tours	10.9	DSEDS15	1 00
Output Drive Current (CL/CP Device)	ІОН									mAd
(VOH = 2.5 Vdc) Source	·OH	5.0	-5.1	_	-4.27	- 12.83	0 28	-3.5	or via	1
(V <sub>OH</sub> = 9.5 Vdc)		10	-2.69	a d Bhe	-2.25	-6.75	15W0	-1.85	885 T)	
(VOH = 13.5 Vdc)		15	-10.5	DIFFE	-8.8	-26.33	HIST TOW	-7.22	ply_and	
(V <sub>OL</sub> = 0.4 Vdc) Sink	la.	5.0	1.24	150 A 21	1.04	3.12	20-00	0.85	tot-line	0.8
(VOL = 0.5 Vdc)	IOL	10	3.18	_	2.66	8.0	n=	2.18		
(VOL = 1.5 Vdc)		15	12.4	_	10.4	31.2	11000	8.50	Hank o A	Pt .
Input Current (AL Device)	l.	15	_	±0.1	_	±0.00001	±0.1	-	±1.0	μAdo
	lin					-		0.000	DIG TRIKE	
Input Current (CL/CP Device)	lin	15	Serrick also	±0.3	alternid s	±0.00001	±0.3	8/5 4	±1.0	μAdd
Input Capacitance (Vin = 0)	Cin	-	-	ynillidos	avel File	5.0	7.5	bivare ti	O Selen	pF
Quiescent Current (AL Device)			A finaliza	Printer and	SI TURETI	peti dalda	110, (197	CONTROL NO	12071300	μAdo
		5.0	-	5.0	- 0	0.005	5.0	MODA O	150	
(Pin 5 is High)	IDD	10	# 0 (2- V15)	10	orte-sol	0.010	10	nin-dia	300	0 0
Auto Reset Disabled		15	-	20	-	0.015	20	E STORE OF	600	3
Quiescent Current (CL/CP Device)				100	L A A				a later est est	μAde
adiabonit odironi (oz,or borico)		5.0	_	20	803 BU	0.005	20	ma nagon	150	Price
(Pin 5 is High)	IDD	10	_	40	Mine poly	0.010	40	nen sos	300	6 0
Auto Reset Disabled	00	15	-	80	g m <u>e</u> n b	0.015	80	-	600	
Auto Reset Quiescent Current				(ggV)	3 0(9)	set Enable	18			μAde
							0.00		4555	
(Pin 5 is low)	IDDR	10	-	250 500	-	30 82	250 500	-	1500	
		15	-	500		82	500		2000	-
Supply Current**†		7								μAdd
(Dynamic plus Quiescent)		5.0				0.4 µA/kHz)				SIGNATOR
as produced to the same of	ID	10				0.8 µA/kHz)				The last to
-1 707		15	50		ID = (	1.2 µA/kHz)	f + DD			100

<sup>\*</sup>Tlow = -55°C for AL Device, -40°C for CL/CP Device.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

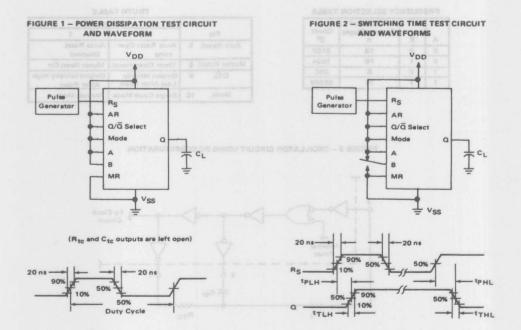
<sup>†</sup>When using the on chip oscillator the total supply current (in  $\mu Adc)$  becomes:  $l_T=l_D+2$   $C_{tc}$   $V_{DD}$  f×10 $^{-3}$  where  $l_D$  is in  $\mu A$ ,  $C_{tc}$  is in pF,  $V_{DD}$  in Volts DC, and f in kHz. (see fig. 3) Dissipation during power-on with automatic reset enabled is typically  $50\mu A$ @  $V_{DD}=10Vdc$ .

SWITCHING CHARACTERISITCS\* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	V <sub>DD</sub>	Min	Typ #	Max	Unit
Output Rise and Fall Time  †TLH, †THL = (1.5 ns/pF) C <sub>L</sub> + 25 ns  †TLH, †THL = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns  †TLH, †THL = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	tTLH, tTHL	5.0 10 15	=	100 50 40	200 100 80	ns.
Propagation Delay, Clock to Q (2 <sup>8</sup> Output) tpLH, tpHL = (1.7 ns/pF) C <sub>L</sub> + 3415 ns tpLH, tpHL = (0.66 ns/pF) C <sub>L</sub> + 1217 ns tpLH, tpHL = (0.5 ns/pF) C <sub>L</sub> + 875 ns		5.0 10 15	-ic	3.5 1.25 0.9	10.5 3.8 2.9	μs -0.1 <sub>22</sub> ft
Propagation Delay, Clock to Q (2 <sup>16</sup> Output) tpHL, tpLH = (1.7 ns/pF) C <sub>L</sub> + 5915 ns tpHL, tpLH = (0.66 ns/pF) C <sub>L</sub> + 3467 ns tpHL, tpLH = (0.5 ns/pF) C <sub>L</sub> + 2475 ns	tPHL tPLH	5.0 10 15	ALL.	6.0 3.5 2.5	18 10 7.5	μs -O E gR
Clock Pulse Width	tWH(cl)	5.0 10 15	900 300 225	300 100 85	=	ns
Clock Pulse Frequency (50% Duty Cycle)	f <sub>cl</sub>	5.0 10 15	=	1.5 4.0 6.0	0.75 2.0 3.0	MHz
MR Pulse Width	twH(R)	5.0 10 15	900 300 225	300 100 85		ns
Master Reset Removal Time	t <sub>rem</sub>	5.0 10 15	420 200 200	210 100 100	_	ns

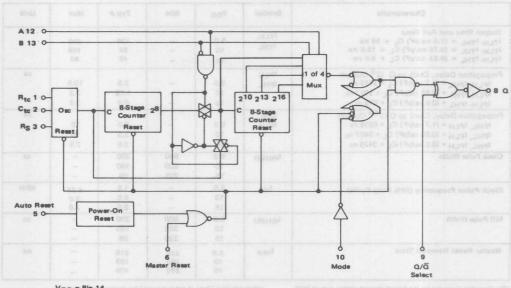
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



## MC14541B

## EXPANDED BLOCK DIAGRAM



V<sub>DD</sub> = Pin 14 V<sub>SS</sub> = Pin 7

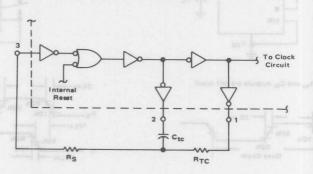
FREQUENCY SELECTION TABLE

A	В	Number of Counter Stages	Count 2n
0	0	13	8192
0	. 1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

1105	RYD	State State					
. Pin		0	# GSA 1				
Auto Reset,	5	Auto Reset Oper- ating	Auto Reset Disabled				
Master Reset, 6		Timer Operational	Master Reset On				
Q/Q,	9	Output Initially Low After Reset	Output Initially High After Reset				
Mode,	10	Single Cycle Mode	Recycle Mode				

FIGURE 3 - OSCILLATOR CIRCUIT USING RC CONFIGURATION



#### TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 - RC OSCILLATOR STABILITY

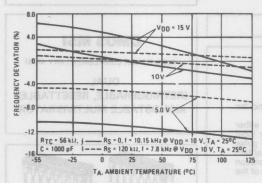
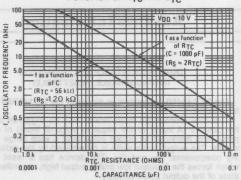


FIGURE 5 - RC OSCILLATOR FREQUENCY AS A FUNCTION OF R<sub>TC</sub> AND C<sub>TC</sub>



#### **OPERATING CHARACTERISTICS**

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a "1" provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3 R_{tc}C_{tc}}$$
 if (1 kHz  $\leq$  f  $\leq$  100 kHz)

and  $R_S \approx 2 R_{tc}$  where  $R_S \ge 10 k\Omega$ 

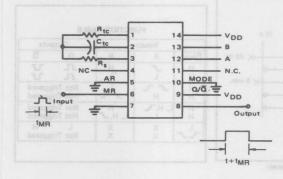
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (28, 210, 213 and 216). The 2<sup>n</sup> counts as shown in the Frequency Selection Table represents the Q output of the N<sup>th</sup> stage of the counter. When A is "1", 216 is selected for both

states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputing 28).

The  $Q/\overline{Q}$  select output control pin provides for a choice of output level. When the counter is in a reset condition and  $Q/\overline{Q}$  select pin is set to a "0" the Q output is a "0", correspondingly when  $Q/\overline{Q}$  select pin is set to a "1" the Q output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop (see Expanded Block Diagram) resets, counting commences, and after 2n-1 counts the RS flip-flop sets which causes the output to change state. Hence, after another 2n-1 counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

### DIGITAL TIMER APPLICATION



When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This "one shot" is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

## MC14548B

## **Advance Information**

#### DUAL MONOSTABLE MULTIVIBRATOR (RETRIGGERABLE, RESETTABLE)

The MC14548B is identical in pinout to the MC14538B and the MC14528B.

This dual monostable multivibrator may be triggered by either the positive (A input) or the negative edge (B input) of an input pulse, and produces an output pulse over a wide range of pulse widths. The output pulse width is determined by the external timing components,  $R_X$  and  $C_X$ . The device has a reset function which forces the Q output low and  $\overline{Q}$  output high, regardless of the state of the output pulse circuitry.

Due to minimal output pulse width variation over temperature, the MC14548 is recommended for new designs in lieu of the MC14528 or MC14538. However, the MC14548 requires more quiescent current than the MC14528 or MC14538.

- Unlimited Rise and Fall Times Allowed on the A Trigger Input
- Output Pulse Width is Independent of the Trigger Pulse Width
- · Latched Trigger and Reset Inputs
- Supply Voltage Range = 3.0 to 18.0 Vdc
- $\bullet$  For pulse widths < 1  $\mu$ s, use the HC4538

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL

(RETRIGGERABLE, RESETTABLE)
MONOSTABLE MULTIVIBRATOR



16/11/11/11

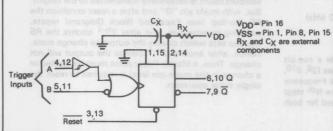
L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

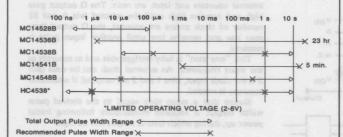
## BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)



#### PIN ASSIGNMENT

Vss	1	16 VDD
CX1/RX1	2	15 VSS
Reset 1	3	14 CX2/RX2
A1 C	4	13 Reset 2
B1 C	5	12 A2
010	6	11 B2
010	7	10 02
VSS C	8	9 02

## ONE-SHOT SELECTION GUIDE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

#### FUNCTION TABLE

	Inputs	30	Out	puts		
Reset	A	В	Q	ā		
H	7	7	T.	7 T		
H	<b>→</b>	5-2		iggered iggered		
H	L, H,~	L, H,		iggered iggered		
~~	X	X	L Not Tr	H		

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter 7 RA	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
In. Iout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

### ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

			V <sub>DD</sub>	Tlo	w*		25°C		Thi	igh*	
Characteristic		Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Uni
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"O" Level	V <sub>OL</sub>	5.0 10 15	-81	0.05 0.05 0.05	_	0 0	0.05 0.05 0.05	( <u>-</u> )01 -	0.05 0.05 0.05	V
$V_{in} = 0 \text{ or } V_{DD}$	"1" Level	VOH	5.0 10 15	4.95 9.95 14.95	-	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	-8.70 -	V
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"O" Level	V <sub>IL</sub>	5.0 10 15	0.0 01 	1.5 3.0 4.0	-	2.25 4.50 6.75	1.5 3.0 4.0	<u>E</u> 10 A	1.5 3.0 4.0	V
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"1" Level	V <sub>IH</sub>	5.0 10 15	3.5 7.0 11.0	- - -	3.5 7.0 11.0	2.75 5.50 8.25		3.5 7.0 11.0	-	V
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	ІОН	5.0 5.0 10 15	-3.0 -0.64 -1.6 -4.2		-2.4 -0.51 -1.3 -3.4	-4.2 -0.88 -2.25 -8.8		-1.7 -0.36 -0.9 -2.4	-	mA
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink	lor	5.0 10 15	0.64 1.6 4.2	-	0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4	197 = 4 100 - - 	mA
Input Current, Pin 2 or 14		l <sub>in</sub>	15	315 01	±0.05	-	± 0.00001	±0.05	-	±0.5	μА
Input Current, Other Inputs	60 50	lin	15	01 01 88	±0.1	-	± 0.00001	±0.1	125 001	±1.0	μА
Input Capacitance, Pin 2 or 1	4	C <sub>in</sub>	-	-5.8 10	70	77-	25	ы жы	o removing	package	pF
Input Capacitance, Other Input (V <sub>in</sub> = 0)	uts	C <sub>in</sub>	- 1	-	-	-	5.0	7.5	- Eul 00	-28 40	pF
Quiescent Current, Standby Sta (AL Devices) (Per Package) $Q = Low, \overline{Q} = High$	ite	IDD	5.0 10 15	=	60 85 110	500	50 75 80	60 85 110	A coll to	170 220 270	μА
Quiescent Current, Standby Sta (CL/CP Devices) (Per Packag $\overline{Q} = \text{Low}, \overline{\overline{Q}} = \text{High}$		IDD	5.0 10 15	=	80 105 130	=	50 75 80	80 105 130	GLOGISTS GOOGLISTS	220 270 370	μА
Quiescent Current, Active State (Per Package)  Q=Low, Q=High	(ALL)	IDD	5.0 10 15	o ho ligus	2.0 2.0 2.0	uo <u>T</u> ets	.04 .08 .13	.20 .45 .70	epiles elde	2.0 2.0 2.0	mA

 $T_{low} = -55$ °C for AL Device, -40°C for CL/CP Device.  $T_{high} = +125$ °C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

			13000	dulav	-	II Types		-
Characte			Symbol	V <sub>DD</sub> Vdc	Min	Тур #	Max	Unit
Output Transition Time	bill abs	Hor yes	tTLH,	5.0	- 1000	100	200	ns
Q or Q			†THL	10	roller), par Pir	50	100	\$0 Jugar
			I want to	15		40	80	O Yesto
Propagation Delay Time	- Nonel	1 2 1 4 1	1.3	5.0		200	400	ns
A or B to Q or Q			tPLH,	10	factor (taken	100	200	wher bas
			THE	15	ness and of manages and	80	160	Mis coults
				Ocean a	A TOTAL monet CVP Miles CV	Characteristics (	FAIRE S	unitered s
Reset to Q or Q				5.0	FOOT most CHIMNET -	185	370	ns
				10	-	90	180	
				15	_	75	150	
nput Pulse Width			t <sub>w(H)</sub> ,	5.0	50	25	_	ns
A, B or Reset			tw(L)	10	30	15	HEY-	10 345
				15	20	10		
1000		25,00		NOT.	1 00V			-
Retrigger Time, To Extend Pu Input A or B ( $C_X$ in $\mu$ f)	ISO		trx	5.0	K <sub>1</sub> C <sub>X</sub>	Total (	CONT. DO	μS
			- 80.0	15	0.75 + V <sub>DD</sub> +K <sub>2</sub> C <sub>X</sub>	love/ "g"		wastio
$K_1 = 2000 \left(\frac{V}{\mu F}\right)$ , $K_2 = 13 \left(\frac{V}{\mu F}\right)$			- 20.0		00 2 - 2			VOD OF
Retrigger Time, To Issue New	Pulse	- 4	trr	5.0	0	_	-	ns
Input A or B	-		8.8 1 -	10	0.0	fand T. June	-	
			2.0	15	0 0	_	-	00 P to 0
Recovery Time			trec	5.0	20	11.6		ns
Reset Inactive to A or B			190	10	10	4.8	-	Olon A A
			1 000	15	6	3.0		0 0 0 B
	NAME OF	20.00					- 100 V M	10000
nput Rise and Fall Time			t <sub>r</sub> , t <sub>f</sub>	5.0	-	-	15	μѕ
Reset			10	10 15		Ibash	5	J. Can
				13	1 08 1 - 1		107 / 10	0.0
B Input			The L	5.0	1 at 1 = 1	286	200	1000
S input				10		40	25	1000
				15	1 -101 -1	22	15	rive Out
A Input			15-	5.0	1 9.8	SELECTION .	- 18	V 9-5 v
- 35.0-			10	10	100	No Limit		3 1 9 2 3
- 8.Q-		#5.S 13		15	04		- 9	8 ( 2 8 -
Output Pulse Width — Q or C	1		т	5.0	9	12.6	15	μs
$C_X = 0.001 \mu F R_X = 10 k\Omega$			8.0	10	8 8	11.8	14	DA VO
				15	8	11.0	14	6 V 3.G
$C_X = 0.01 \mu F R_X = 10 k\Omega$				5.0	82	90	100	μs
			- 80.0	10	69	77	85	
				15	61	73	80	rent, Pip
$C_X = 1.0 \mu F R_X = 100 k\Omega$			- 10	5.0	64	71	78	ms
				10	62	68	75	diam'r.
				15	62	68	75	111101
Pulse Width Match between o	ircuits in		T1 - T2	5.0	-12	± 1	E 10 1_119.	%
the same package			T1	10	-	±1	_	
$C_X = 0.1 \mu F R_X = 100 k\Omega$				15	_	±1		

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

#### **OPERATING CONDITIONS**

External Timing Resistance	RX	- 1	5.0	-	1	kΩ
External Timing Capitance	Cv	-	0			DF

The maximum allowable values of R<sub>X</sub> and C<sub>X</sub> are a function of the leakage of capacitor C<sub>X</sub>, the leakage of the MC14548B, and leakage due to board layout and surface resistance. Values of R<sub>X</sub> and C<sub>X</sub> should be chosen so that the maximum current into pin 2 or pin 14 is 10 mA. Susceptibility to externally induced noise signals may occur for R<sub>X</sub> > 1 MΩ.

A1, A2 (Pins 4, 12) - Positive-edge trigger inputs. A rising-edge signal on either of these pins will trigger the corresponding multivibrator when there is a high voltage level on the B1 or B2 input.

B1, B2 (Pins 5, 11) - Negative-edge trigger inputs. A falling-edge signal on either of these pins will trigger the corresponsing multivibrator when there is a low voltage level on the A1 or A2 input.

Reset 1, Reset 2 (Pins 3, 13) - Reset inputs (active low). When a low voltage is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low voltage and the Q output is set to a high voltage.

Cx1/Rx1 and Cx2/Rx2 (Pins 2 and 14) - External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram).

#### OUTPUTS

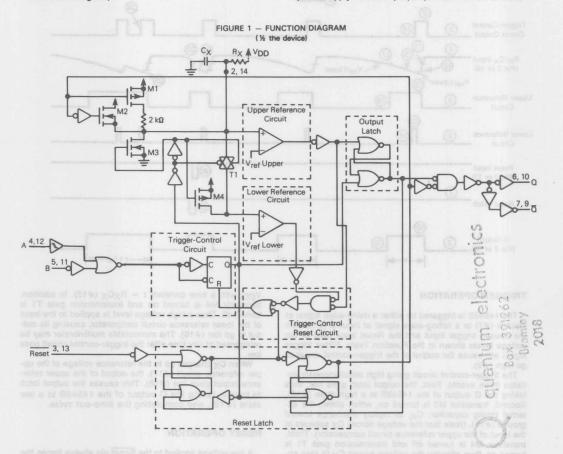
Q1. Q2 (Pins 6,10) - Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, Rx and Cx.

Q1, Q2 (Pins 7, 9) — Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

Vpp (Pin 16) - Most positive supply potential. This voltage may range from 3 to 18 volts with respect to VSS.

VSS (Pins 1, 8, 15) - Most negative supply potential (usually ground).

NOTE: All 3 pins must be connected externally to the power supply to insure proper performance.



#### CIRCUIT OPERATION

Figure 4 shows the 14548B configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 1). In the quiescent state, the external timing capacitor, Cx, is charged to VDD. When a trigger occurs, the Q output goes high and Cx discharges quickly to the lower reference voltage ( $V_{ref}$  Lower  $\approx$  1/3  $V_{DD}$ ). C $\chi$  then charges, through Rx, back up to the upper reference voltage (Vref Upper ≈ 2/3 VDD), at which point the one-shot has timed out and the Q output goes low.

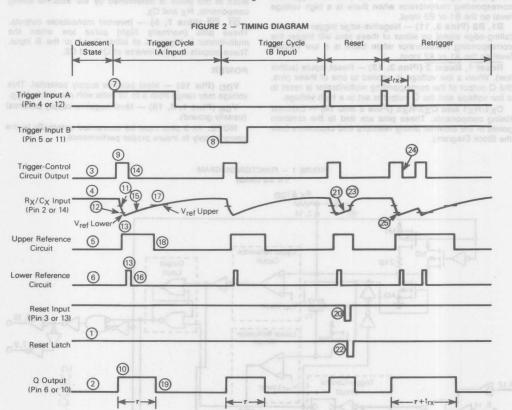
The following, more detailed description of the circuit operation refers to both the function diagram (Figure 1) and the timing diagram (Figure 2).

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 2). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 2).

The output of the trigger-control is low (#3), and transistors M1, M2, and M3 are turned off. The external timing

capacitor,  $C\chi$ , is charged to  $V_{DD}$  (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and transmission gate T1 is turned off. Thus the lower reference circuit has  $V_{DD}$  at the noninverting input and a resulting low output (#6).

In addition, the output of the trigger-control reset circuit is low.



#### TRIGGER OPERATION

The 14548B is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus taking the Q output of the 14548B to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, Cx, to rapidly discharge toward ground (#11). (Note that the voltage across Cx appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across Cx to also appear at the input of the lower reference circuit comparator.

When C<sub>X</sub> discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flipflop to a low state (#14). This turns transistor M3 off again, allowing C<sub>X</sub> to begin to charge back up toward

VDD, with a time constant  $t=R\chi C\chi$  (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low

When  $C\chi$  charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the 14548B to a low state (#19), and completing the time-out cycle.

#### RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the 14548B to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while  $C_X$  is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus  $C_X$  is allowed to quickly charge up to  $V_{DD}$  (#23) to await the next trigger signal.

#### RETRIGGER OPERATION

When used in the retriggerable mode (Figure 4), the MC14548B may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after  $C_X$  has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time,  $t_{\rm TX}$  (Figure 1) is a function of internal propagation delays and the discharge time of  $C_X$ .

Figure 5 shows the device configured in the non-trigger-

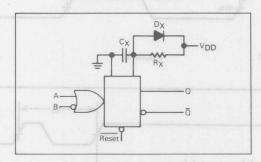
#### POWER-DOWN CONSIDERATIONS

Large values of Cx may cause problems when powering down the 14548B because of the amount of energy stored

in the capacitor. When a system containing this device is powered down, the capacitor may discharge from  $V_{DD}$  through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 10 mA, therefore, the turn-off time of the  $V_{DD}$  power supply must not be faster than  $t=V_{DD}\bullet C\chi/(10$  mA). For example, if  $V_{DD}=5$  V and  $C\chi=15$   $\mu F$ , the  $V_{DD}$  supply must turn off no faster than  $t=(5\ V)\bullet(15\ \mu F)/10$  mA = 7.5 ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V<sub>DD</sub> to zero volts occurs, the MC14548B may sustain damage. To avoid this possibility, use an external clamping diode, D<sub>X</sub>, connected as shown in Figure 3.

FIGURE 3 — DISCHARGE PROTECTION DURING POWER DOWN



TYPICAL APPLICATIONS

FIGURE 4 - RETRIGGERABLE MONOSTABLE CIRCUITRY

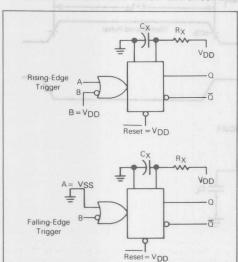
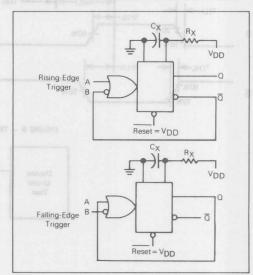
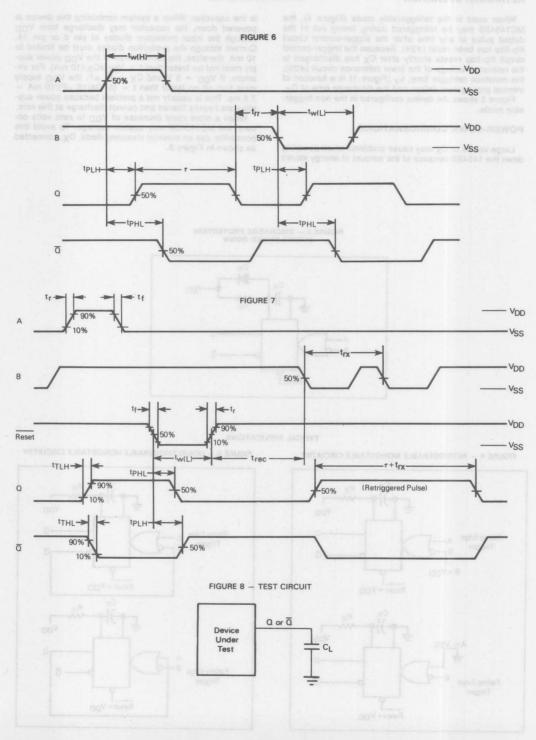


FIGURE 5 - NONRETRIGGERABLE MONOSTABLE CIRCUITRY



#### SWITCHING WAVEFORMS



#### ANALOG MULTIPLEXER/DEMULTIPLEXER

The MC14551B is a digitally-controlled analog switch. This device implements a 4PDT solid state switch with low ON impedance and very low OFF Leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V<sub>DD</sub>-V<sub>EE</sub>) = 3 to 18 V
   Note: V<sub>EE</sub> must be ≤ V<sub>SS</sub>
- Linearized Transfer Characteristics
- Low Noise 12 nV/ √Cycle, f ≥ 1 kHz typical
- For Lower R<sub>ON</sub>, Use The HC4051, HC4052, or HC4053 High-Speed CMOS Devices

#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage (Referenced to V <sub>EE</sub> , V <sub>SS</sub> ≥ V <sub>EE</sub> )	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient) (Referenced to V <sub>SS</sub> for Control Input & V <sub>EE</sub> for Switch I/O)	-0.5 to V <sub>DD</sub> +0.5	٧
lin	Input Current (DC or Transient), per Control Pin	± 10	mA
Isw	Switch Through Current	± 25	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
Z-TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXER/ DEMULTIPLEXER



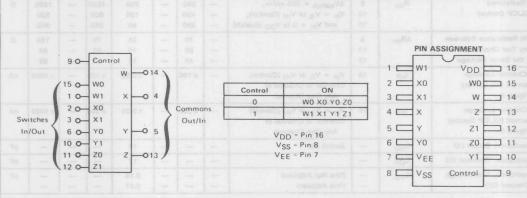
L SUFFIX
CERAMIC PACKAGE

P SUFFIX
PLASTIC PACKAGE

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



Note: Control Input referenced to  $V_{SS}$ , Analog Inputs and Outputs reference to  $V_{EE}$ .  $V_{EE}$  must be  $\leqslant V_{SS}$ .

				Tie	ow"	THE R	25°C		Thi	gh"	1
Characteristic	Symbol	VDD	Test Conditions	Min	Max	Min	Тур#	Max	Min	Max	Unit
SUPPLY REQUIREME	NTS (Voltages	Refere	nced to V <sub>EE</sub> )								
Power Supply Voltage Range	V <sub>DD</sub>	-	V <sub>DD</sub> -3 > V <sub>SS</sub> > V <sub>EE</sub>	3	18	3	-	18	3	18	V
Quiescent Current Per Package (AL Device)	IDD	5 10 15	Control Inputs: $V_{\text{in}} = V_{\text{SS}} \text{ or } V_{\text{DD}}$ , Switch I/O: $V_{\text{EE}} \le V_{\text{I/O}} \le V_{\text{DD}}$ , and $\Delta V_{\text{switch}} \le 500 \text{ mV**}$	Lmiii —	5 10 20	DES.	0.005 0.010 0.015	5 10 20	AHTA —	150 300 600	μА
Quiescent Current Per Package (CL/CP Device)	IDD	5 10 15	Control Inputs: $V_{in} = V_{SS} \text{ or } V_{DD}$ , Switch I/O: $V_{EE} \le V_{I/O} \le V_{DD}$ , and $\Delta V_{switch} \le 500 \text{ mV**}$	PIC V BIC V BITER	20 40 80	130m 1070m 1070m	0.005 0.010 0.015	20 40 80	4 T pla 4653 3 10050 X	150 300 600	μА
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	81 0	Ту	pical	(0.07 μA/k (0.20 μA/k (0.36 μA/k	Hz)f +	DD	e Su	μА
CONTROL INPUT (Volta	ages Reference	ed to Vs	s)	OLC	1947	uq	A sala	ouraniu-	all tal	100	
Low-Level Input Voltage	VIL	5 10 15	R <sub>on</sub> = per spec, l <sub>off</sub> = per spec		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0	eallize V <u>N</u> ois	1.5 3.0 4.0	V
High-Level Input Voltage	VIH	5 10 15	R <sub>on</sub> = per spec, l <sub>off</sub> = per spec	3.5 7.0 11.0	10 <u>14</u> (1	3.5 7.0 11.0	2.75 5.50 8.25	1001	3.5 7.0 11.0	MO_ W	V
Input Leakage Current (AL Device)	lin	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	-	±0.1	_	±0.00001	±0.1	-	±1.0	μА
Input Leakage Current (CL/CP Device)	lin	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	-	±0.3		±0.00001	±0.3	-	±1.0	μА
Input Capacitance	Cin	-	V 0.87 × 0/0 0	-	198	0.00	5.0	7.5	graphic .	0010	pF
SWITCHES IN/OUT A	ND COMMO	NS O	UT/IN - W, X, Y, Z (Voltages I	Referen	nced to	VEE)	u OC) seen	No march	O to to	user law	Vield
Recommended Peak-to- Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	E A	Channel On or Off	0	V <sub>DD</sub>	0	s 10v <u>C</u> onus or Trucsion	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>p-l</sub>
Recommended Static or Dynamic Voltage Across the Switch** (Figure 3)	ΔV <sub>switch</sub>	1 (0	Channel On	0	600	0		600	0	300	m\
Output Offset Voltage	V00	-	V <sub>in</sub> = 0 V, No load	-	750	-	10	F11/1016	gra <del>dí</del> t	10.1	μV
ON Resistance (AL Device)	Ron	5 10 15	$\Delta V_{\text{switch}} \leq 500 \text{ mV**},$ $V_{\text{in}} = V_{\text{IL}} \text{ or } V_{\text{IH}} \text{ (Control)},$ and $V_{\text{in}} = 0 \text{ to } V_{\text{DD}} \text{ (Switch)}$	1 o → p no.1 0 on_2 v	800 400 220	61-6 	250 120 80	1050 500 280	91—19 9142-19	1300 550 320	Ω
ON Resistance (CL/CP Device)	R <sub>on</sub>	5 10 15	$\Delta V_{\text{switch}} \le 500 \text{ mV**},$ $V_{\text{in}} = V_{\text{IL}} \text{ or } V_{\text{IH}} \text{ (Control)},$ and $V_{\text{in}} = 0 \text{ to } V_{\text{DD}} \text{ (Switch)}$		880 450 250		250 120 80	1050 500 280	=	1200 520 300	Ω
Any Two Channels in the Same Package	ΔR <sub>on</sub>	5 10 15			70 50 45		25 10 10	70 50 45	-	135 95 65	Ω
Off-Channel Leakage Current (AL Device) (Figure 8)	loff	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	-	± 100	Name of the last	±0.05	± 100	-0 ar	±1000	nA
Off-Channel Leakage Current (CL/CP Device) (Figure 8)	loff	15	V <sub>In</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	-	±300	1	±0.05	±300	2.0- 3.0- 6.0-	± 1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	-	Switch Off	_	-	_	10	121	-Q_01	-	pF
Capacitance, Common O/I	C <sub>O/I</sub>	-	1 617 133 V	_	_	-	17	-	-	-	pF
	-				-				-0.55		-

<sup>\*</sup>  $T_{low} = -55$ °C for AL Device, -40° for CL/CP Device.

Capacitance, Feedthrough

(Channel Off)

C1/0

Pins Not Adjacent

Pins Adjacent

0.15

0.47

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>For voltage drops across the switch ( $\Delta V_{switch}$ ) >600 mV (>300 mV at high temperature), excessive  $V_{DD}$  current may be drawn; i.e. the current out of the switch may contain both VDD and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (C. = 50 pF Ta = 25°C Ver & Vec

Characteristic	Symbol	VDD-VEE	Min	Тур #	Max	Unit
Propagation Delay Times Switch Input to Switch Output ( $R_L=10~k\Omega$ ) $t_{PLH},~t_{PHL}=(0.17~ns/pF)~C_L+26.5~ns$ $t_{PLH},~t_{PHL}=(0.08~ns/pF)~C_L+11~ns$ $t_{PLH},~t_{PHL}=(0.06~ns/pF)~C_L+9.0~ns$	tpLH, tpHL	5.0 10 15	E	35 15 12	90 40 30	ns
Control Input to Output (R <sub>L</sub> = 10 kΩ) VEE = VSS (Figure 4)	tPLH, tPHL	5.0 10 15		350 140 100	875 350 250	ns
Second Harmonic Distortion R <sub>L</sub> =10 kΩ, f=1 kHz, V <sub>in</sub> =5 V <sub>p-p</sub>	part .	10	M-1	0.07	-	%
Bandwidth (Figure 5) $R_L = 1 \text{ k}\Omega, \text{ V}_{in} = 1/2 \text{ (V}_{DD} - \text{V}_{EE}) \text{ p-p}.$ $20 \text{ Log } \frac{\text{V}_{out}}{\text{V}_{in}} = -3 \text{ dB, C}_L = 50 \text{ pF}$	BW	10		17 35V	-	MHz
Off Channel Feedthrough Attenuation, Figure 5 R <sub>L</sub> = 1 k $\Omega$ , V <sub>in</sub> = 1/2 (V <sub>DD</sub> - V <sub>EE</sub> ) p-p, $f_{in}$ = 55 MHz	-	10		- 50	- 1	dB
Channel Separation (Figure 6) R <sub>L</sub> = 1 k $\Omega$ , V <sub>In</sub> = 1/2 (V <sub>DD</sub> - V <sub>EE</sub> ) p-p, $f_{\text{in}}$ = 3 MHz	Oint	10	_	- 50	lon <del>m</del> a3	dB
Crosstalk, Control Input to Common O/I, Figure 7 R1 = 1 k $\Omega$ , R <sub>L</sub> = 10 k $\Omega$ , Control t <sub>r</sub> = t <sub>f</sub> = 20 ns	-	10	1	75	-	mV

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$  for control inputs and  $V_{EE} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$  for Switch I/O.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS, VEE, or VDD). Unused outputs must be left open.

FIGURE 1 - SWITCH CIRCUIT SCHEMATIC Secure Input to Switch Capper (Fig. # 10 PG)

Switch Input to Switch Capper (Fig. # 10 PG)

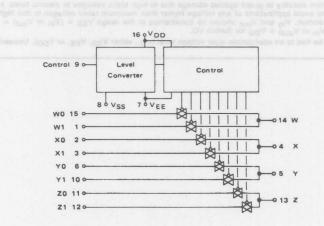
Spitch Spitch (IO.09 no.ph) Ci. + 17 na.

Spitch Spitch (IO.09 no.ph) Ci. + 17 na.

Spitch Spitch (IO.09 no.ph) Ci. + 17 na.

Codest Input to Capper (IO.09 no.ph) Ci. + 10 pt. VDD VDD VDD + VDD Out/In II 4 In/Out o--~~ ≈ 10Ω  $\approx 10\Omega$ VEE 4-9 (3-27 - 00/0 5/4 - NV . D.S. 1 - 1/2 VEE LI VDD . Control In/Out O-Control VEE

FIGURE 2 - MC14551B FUNCTIONAL DIAGRAM



## TEST CIRCUITS



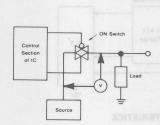


FIGURE 4 — PROPAGATION DELAY TIMES, CONTROL TO OUTPUT

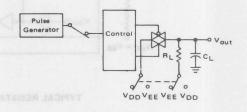


FIGURE 5 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

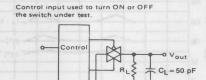




FIGURE 6 — CHANNEL SEPARATION (Adjacent Channels Used for Setup)

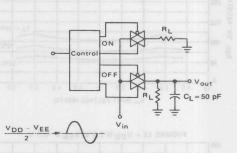


FIGURE 7 — CROSSTALK, CONTROL INPUT TO COMMON O/I

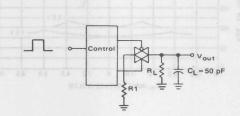
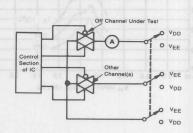
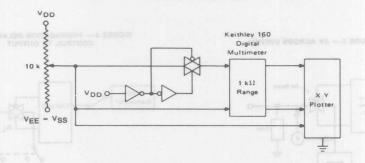


FIGURE 8 - OFF CHANNEL LEAKAGE

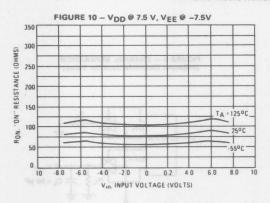


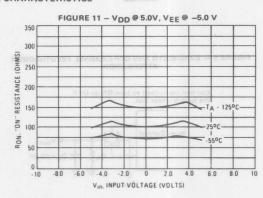
.

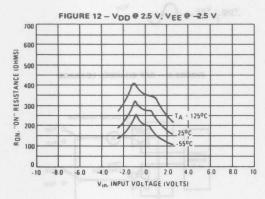
FIGURE 9 - CHANNEL RESISTANCE (RON) TEST CIRCUIT

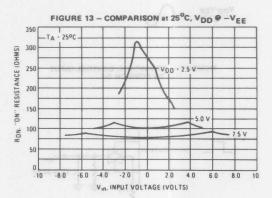


### TYPICAL RESISTANCE CHARACTERISTICS









## APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figure 2. The 0-to-5 volt Digital Control signal is used to directly control a 9  $V_{p-p}$  analog signal.

The digital control logic levels are determined by  $V_{DD}$  and  $V_{SS}$ . The  $V_{DD}$  voltage is the logic high voltage; the  $V_{SS}$  voltage is logic low. For the example,  $V_{DD} = +5 \text{ V} = \text{logic high at the control inputs; } V_{SS} = \text{GND} = 0 \text{ V} = \text{logic low.}$ 

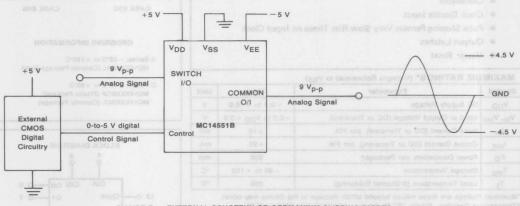
The maximum analog signal level is determined by VDD and VEE. The VDD voltage determines the maximum recommended peak above VSS. The VEE voltage determines the maximum swing below VSS. For the example, VDD - VSS = 5 volt maximum swing above VSS; VSS - VEE = 5 volt maximum swing

below VSS. The example shows a  $\pm 4.5$  volt signal which allows a 1/2 volt margin at each peak. If voltage transients above VDD and/or below VEE are anticipated on the analog channels, external diodes  $(D_X)$  are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

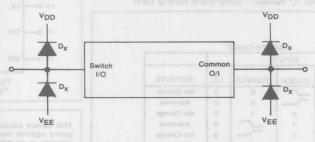
The absolute maximum potential difference between VDD and VEE is 18.0 volts. Most parameters are specified up to 15 volts which is the recommended maximum difference between VDD and VEE.

Balanced supplies are not required. However, VSS must be greater than or equal to VEE. For example,  $V_{DD} = +10$  volts,  $V_{SS} = +5$  volts, and  $V_{EE} = -3$  volts is acceptable. See the table below.

#### FIGURE A - APPLICATION EXAMPLE



#### FIGURE B — EXTERNAL SCHOTTKY OR GERMANIUM CLIPPING DIODES



#### POSSIBLE SUPPLY CONNECTIONS

V <sub>DD</sub> In Volts	V <sub>SS</sub> V <sub>EE</sub> in Volts		Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range in Volts			
+8	0	-8	+8/0	+8 to -8 = 16 V <sub>p-p</sub>			
+5	um alugius be	12 N V	+5/0	+5 to -12 = 17 V <sub>p-p</sub>			
+5	0	0	+5/0 +5 to 0 = 5				
+5	0	-5	-5 +5/0 +				
+10	+5	-5	+10/+5	$+10 \text{ to } -5 = 15 \text{ V}_{p-p}$			

## MC14553B

#### THREE-DIGIT BCD COUNTER

The MC14553B three-digit BCD counter consists of three negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Compatible Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

#### MAXIMUM RATINGS\* (Voltages Referenced to Vss)

Symbol	Parameter	Value	Unit	
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧	
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧	
In -	Input Current (DC or Transient), per Pin	±10	mA	
lout	Output Current (DC or Transient), per Pin	+ 20	mA	
PD	Power Dissipation, per Package†	500	mW	
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C	
TL	Lead Temperature (8-Second Soldering)	260	°C	

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/"C from 65°C to 85°C
Ceramic "L" Package: -12mW/"C from 100°C to 125°C

#### TRUTH TABLE

MASTER RESET	CLOCK	DISABLE	LE	OUTPUTS			
0	5	0	0	No Change			
0	_	0	0	Advance			
0 X		1	×	No Change			
0	1		0	Advance			
0	1		0	No Change			
0	0	×	×	No Change			
0	×	×	5	Latched Latched			
0	×	×	1				
eng 1 gold plick r	×	×	0	Q0 = Q1 = Q2 = Q3 = 0			

X = Don't Care

## CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

THREE-DIGIT BCD COUNTER

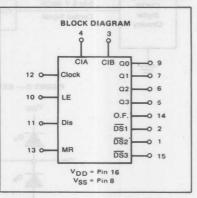


L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

Min Typ # Meax Gall	1994	VDD	T <sub>low</sub> *			25°C	olista	Thigh*		1
Characteristic	Symbol	Vdc	Min	Max	Min	Тур #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	10 TRava	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0		10	-	0.05	_	0	0.05	O Flines	0.05	
		15	-	0.05	-	0	0.05	O Page	0.05	
"1" Level	VOH	5.0	4.95		4.95	5.0	-	4.95	_	
V <sub>in</sub> =0 or V <sub>DD</sub>	.Оп	10	9.95	43.	9.95	10		9.95	IVO	
0001 000		15	14.95	_	14.95	15		14.95	-	
nput Voltage "0" Level	VIL					-	-		-	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	9:8	5.0	HIP-	1.5	-	2.25	1.5	_	1.5	
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	-	3.0	-	4.50	3.0	_	3.0	
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	-	4.0	_	6.75	4.0	_	4.0	
"1" Level	VIH		le qf	01					NO	
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	0.8	5.0	3.5	_	3.5	2.75	_	3.5	-	
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	_	7.0	5.50	_	7.0	-	
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	700	11.0	8.25	Total S	11.0	- T	
Output Drive Current (AL Device)	ІОН					eini	Batus	udenii ii	HELL OF	mAd
(VOH = 4.6 Vdc) Source - Pin 3	15	5.0	-0.25	_	-0.20	-0.36	_	0.14	_	
(Vou=9.5 Vdc)		10	-0.62	-	-0.50	-0.9	_	0.35	-	
(V <sub>OH</sub> = 13.5 Vdc)		15	-1.8	0.5	- 1.5	-3.5	_	1.1	0.70	
(VOH=4.6 Vdc) Source - Other		5.0	-0.64	_	-0.51	-0.88	_	-0.36	_	
(VOH = 9.5 Vdc) Outputs		10	-1.6		-1.3	-2.25	_	-0.9	_	
(VOH = 13.5 Vdc)		15	-4.2	45	-3.4	-8.8	_	-2.4	Attitute	
(V <sub>OL</sub> = 0.4 Vdc) Sink - Pin 3	loL	5.0	0.5	_	0.4	0.88	_	0.28	_	
(V <sub>OL</sub> =0.5 Vdc)	·OL	10	1.1		0.9	2.25		0.65	_	
(V <sub>OL</sub> = 1.5 Vdc)		15	1.80	100	1.5	8.8	_	1.20	ritelly	
(VoL = 0.4 Vdc) Sink - Other Outputs		5.0	3.0	_	2.5	4.0	_	1.6	_	
(V <sub>OL</sub> = 0.5 Vdc)		10	6.0	_	5.0	8.0		3.5	_	
(V <sub>OL</sub> = 1.5 Vdc)		15	18	_	15	20		10	em <u>at</u> la	
Output Drive Current (CL/CP Device)	ГОН							- 11		mAd
(V <sub>OH</sub> =4.6 Vdc) Source - Pin 3	·On	5.0	-0.2	_	-0.16	-0.36		-0.12		
(V <sub>OH</sub> =9.5 Vdc)		10	-0.5	_	-0.4	-0.9	_	-0.3	rio <u>up</u> si	
(V <sub>OH</sub> = 13.5 Vdc)		15	-1.4	_	-1.2	-3.5	_	-1.0	_	
(VOH = 4.6 Vdc) Source-Other Outputs		5.0	-0.52	_	-0.44	0.88		-0.36	_	
(V <sub>OH</sub> =9.5 Vdc)		10	-1.3	_	-1.1	-2.25	_	-0.9	m12-20	
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	_	-3.0	-8.8		-2.4	_	
(V <sub>OL</sub> = 0.4 Vdc) Sink - Pin 3	loL	5.0	0.23	_	0.2	0.88		0.16	_	
(V <sub>OL</sub> = 0.5 Vdc)		10	0.60	_	0.5	2.25	_	0.40		
(V <sub>OL</sub> = 1.5 Vdc)		15	1.80	_	1.5	8.8	_	1.20	L THE	
(V <sub>OL</sub> = 0.4 Vdc) Sink - Other Outputs		5.0	2.4	_	2.0	4.0	_	1.6	_	
(V <sub>OL</sub> = 0.5 Vdc)		10	3.8	-	3.0	8.0		2.5		
(V <sub>OL</sub> = 1.5 Vdc)		15	10	_	8.4	20	_	7.0	_	
Input Current (AL Device)	l <sub>in</sub>	15	_	± 0.1	-	± 0.00001	± 0.1	_	±1.0	μAd
Input Current (CL/CP Device)	lin	15	-	±0.3	_	±0.00001	±0.3	_	±1.0	μAd
Input Capacitance	C <sub>in</sub>	_	-		_	5.0	7.5	_		pF
(V <sub>in</sub> = 0)	Jin					0.0			14. 1	Pr
Quiescent Current (AL Device)	IDD	5.0	-	5.0	_	0.010	5.0	_	150	μΑσ
(Per Package)	00	10	_	10	_	0.020	10	_	300	
MR=V <sub>DD</sub>		15	-	20	_	0.030	20	_	600	
Quiescent Current (CL/CP Device)	IDD	5.0	_	50	_	0.010	50	_	375	μAd
(Per Package)	.00	10	_	100	_	0.020	100	_	750	p., 10
MR = V <sub>DD</sub>		15	_	200	_	0.030	200	_	1500	
Total Supply Current**†	1-	5.0			l== (0.1	35 μA/kHz)				μΑσ
(Dynamic Plus Quiescent,	lΤ	10				35 μA/kHz)				μΑ
Per Package)		15				50 μA/kHz)			100	
(C <sub>L</sub> = 50 pF on all outputs,						,	UU			
all buffers switching)										

 $<sup>^*</sup>T_{low} = -55^\circ\text{C}$  for AL Device,  $-40^\circ\text{C}$  for CL/CP Device.  $T_{high} = +125^\circ\text{C}$  for AL Device,  $+85^\circ\text{C}$  for CL/CP Device.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS (CL = 50 pF. TA = 25°C)

"nd	Characte	eristic	0.45		Figure	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time TTLH, TTHL=(1.5 ns/pF) CL+25 ns TTLH, TTHL=(0.75 ns/pF) CL+12.5 ns TTLH, TTHL=(0.55 ns/pF) CL+9.5 ns					2a	t <sub>TLH</sub> ,	5.0 10 15	_ lovis.	100 50 40	200 100 80	ns
Clock to BCD Out	4.26 9.96 14.95		0.8 -0.1 -8.9	30. 30.	2a	tPLH,	5.0 10 15	E	900 500 200	1800 1000 400	ns
Clock to Overflow	-	8 7 . 0.6 0.4	9.25 4.50 8.25		2a	tPHL 0.8	5.0 10 15	=	600 400 200	1200 800 400	ns
Reset to BCD Out	2.E 0.5		27/5 68/8	8.1	2b	tPHL a.s. d.e.	5.0 10 15	- 1978 -	900 500 300	1800 1000 600	ns
Clock to Latch Enable Master Reset to Latc			Time	0.0	2b	tsu	5.0 10 15	600 400 200	300 200 100	26 13 6 V 2 C=unt 6 V(△) 2	ns
Removal Time Latch Enable to Cle	ock		- 0.9 - 0.5 - 0.86	2 d d d d d d d d d d d d d d d d d d d	2b	trem	5.0 10 15	-80 -10 0	-200 -70 -50	3.6 V <u>o</u> v 8	ns
Clock Pulse Width	6.0 6.3 6.20	-	8.8 - 89.0	4.8	2a	tWH(cl)	5.0 10 15	550 200 150	275 100 75	(100 to 100)	ns
Reset Pulse Width	08.1 08.1		0.6	2.5	2b	tWH(R)	5.0 10 15	1200 600 450	600 300 225	US CENT A	ns
Reset Removal Time	01	-	09	- 6	-	ar trem an	5.0 10 15	- 80 0 20	- 180 - 50 - 30	S Viet	ns
Input Clock Frequenc	0.1-	-	8.0 - 8.6 -	5.0	2a	o fel at	5.0 10 15	=	1.5 5.0 7.0	0.9 2.5 3.5	МН
Input Clock Rise Tim	9.0- 2.2-		88.0	6.0	2b	tTLH ar	5.0 10 15		No Limit	b Vac) Lb Vac) 4 Vac)	ns
Scan Oscillator Frequ (C1 measured in μ			8.05	3.0	1	fosc	5.0 10 15	=	1.5/C1 4.2/C1 7.0/C1	5 V4 <u>0</u> 2 5 V4 <u>0</u> 2	Hz

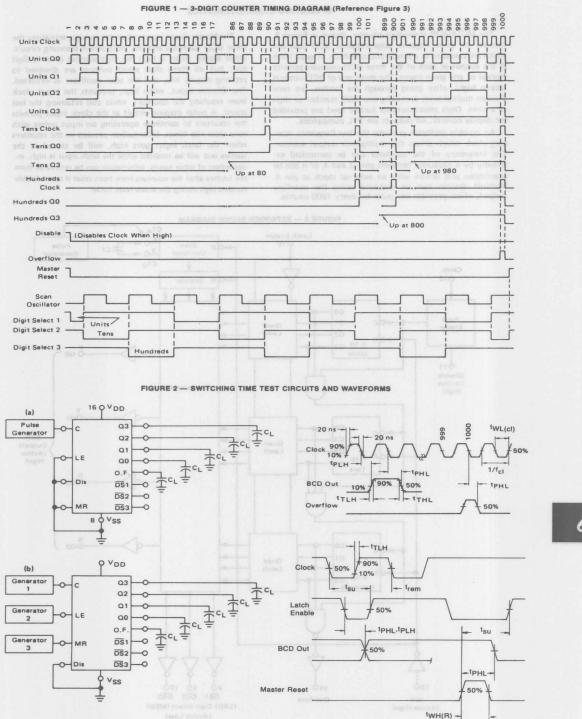
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

₱Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

6-400

# MC14553B

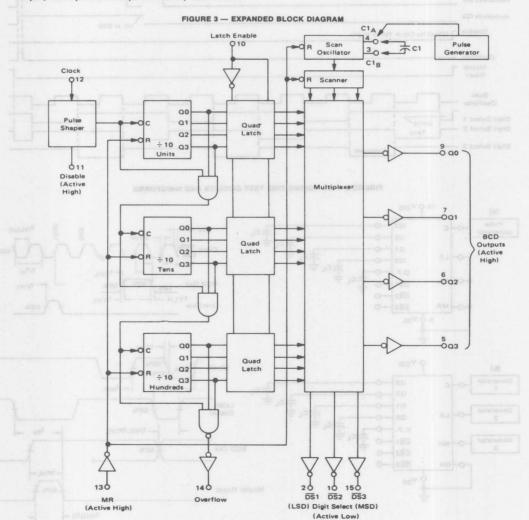


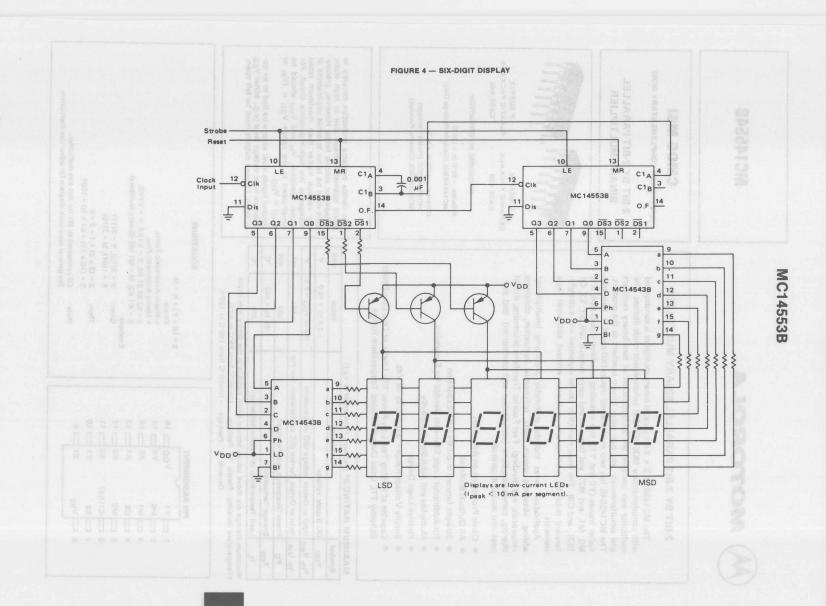
### **OPERATING CHARACTERISTICS**

The MC14553B three-digit counter, shown in Figure 3, consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.





# MC14554B

### 2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

The MC14554B 2 x 2-bit parallel binary multiplier is constructed with complementary MOS (CMOS) enhancement mode devices. The multiplier can perform the multiplication of two binary numbers and simultaneously add two other binary numbers to the product. The MC14554B has two multiplicand inputs (X0 and X1), two multiplier inputs (Y0 and Y1), five cascading or adding inputs (K0, K1, M0, M1, and M2), and five sum and carry outputs (S0, S1, S2, C1 [S3], and C0). The basic multiplier can be expanded into a straightforward m-bit by n-bit parallel multiplier without additional logic elements

Application areas include arithmetic processing (multiplying/adding, obtaining square roots, polynomial evaluation, obtaining reciprocals, and dividingly, Fast Fourier Transform processing, digital filtering, communications (convolution and correlation), and process and machine controls.

- Diode Protection on All Inputs
- All Outputs Buffered
- Straight-forward m-Bit By n-Bit Expansion
- No Additional Logic Elements Needed for Expansion
- Multiplies and Adds Simultaneously
- Positive Logic Design
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS\* (Voltages Referenced to Voc)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C
Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

PIN ASSIGNMENT VDD 16 YOL MO \_\_\_ 15 M1 X0 \_\_\_\_ 14 CO X1 13 M2 K0 12 C1[S3] SO 11 52 K1 10 7 = 8 [ VSS S1 19

### EQUATIONS

 $S = (X \times Y) + K + M$ 

Where:

x Means Arithmetic Times.
+ Means Arithmetic Plus.

S = S3 S2 S1 S0, X = X1X0, Y = Y1Y0,

S = 53 52 51 50, X = X1X0, Y = Y1Y0, K = K1 K0, M = M1 M0 (Binary Numbers).

Example:

Given: X = 2(10), Y = 3(11)

K = 1(01), M = 2(10)

Then:  $S = (2 \times 3) + 1 + 2 = 9$  $S = (10 \times 11) + 01 + 10 = 1001$ 

Note: C0 connected to M2 for this size multiplier.

See general expansion diagram for other size multipliers.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to Vss)

	nilit	VDD	Tio	w		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0	-	0.05	-	0	0.05	h (adirent)	0.05	Vdc
$V_{in} = V_{DD}$ or 0	77	10	1	0.05	-	0	0.05	(Piquetr at	0.05	HUTT
08 05	7 1	15	-	0.05	-	0	0.05	(Fig gin di	0.05	HEATT?
"1" Level	VOH	5.0	4.95	4.191	4.95	5.0	-	4.95	shiO_no-t	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	On	10	9.95	191915	9.95	10		9.95	50 c	33
270 675	-	15	14.95	-	14.95	15	JOJE Ray	14.95	M97.41.15	
Input Voltage "0" Level	VIL	W.				18 X8 ±	OF CHARLIE	00.01 ×	H92, H29	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	-	5.0		1.5		2.25	1.5	(Q.5 e)	15	1
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$		10		3.0	-	4.50	3.0	-	3.0	OM.
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	100	15	- 1	4.0		6.75	4.0	n (1.7 n	4.0	
"1" Level	VIH	100				437 3 702 7	Don a getting	100.00	PLH, VPIS	
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	- 44	5.0	3.5		3.5	2.75	LID (Flah	3.5	Maj HTa	Vdc
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$		10	7.0	- 0	7.0	5.50	to be read a	7.0	ovio-asken	ot onT
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25		11.0	-	-
Output Drive Current (AL Device)	ГОН				111111111111111111111111111111111111111	ord regions is	it topper out	of took of "a	ST PRINCE	mAdc
(V <sub>OH</sub> = 25 Vdc) Source	·Un	5.0	-3.0		-2.4	-4.2	and in case and	-1.7	mi no se bo	Interest.
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88		-0.36	- 1	
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6		-1.3	-2.25		-0.9		
(VOH = 13.5 Vdc)		15	-4.2		-3.4	-8.8	_	-2.4		
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	_	0.36	-	mAdc
(V <sub>OL</sub> = 0.5 Vdc)	·OL	10	1.6		1.3	2.25		0.9		IIIAGC
(VOI = 1.5 Vdc)	Mark S	15	4.2	-	3.4	8.8	ANDIG PO	2.4	anuars	
Output Drive Current (CL/CP Device)	lau		-		-	-	30737H	111		mAdc
(VOH = 2.5 Vdc) Source	ЮН	5.0	-2.5		-2.1	-4.2	- AND DEC	-1.7		MAGE
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52		-0.44	-0.88	- and his	-0.36		
(VOH = 9.5 Vdc)	8 %	10	-1.3	QQV.	-1.1	-2.25		-0.9		
$(V_{OH} = 13.5 \text{ Vdc})$	earl a	15	-3.6		-3.0	-8.8	1300	-2.4		
(VOL = 0.4 Vdc) Sink	1	5.0	0.52	100	0.44	0.88	-	0.36		mAdc
$(V_{OL} = 0.5 \text{ Vdc})$	OL	10	1.3		1.1	2.25	149-	0.36	PEN Cycle	MAGC
(V <sub>OL</sub> = 1.5 Vdc)	5. 3899	15	3.6		3.0	8.8		2.4		
Input Current (AL Device)		15	-	± 0 1			± 0.1	-		μAdc
	lin		-		7	± 0.00001		-	±10	-
Input Current (CL/CP Device)	lin	15		±03	-	±0.00001	±0.3	-	± 1.0	µAdc
Input Capacitance (V <sub>in</sub> - 0)	Cin	0.0 <u>36</u> 2 (0.0)	-	-	A (14/17/2012)	5.0	7.5	HOL DA	-	pF
Quiescent Current (AL Device)	IDD	50	-	5.0	-	0.005	50	-	150	иAdc
(Per Package)	Fr VEX	10	-	10	-	0.010	10	001	300	
-501713	THE DAME LAND	15	-	20	-	0.015	20	1,9	600	
Quiescent Current (CL/CP Device)	1DD	5.0	44.7	20	-	0.005	20	-	150	μAdc
(Per Package)		10	~	40	-	0.010	40	-	300	
		15	-	80	0000	0.015	80	2 -	600	
Total Supply Current**†	IT	5.0			IT = (1	.0 μA/kHz)	f + Inn	1 Year op	thus.	μAdc
(Dynamic plus Quiescent,		10				.0 μA/kHz)				la .
Per Package)	L192 9	15	1557			.0 μA/kHz)				0.00
(C <sub>L</sub> 50 pF on all outputs, all buffers switching)	11									

 $<sup>^{\</sup>circ}T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

\*\*The formulas given are for the typical characteristics only at 25°C. †To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_{T}$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (VDD –VSS) in volts, f in kHz is input frequency, and k = 0.0035.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

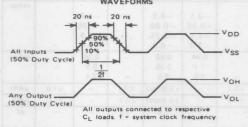
SWITCHING CHARACTERISTICS\* (C1 = 50 pF, TA = 25°C)

Characteristic		Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	6(20)	tTLH.	M sbV	indeved		ametime (3)	ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns		tTHL	5.0	15 V	100	200	driev-ruges
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns		20.0	10	-	50	100	No. of Sec.
$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		20.0	15	-	40	80	
Propagation Delay Time	88.9	tPLH,	a 0'e	T way	Isocali Tito		ns
K0 to C0		tPHL .	2 53			Light 1	old - av
tpLH, tpHL = (1.7 ns/pF) CL + 185 ns		Tall as	5.0	-	270	675	
tpLH, tpHL = (0.66 ns/pF) CL + 82 ns			10	7.3	115	290	Action V report
tPLH, tPHL = (0.5 ns/pF) CL + 60 ns		az II	15	-	85	215	Die wie
M0 to S2		DE .	1 00			Samuel St. Samuel	tra
tpLH, tpHL = (1.7 ns/pF) CL + 595 ns		0.6	5.0	-	680	1700	T
tpLH, tpHL = (0.66 ns/pF) CL + 247 ns		-	10	-	280	750	di - GA
tpLH, tpHL = (0.5 ns/pF) CL + 185 ns			15	_	210	570	A Decays

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - DYNAMIC POWER DISSIPATION WAVEFORMS



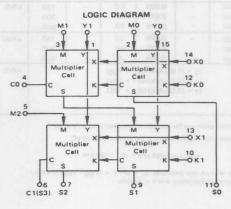
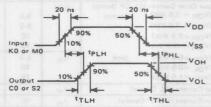
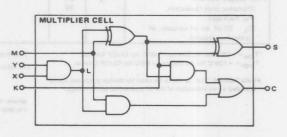


FIGURE 2 - DYNAMIC SIGNAL WAVEFORMS



For K0 to C0: Inputs X0, X1, Y0, Y1, K1, and M2 low, and inputs M0 and M1 high.

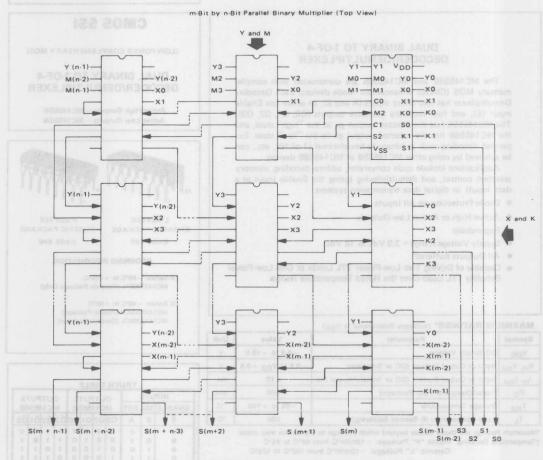
For M0 to S2: Inputs X1, Y1, and K0 low, and inputs X0, Y0, K1, M1, and M2 high.



### MC14554B

EXPANSION DIAGRAM





S = (X x Y) + K + M Where: x means Arithmetic Times.

+ means Arithmetic Plus.

$$\begin{split} S &= S(m+n\cdot 1) \; S(m+n\cdot 2) \cdots S2 \; S1 \; S0 \\ X &= X(m\cdot 1) \; X(m\cdot 2) \cdots X2 \; X1 \; X0, \; Y = Y(n\cdot 1) \; Y(n\cdot 2) \cdots Y2 \; Y1 \; Y0 \\ &= X(n\cdot 1) \; X(n\cdot 2) \cdots X2 \; X1 \; X0, \; Y = Y(n\cdot 1) \; Y(n\cdot 2) \cdots Y2 \; Y1 \; Y0 \\ &= X(n\cdot 1) \; X(n\cdot 2) \cdots X2 \; X1 \; X0, \; Y = X(n\cdot 1) \; Y(n\cdot 2) \cdots Y2 \; Y1 \; Y0 \\ &= X(n\cdot 1) \; X(n\cdot 2) \cdots X2 \; X1 \; X0, \; Y = X(n\cdot 1) \; Y(n\cdot 2) \cdots Y2 \; Y1 \; Y0 \\ &= X(n\cdot 1) \; X(n\cdot 2) \cdots X2 \; X1 \; X0, \; Y = X(n\cdot 1) \; Y(n\cdot 2) \cdots Y2 \; Y1 \; Y0 \\ &= X(n\cdot 2) \; X(n\cdot 2) \; X(n\cdot 2) \; X(n\cdot 2) \; X(n\cdot 2) \; X(n\cdot 2) \; X(n\cdot 2) \; Y(n\cdot 2) \; Y(n$$

 $K = K(m-1) \ K(m-2) \cdots K2 \ K1 \ K0 \ and \ M = M(n-1) \ M(n-2) \cdots M2 \ M1 \ M0$ (Binary Numbers).

Number of output binary digits = m + n

Number of packages = mxn/4 (For m or n or both odd select next highest even number.)

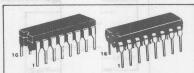
# MC14555B MC14556B

## **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

# DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

Active High Outputs - MC14555B Active Low Outputs - MC14556B



CERAMIC PACKAGE

CASE 620

P SUFFIX PLASTIC PACKAGE

CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

# DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/ Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

	0445555	BLUCK L	DIAGRAM		
M	C14555B			MC1	4556B
				(4) 102 3	KG, Y. TURN
2 A	00	4 967	2	A	<u>0</u> 0
2 B	01	5	3	В	ā1 !
1-QE	02	6	3	OE	Q2
1-95	03	7	Right Tool or to	9 =	Q3
	00	12			50
4———A	00-	12	14	A	āo 1
	01	<del></del> 11 .	14 <del></del>	A B	ā1 1
13—B	Q1 — Q2 —		13	В	Q1 1 Q2 1
	01	<del></del> 11 .			ā1 1
13—B	Q1 — Q2 —	—— 11 —— 10 —— 9	13	В	Q1 1 Q2 1

INPUTS			0	OUTPUTS				OUTPUTS				
ENABLE	SEI	LECT	M	C14	155	5B	N	IC14	455	6B		
Ē	В	A	Q3	02	Q1	QO	ŌЗ	ā2	ā1	ã		
0	0	0	0	0	0	1	1	1	1	0		
0	0	1	0	0	1	0	1	1	0	1		
0	1	0	0	1	0	0	1	0	1	1		
0	1	1	1	0	0	0	0	1	1	1		
1	x	×	0	0	0	0	1	1	1	1		

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

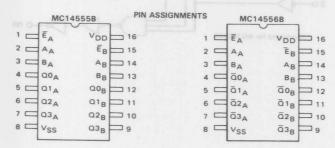
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

		000	VDD	TI	ow*		25°C	Billione	Thi	gh °	
Characterist	tic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	0.120,811	0.05	Vdc
$V_{in} = V_{DD}$ or 0			10	-	0.05	-	0	0.05	S taron s	0.05	ort must
			15	-	0.05	-	0	0.05	G (Registr) B	0.05	el atay
	"1" Level	VOH	5.0	4.95	RUN	4.95	5.0	B 12 Da	4.95	yelled as	Vdc
$V_{in} = 0 \text{ or } V_{DD}$		011	10	9.95	36601	9.95	10	CE 2 130	9.95	19 14:97	192
111		-	15	14.95	-	14.95	15	35-31	14.95	2 (4/07	192
Input Voltage	"O" Level	VIL					- 10	GP 7 33	19/8/19/2	California.	Vdc
$(V_{O} = 4.5 \text{ or } 0.5 \text{ Vdc})$			5.0	_	1.5	-	2.25	1.5	B - aniT	1.5	1-2-251
$(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$		-	10	-	3.0	-	4.50	3.0	(4q)se 7.7	3.0	TPUN
$(V_O = 13.5 \text{ or } 1.5 \text{ Vd})$			15	-	4.0	-	6.75	4.0	91a1_00,0	4.0	PLIST
(40 - 13.3 01 1.3 40	"1" Level	VIH					10	OF FID	Highin d.S.	THIST.	Vdc
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$			5.0	3.5		3.5	2.75	nart-lands	3.5	named and	metol err
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$			10	7.0	_	7.0	5.50	-	7.0	-	
(VO = 1.5 or 13.5 Vdc	:)		15	11.0	- 1	11.0	8.25	107_beau	11.0	"1972 bed	Deck 12:00
Output Drive Current (AL	Device)	ГОН						THE R. P. LEW.	10 10 1000	CONTRACTOR NO.	mAdc
(V <sub>OH</sub> = 2.5 Vdc)	Source	01,	5.0	-3.0	_	-2.4	-4.2		-1.7	-	
(V <sub>OH</sub> = 4.6 Vdc)		1 5 5 7 1	5.0	-0.64	-	-0.51	-0.88	-	-0.36	_	1 199
(VOH = 9.5 Vdc)			10	-1.6		-1.3	-2.25	_	-0.9	_	100
(VOH = 13.5 Vdc)		11年2一日	15	-4.2	REVAM	-3.4	-8.8	HO BAN	-2.4	Ad - 13	FISHI
(V <sub>OL</sub> = 0.4 Vdc)	Sink	IOL	5.0	0.64	-	0.51	0.88	or a sug	0.36	_	mAdc
(V <sub>OL</sub> = 0.5 Vdc)	0	.OL	10	1.6	_	1.3	2.25	for _ red	0.9		1111100
(V <sub>OL</sub> = 1.5 Vdc)		80.0	15	4.2	_	3.4	8.8	-	2.4	_	
Output Drive Current (CL	/CP Device)	ГОН	144	COND *		1				-	mAdc
(V <sub>OH</sub> = 2.5 Vdc)	Source	-OH	5.0	-2.5	- 1	-2.1	-4.2	_	-1.7	_	1111100
(V <sub>OH</sub> = 4.6 Vdc)	201	24	5.0	-0.52	_	-0.44	-0.88	6	-0.36	stage was	(B08)
(V <sub>OH</sub> = 9.5 Vdc)		and the	10	-1.3	200	-1.1	-2.25	187	-0.9	_	
(V <sub>OH</sub> = 13.5 Vdc)			15	-3.6	_	-3.0	-8.8	- 1	-2.4	_	
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	IOL	5.0	0.52	- 1	0.44	0.88	_	0.36	-	mAdc
$(V_{OL} = 0.5 \text{ Vdc})$	201	.OL	10	1.3	and the same of	1.1	2.25	_	0.9	HINCL PINC	- IIIAGC
$(V_{OL} = 1.5 \text{ Vdc})$		LINES !	15	3.6		3.0	8.8	_	2.4	_	
Input Current (AL Device	)	To the second	15	-	± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdc
Input Current (CL/CP Dev		lin	15	-	± 0.3	-	-		-		-
	/ice)	lin		20 Va	20.3	-	±0.00001	± 0.3	(management)	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)		Cin		.isket	D sellon	pay on had	5.0	7.5		W.T.F	pF
Quiescent Current (AL De	evice)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdc
(Per Package)			10		10		0.010	10	- 1	300	
			15	MEDITE	20	-	0.015	20	-	600	
Quiescent Current (CL/CF	Device)	IDD	5.0	(BESIG 1	20	-	0.005	20		150	μAdc
(Per Package)		00	10	-	40	_	0.010	40	-	300	
			15	-	80	-	0.015	80	_	600	
Total Supply Current**†	30Q as	IT	5.0		1	IT = (0	.85 μA/kHz	-	,		μAdc
(Dynamic plus Quiesce	ent,		10	1 9		IT = (1	.7 μA/kHz)	f + Inc	,		m.130
Per Package)			15				.6 μA/kHz)				
(C <sub>1</sub> = 50 pF on all out	puts, all					.,	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	.00			
buffers switching)		36									

<sup>\*</sup>Tlow = -55°C for AL Device, -40°C for CL/CP Device.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I  $_T$  is in  $\mu A$  (per package), C  $_L$  in pF, V = (V  $_{DD}$  – V  $_{SS}$ ) in volts, f in kHz is input frequency, and k = 0.002.



Thigh = + 125°C for AL Device, +85°C for CL/CP Device.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

## MC14555B•MC14556B

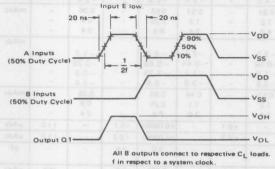
### SWITCHING CHARACTERISTICS\*(C1 = 50 pF, TA = 25°C)

Characteristic		Symbol	VDD	Min	Тур #	Max	Unit
Output Rise and Fall Time	milit	tTLH-	M Jov	10 dimed		Paris consum D	ns
tTLH, tTHL = (1.5 ns/pF) CL + 25 ns		tTHL	5.0		100	200	Aller VIII AND AND AND AND AND AND AND AND AND AND
tTLH, tTHL = (0.75 ns/pF) CL + 12.5 ns		200	10	-20	50	100	parame andro
t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		60.0	15	-	40	80	11/2
Propagation Delay Time - A, B to Output	38.1	tPLH.	4 4 66		total T. Fre		ns
tpLH, tpHL = (1.7 ns/pF) CL + 135 ns		tPHL	5.0	1 2	220	440	1
tpLH tpHL = (0.66 ns/pF) CL + 62 ns			10	-	95	190	MA.
tPLH, tPHL = (0.5 ns/pF) CL + 45 ns			15		70	140	
Propagation Delay Time - E to Output		tPLH,	10.00	1 -11			ns
tpLH, tpHL = (1.7 ns/pF) CL + 115 ns		tPHL	5.0	-	200	400	Se et. (2).)
tPLH, tPHL = (0.66 ns/pF) CL + 52 ns		0.8	10	- 1	85	170	16 = DA
tPLH, tPHL = (0.5 ns/pF) CL + 40 ns			15	-	65	130	IVO = 19

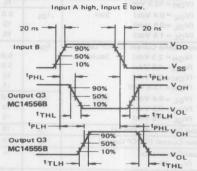
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### FIGURE 1 - DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

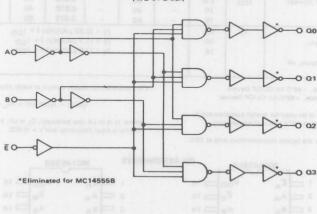


### FIGURE 2 - DYNAMIC SIGNAL WAVEFORMS



### LOGIC DIAGRAM

(1/2 of Dual)



# MC14557B

### 1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers.

- 1-64 Bit Programmable Length
- Q and Q Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or one Lowpower Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages Referenced to Voc.)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V.
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

### LENGTH SELECT TRUTH TABLE

L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1-Bit
0	0	0	0	0	1	2-Bits
0	0	0	0	1	0	3-Bits
0	0	0	0	1	1	4-Bits
0	0	0	1	.0	0	5-Bits
0	0	0	1	0	1	6 Bits
ody)	- V.3	nt p	(Signation)	20 Ve 03	Saint.	might present a
	1	10.0 -	of bridge	go ce copp	of Mg	statistics are
1	0	0	0	0	0	33 Bits
1	0	0	0	0	1	34-Bits
RIGIS	8,000	0 10 1	40.00h	ry ottal		for sub apernal
				erthan		au saubių abei
1	1	1	1	0	0	61-Bits
1	1	1	1	0	1	62-Bits
1	1	1	1	1	0	63-Bits
1	1	1	1	1	1	64-Bits

Note: Length equals the sum of the binary length control subscripts plus one.

## CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

#### BLOCK DIAGRAM Reset 40 Clock 50-OCE 60--010 70-90 A/B Select 20-L1 10-150 L4 ō -011 140-L8 130-L16 120 L32 V<sub>DD</sub> = Pin 16

# V<sub>SS</sub> = Pin 8 TRUTH TABLE

me cara	In	outs		Output
Rst	A/B	Clock	CE	Q
0	0	7	0	В
0	. 1	5	0	A
0	0	1	~	В
0	1	1	~	Α
1	×	×	×	0

Q is the output of the first selected shift register stage.

X = Don't Care.



### ELECTRICAL CHARACTERISTICS (Voltages Referenced to Vos

15			VDD	Tic	w *		25°C		Th	igh °	-
Vin = Vpp or 0	Characteristic	Symbol		Min	Max	Min	Typ #	Max	Min	Max	Uni
Vin = Vpp or 0	Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdd
V <sub>In</sub> = 0 or V <sub>DD</sub>	V <sub>in</sub> = V <sub>DD</sub> or 0		10	-	0.05	-	0	0.05	-	0.05	
Vin = 0 or VpD			15	-	0.05	-	0	0.05	-	0.05	
Vin = 0 or VpD	"1" Level	VOH	5.0	4.95	30-23	4.95	5.0	66540	4.95	400 7000	Vd
		0		9.95	-	9.95	10	AGEN	9.95	90-01-	
VO = 4.5 or 0.5 Vdc    Source   Source   VO = 4.5 or 0.5 Vdc    VO = 4.5 or 0.5 Vdc    VO = 4.5 or 1.5 Vdc    VO = 4.5 or 4.5 Vdc    VO = 4.5 vdc			15	14.95	-	14.95	15	-	14.95	-	
(VQ = 4.5 or 0.5 Vdc)   10	nput Voltage "0" Level	VIL	1 04	100	1 11 12 18 1	PINE III	THE LESS HAVE	PARTE N	St aliens	I cann an i	Vd
VO = 13.5 or 1.5 Vdc	(VO = 4.5 or 0.5 Vdc)		5.0	1945 UNIT	1.5	1	2.25	1.5	palime	1.5	DITT -
Vo   0.5 or 4.5 Vdc    V1H   S.0   3.5   - 3.5   2.75   - 3.	(VO = 9.0 or 1.0 Vdc)		10	sh Times	3.0	TO INVE	4.50		Daller all		unit.
(VO - 0.5 or 4.5 Vdc) (VO - 1.0 or 9.0 Vdc) (VO - 1.5 or 13.5 Vdc)  Dutput Drive Current (AL Device) (VOH = 2.5 Vdc) (VOH = 9.5 Vdc) (VOH = 9.5 Vdc) (VOH = 13.5 Vdc)  Dutput Drive Current (CL/CP Device) (VOH = 1.5 Vdc)  Source (VOH = 4.6 Vdc) (VOH = 1.5 Vdc)  Source (VOH = 1.5 Vdc) (VOH = 1.5 Vdc)  Source (VOH = 1.5 Vdc) (VOH = 1.5 Vdc) (VOH = 1.5 Vdc)  Source (VOH = 1.5 Vdc) (VO	(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	H RE TO	4.0	81 21	6.75	4.0	tino2 ruj	4.0	sne
10	"1" Level	VIH		AN CITYON	6760 8	TO PL BIL	toon ba	06185 05	V6/71 438	5 Mines	ano -
15	(V <sub>O</sub> = 0.5 or 4.5 Vdc)		5.0	3.5	phylaus u	3.5	2.75	rank airil	3.5	A/B-elec	Vdc
Dutput Drive Current (AL Device)			10	7.0	Burrials.	7.0	5.50	a r <del>a</del> gni	7.0	Hook-Engl	A-
VOH = 2.5 Vdc    Source   So	(V <sub>O</sub> = 1.5 or 13.5 Vdc)	-	15	11.0	-	11.0	8.25	iui <del>o</del> prii	11.0	9 9 FT BOSE	170
VOH = 4.6 Vdc    Source   So	Dutput Drive Current (AL Device)	10Н	29	all valleling	elidip a	BRITEN H	F-bass yes	vitostia		Pha device	mAd
(VOH = 9.5 Vdc) (VOH = 13.5 Vdc) (VOL = 0.4 Vdc) Sink (VOL = 0.5 Vdc) (VOL = 0.5 Vdc) (VOL = 1.5 Vdc) (VOL = 1.5 Vdc) (VOH = 2.5 Vdc) (VOH = 2.5 Vdc) (VOH = 2.5 Vdc) (VOH = 2.5 Vdc) (VOH = 4.6 Vdc) (VOH = 9.5 Vdc) (VOH = 9.5 Vdc) (VOH = 13.5 Vd	(VOH = 2.5 Vdc) Source		5.0	100000	219th digit	2.75776	FEET - 124 - 125 E	o toam		victoria.	30
(VOH = 13.5 Vdc) (VOH = 13.5 Vdc) (VOL = 0.4 Vdc) Sink (VOL = 0.5 Vdc) (VOL = 0.5 Vdc) (VOH = 2.5 Vdc) (VOH = 3.5 Vdc) (VOH = 13.5 Vdc) (	(VOH = 4.6 Vdc)	Sour I	5.0		-	1		-		-	
(VQL = 0.4 Vdc) Sink	(V <sub>OH</sub> = 9.5 Vdc)		10	0.000	-		120,000,000	Para Taloni		130	10
10	(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	1 -	-3.4	-8.8	19 Galet	-2.4	D bns L	- (0)
Vol = 1.5 Vdc   Vol = 1.5 Vdc   Source   Vol = 2.5 Vdc   Source   Vol = 2.5 Vdc   Source	(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	MARTE AND	100000000000000000000000000000000000000		mAd
Doutput Drive Current (CL/CP Device)   IOH	(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.25	- 0	1	JUGQ 118	-
(VOH = 2.5 Vdc)   Source   S	(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	16 MIN 1	2.4	Me lemit	6
VOH = 4.6 Vdc   Sink   IOL   Sink   Sink   IOL   Sink	Output Drive Current (CL/CP Device)	ІОН				70.8.40	31 2014 6	A PER	NA SOCIE	A Antoni	mAd
10	(VOH = 2.5 Vdc) Source	1	5.0								0.
15	(V <sub>OH</sub> = 4.6 Vdc)		5.0		a) admin	-		118217	1		
(VOH = 13.5 Vdc) (VOL = 0.4 Vdc) Sink (VOL = 0.5 Vdc) (VOL = 0.5 Vdc) (VOL = 1.5 Vdc)  (VOL = 0.4 Vdc)  (VOL = 0.4 Vdc)  (VOL = 0.4 Vdc)  (VOL = 0.4 Vdc)  (VOL = 0.4 Vdc)  (VOL = 0.4 Vdc)  (VOL = 0.4 Vdc)  (VOL = 0.4 Vdc)  (VOL = 0.5 Vdc)  (VOL			100		-	100000	H THE STATE OF THE	-		agner	
10	(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 1.5 Vdc)		IOL			-	V5307		l ireputio	100000000000000000000000000000000000000	TAR Set	mAd
15   3.6   - 3.0   8.8   - 2.4   - 1.0		1 1	HINGE 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	-	1000000				-	louin
Input Current (CL/CP Device)	(V <sub>OL</sub> = 1.5 Vdc)		15	3.6		3.0	8.8		2.4		1000
Total Supply Current (**)   Total Supply Current (**)	nput Current (AL Device)	lin	15		± 0.1	-	± 0.00001	± 0.1	philon	± 1.0	μAd
(V <sub>in</sub> = 0)       Quiescent Current (AL Device)     IDD     5.0     -     5.0     -     0.010     5.0     -     150       (Per Package)     10     -     10     -     0.020     10     -     300       Quiescent Current (CL/CP Device)     IDD     5.0     -     50     -     0.010     50     -     375       (Per Package)     10     -     100     -     0.020     100     -     750       (Per Package)     15     -     200     -     0.030     200     -     1500       Total Supply Current**†     17     5.0     IT = (1.75 µA/kHz) f + IDD       (Dynamic plus Quiescent,     10     IT = (3.5 µA/kHz) f + IDD       Part Package     10     IT = (3.5 µA/kHz) f + IDD	nput Current (CL/CP Device)	lin	15	D. L. D. O.A.	± 0.3	-	±0.00001	± 0.3	lov Linte	± 1.0	μAd
Quiescent Current (AL Device)     IDD     5.0     -     5.0     -     0.010     5.0     -     150       (Per Package)     10     -     10     -     0.020     10     -     300       0uiescent Current (CL/CP Device)     IDD     5.0     -     50     -     0.030     20     -     600       Quiescent Current (CL/CP Device)     IDD     5.0     -     50     -     0.010     50     -     375       (Per Package)     10     -     100     -     0.020     100     -     750       15     -     200     -     0.030     200     -     1500       Total Supply Current**†     IT     5.0     IT     (1.75 µA/kHz) f + IDD       (Dynamic plus Quiescent,     10     IT     (2.5 µA/kHz) f + IDD       (Per Package)     10     IT     (3.5 µA/kHz) f + IDD		Cin	Aug.	= 07 g	-	NS wg .	5.0	7.5	NO + loty	) ja kugal	pF
10		Inn	5.0	-	5.0	-	0.010	5.0	-	150	μAd
15	and the second s	.00	10	- 0	10	-	0.020	10	PERSONAL PROPERTY.	10111300 C/11/100	nin
Duescent Current (CL/CP Device)   IDD   5.0   -     50   -     0.010     50   -     375     (Per Package)   10   -     100   -     0.020   100   -     750     15   -     200   -     0.030     200   -     1500       17     (Dynamic plus Quiescent,   10     17     (3.5 µA/kHz) f + IDD     17   (3.5 µA/kHz) f + IDD     18   (5.25 µA/kHz) f +   100       17   (5.25 µA/kHz) f +   100	BLOCK DIAGRAM		15	_ 089	20	-	0.030	20	ST# \$100		1
10	Quiescent Current (CL/CP Device)	lpp	5.0	POR 2800 1	50	of egémi	0.010	50	ov opariti	375	μAd
15				_0188	100	and grown	0.020	100	праци з		16120
(Dynamic plus Quiescent, 10 IT = (3.5 \(\mu A/kHz\)) f + IDD	1001D		15	0.521 0	200	H OZWA	0.030	200	Cgran	1500	
(Dynamic plus Quiescent, 10 1 <sub>T</sub> = (3.5 μA/kHz) f + 1 <sub>DD</sub>	Total Supply Current * * †	IT	5.0	-		IT = (1	.75 µA/kHz	) f + Ipr			μAd
Par Backers)	(Dynamic plus Quiescent,		10	1111					24		
rer Package) 15 17 = (5.25 \(\mu\)A(\(\mu\)) 1 + 1DD	Per Package)		15	ritin.							
(CL = 50 pF on all outputs, all	(CL = 50 pF on all outputs, all	34 1		-							

 $^*T_{low} = -55^\circ C$  for AL Device,  $-40^\circ C$  for CL/CP Device.  $T_{high} = +125^\circ C$  for AL Device,  $+85^\circ C$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.001.

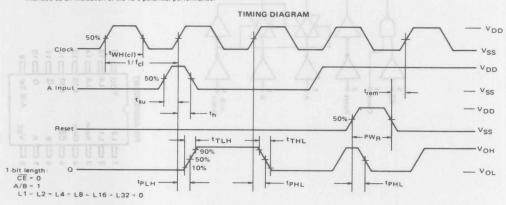
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

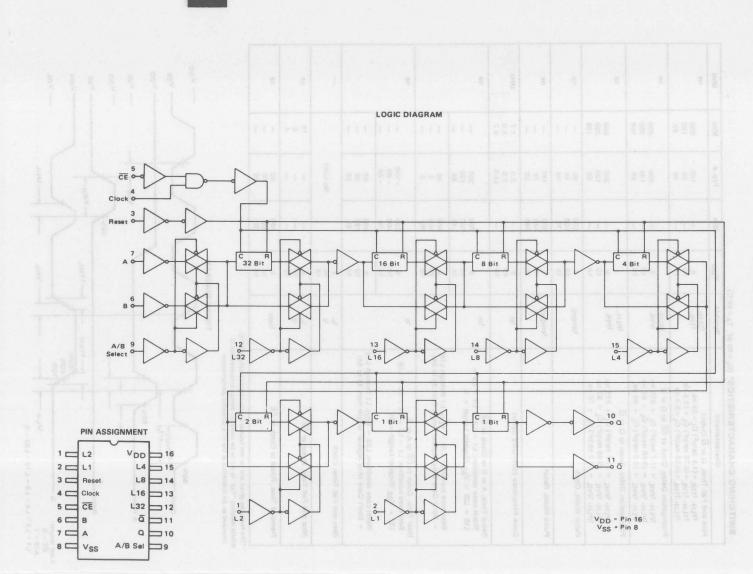
SWITCHING CHARACTERISTICS\* (C1 = 50 pF. TA = 25°C)

Characteristic	Symbol	V <sub>DD</sub>	Min	Typ #	Max	Unit
Rise and Fall Time, Q or Q Output tTLH, tTHL = (1.5 ns/pF) CL + 25 ns tTLH, tTHL = (0.75 ns/pF) CL + 12.5 ns tTLH, tTHL = (0.55 ns/pF) CL + 9.5 ns	tTLH, tTHL	5 10 15		100 50 40	200 100 80	ns
Propagation Delay, Clock or CE to Q or Q  tpLH, tpHL = (1.7 ns/pF) CL + 215 ns tpLH, tpHL = (0.66 ns/pF) CL + 97 ns tpLH, tpHL = (0.5 ns/pF) CL + 65 ns	tPLH, tPHL	5 10 15		300 130 90	600 260 180	ns
Propagation Delay, Reset to Q or \( \overline{Q} \)  tplH, tpHL = (1.7 ns/pF) CL + 215 ns tplH, tpHL = (0.66 ns/pF) CL + 97 ns tplH, tpHL = (0.5 ns/pF) CL + 70 ns	<sup>†</sup> PLH, <sup>†</sup> PHL	5 10 15		300 130 95	600 260 190	ns
Pulse Width, Clock	<sup>†</sup> WH(cl)	5 10 15	200 100 75	95 45 35	= =	ns
Pulse Width, Reset	<sup>t</sup> WH(rst)	5 10 15	300 140 100	150 70 50	=	ns
Clock Frequency (50% Duty Cycle)	fcI	5 10 15		3.0 7.5 13.0	1.7 5.0 6.7	MHz
Setup Time, A or B to Clock or $\overline{\text{CE}}$ Worst case condition: L1 = L2 = L4 = L8 = L16 = L32 = V <sub>SS</sub> (Register Length = 1)  Best case condition: L32 = V <sub>DD</sub> , L1 through L16 = Don't Care (Any register length from 33 to 64)	<sup>t</sup> su	5 10 15 5 10	700 290 145 400 165 60	350 130 85 45 5	1111	ns
Hold Time, Clock or $\overline{\text{CE}}$ to A or B Best case condition: L1 = L2 = L4 = L8 = L16 = L32 = $V_{SS}$ (Register Length = 1)  Worst case condition: L32 = $V_{DD}$ , L1 through L16 = Don't Care (Any register length from 33 to 64)	t <sub>h</sub>	5 10 15 5 10 15	200 100 10 400 185 85	- 150 - 60 - 50 50 25 22		ns
Rise and Fall Time, Clock	t <sub>r</sub> , t <sub>f</sub>	5 10 15		No Limit		-
Rise and Fall Time, Reset or CE	t <sub>r</sub> ,	5 10 15	1 🗏		15 5 4	μs
Removal Time, Reset to Clock or CE	<sup>t</sup> rem	5 10 15	160 80 70	80 40 35	=	ns

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.





6-41

# MC14560B

### **NBCD ADDER**

The MC14560B adds two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

This device can also subtract when one set of inputs is complemented with a 9's Complementer (MC14561B).

All inputs and outputs are active high. The carry input for the least significant digit is connected to VSS for no carry in.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
In lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	- 65 to + 150	°C
Tohus	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur †Temperature Derating: Plastic "P" Package - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

### TRUTH TABLE

				INPUT	1301				1	C	UTPU	T	
Α4	А3	A2	A1	B4	В3	B2	B1	Cin	Cout	54	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	-1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	01V	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

\*Partial truth table to show logic operation for representative input values.

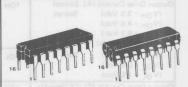
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\text{In}}$  and  $V_{\text{Out}}$  should be constrained to the range  $V_{\text{SS}} \leqslant (V_{\text{in}} \text{ or } V_{\text{Out}}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

# **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

NBCD ADDER



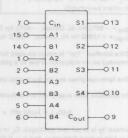
L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### BLOCK DIAGRAM



V<sub>DD</sub> = Pin 16 V<sub>SS</sub> = Pin 8 \_

### ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		VDD	Tic	ow*		25°C		Th	igh °	1
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0	-	10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
$V_{in} = 0 \text{ or } V_{DD}$	011	10	9.95		9.95	10		9.95	_	
		15	14.95	_	14.95	15	387	14.95	_	
Input Voltage "0" Level	VIL								Common Co	Vdc
(Vo 4.5 or 0.5 Vdc)		5.0	into late	1.5	Al ur sur	2.25	1.5	ps allege	1.5	
(VO = 9.0 or 1.0 Vdc)		10	1615 01 3	3.0	150 006	4.50	3.0	migl (II	3.0	000
(VO = 13.5 or 1.5 Vdc)	11	15	_	4.0	-	6.75	4.0	-	4.0	000
"1" Level	VIH	- 191	2000 B	el elegate di	130 944	10000 754	HOUR O	5. 760 5	MANA SIM	
(Vo = 0.5 or 4.5 Vdc)		5.0	3.5		3.5	2.75	nerzelge	3.5	drive but	Vdc
(VO : 1.0 or 9.0 Vdc)		10	7.0	ni was	7.0	5.50	OS -CRUCI	7.0	down It.	
(VO = 1.5 or 13.5 Vdc)		15	11.0	/H = 1183	11.0	8.25	005-100	11.0	soft-floa	Tenant T
Output Drive Current (AL Device)	ТОН									mAdd
(VOH = 2.5 Vdc) Source	·OH	5.0	-3.0	_	-2.4	-4.2	101-1A 0	-1.7	mi9-shot	1 0
(VOH = 4.6 Vdc)		5.0	-0.64	_	-0.51	-0.88	_	-0.36	_	
(VOH = 9.5 Vdc)		10	-1.6	_	-1.3	-2.25	-Lagn	-0.9	oV <u>ulqqu</u>	- 6
(VOH = 13.5 Vdc)	Orien I	15	-4.2	nO-n si	-3.4	-8.8	al -ur	-2.4	a subtance	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	noFLand	0.51	0.88	11 - 10	0.36	enoticu	mAde
(V <sub>OL</sub> = 0.5 Vdc)	.OL	10	1.6		1.3	2.25	_	0.9	fundation	
(VOI = 1.5 Vdc)	C. Della .	15	4.2	_	3.4	8.8	_	2.4	_	
Output Drive Current (CL/CP Device)	ГОН				-					mAdd
(VOH = 2.5 Vdc) Source	·OH	5.0	-2.5		-2.1	-4.2		-1.7	_	1
(VOH = 4.6 Vdc)	HED A	5.0	-0.52		-0.44	-0.88		-0.36		
(VOH = 9.5 Vdc)		10	-1.3		-1.1	-2.25		-0.9		
(VOH = 13.5 Vdc)		15	-3.6	_	-3.0	-8.8	el degrado	-2.4	RTALR M	Jiel X
(VOI = 0.4 Vdc) Sink	loL	5.0	0.52	_	0.44	0.88	00007210.50	0.36	-	mAdo
(VOL = 0.5 Vdc)	.01	10	1.3	3 E-	1.1	2.25	_	0.9	ulara 2 De	IIIAGC
(V <sub>OL</sub> = 1.5 Vdc)	x 1	15	3.6		3.0	8.8	-	2.4	muque or	1 535
nput Current (AL Device)	lin	15	_	± 0.1		±0.00001	± 0.1	-	± 1.0	µАdc
nput Current (CL/CP Device)		15	_	± 0.3		±0.00001	± 0.3	the base	± 1.0	u Adc
	lin		_	10.3	-				± 1.0	
Input Capacitance (V <sub>in</sub> = 0)	Cin	107		ag	-	5.0	7.5	mulis agri	eT agaids	pF
Quiescent Current (AL Device)	IDD	5.0	- 00	5.0	-	0.005	5.0	1,17 77519	150	μAdc
(Per Package)		10	ao Tum i	10	or others	0.010	10	-	300	i more
		15		20	BASE TOWN	0.015	20		600	Kale valor
Quiescent Current (CL/CP Device)	IDD	5.0	0/2010	20	(A) (上)	0.005	20	Inine D	150	μAdo
(Per Package)		10		40	-	0.010	40	-	300	
		15	-	80	- 1	0.015	80	-	600	
Total Supply Current**†	IT	5.0			IT = (1	.68 μA/kHz	f+ Ipp			μAdc
(Dynamic plus Quiescent,		10				.35 μA/kHz				
Per Package)		15				.03 μA/kHz				EA.
(CL = 50 pF on all outputs, all										-
buffers switching)										0

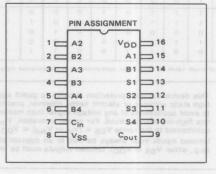
 $^*T_{low} = -55^\circ\text{C}$  for AL Device,  $-40^\circ\text{C}$  for CL/CP Device.  $T_{high} = +125^\circ\text{C}$  for AL Device,  $+85^\circ\text{C}$  for CL/CP Device.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: IT is in  $\mu A$  (per package),  $C_L$  in pF, V = (VDD – VSS) in volts, f in kHz is input frequency, and k = 0.005.



SWITCHING CHARACTERISTICS\* (CL = 50 pF TA = 25°C)

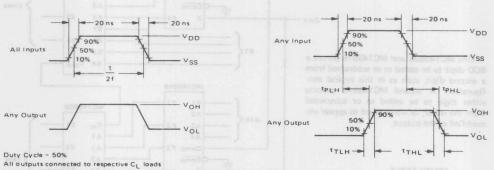
Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH.					ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTHL	5.0	-	100	200	
$t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	1	10	-	50	100	12
$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	The state of the s	15	-	40	80	A P
Propagation Delay Time	tPLH,			+(_1#	HULL	ns
A or B to S	tPHL					
tpLH, tpHL = (1.7 ns/pF) CL + 665 ns		5.0	-	750	2100	
tPLH, tPHL = (0.66 ns/pF) CL + 297 ns		10	11-1-	330	900	1
tPLH, tPHL = (0.5 ns/pF) CL + 195 ns	- I hallow	15	-	220	675	
A or B to Cout		TA E	He LU		77	ns
tPLH tPHL = (1.7 ns/pF) CL + 565 ns		5.0		650	1800	
tPLH tPHL = (0.66 ns/pF) CL + 197 ns		10	114	230	600	-
tpLH, tpHL = (0.5 ns/pF) CL + 145 ns		15		170	450	EA
Cin to Cout						ns
tPLH, tPHL = (1.7 ns/pF) CL + 465 ns		5.0	- 1	550	1500	838
tPLH, tPHL = (0.66 ns/pF) CL + 187 ns		10	11-11	220	600	-
tPLH, tPHL = (0.5 ns/pF) CL + 135 ns		15		160	450	A
Turn-Off Delay Time	tPLH	to the second		100		ns
Cin to S			The state of the s			200
tpLH = (1.7 ns/pF) CL + 715 ns		5.0	-	800	2250	
tPLH = (0.66 ns/pF) CL + 197 ns		10	-	350	975	
tpLH = (0.5 ns/pF) CL + 215 ns		15		240	750	
Turn-On Delay Time	tPHL					ns
C <sub>in</sub> to S	-XI		Number of the			\$5.00 = 5003
tpHL = (1.7 ms/pF) CL + 565 ns		5.0	-	650	1800	8 519 = gpV
tpHL = (0.66 ns/pF) CL + 197 ns		10	-	230	600	
tpHL = (0.5 ns/pF) CL + 145 ns		15	-	170	450	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### FIGURE 1 - POWER DISSIPATION WAVEFORMS

### FIGURE 2 - SWITCHING TIME WAVEFORMS



f = System clock frequency

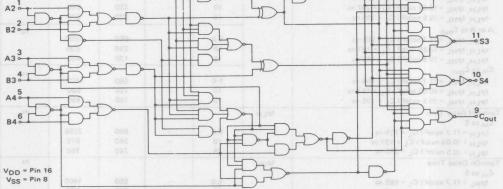
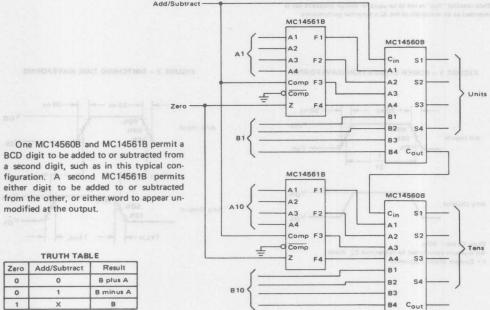


FIGURE 3 - PARALLEL ADD/SUBTRACT CIRCUIT



Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	В

X = Don't Care

B1

# 0

# APPLICATIONS INFORMATION

### INTRODUCTION

Frequently in small digital systems, simple decimal arithmetic is performed. Decimal data enters and leaves the system arithmetic unit in a binary coded decimal (BCD) format. The adder/subtracter in the airthmetic unit may be required to accept sign as well as magnitude, and generate sign, magnitude, and overflow. In the past, it has been cumbersome to build sign and magnitude adder/subtracters. Now, using Motorola's MSI CMOS functions, the MC14560 NBCD Adders and MC14561 9's Complementers, NBCD adder/subtracters may be built economically, with surprisingly low package count and moderate speed.

Some background information on BCD arithmetic is presented here, followed by simple circuits for unsigned adder/subtracters. The final circuit discussed is an adder/subtracter for signed numbers with complete overflow and sign correction logic.

### **DECIMAL NUMBER REPRESENTATION**

Because logic elements are binary or two-state devices, decimal digits are generally represented as a group of bits in a weighted format. There are many possible binary codes which can be used to represent a decimal number. One of the most popular codes using 4 binary digits to represent 0 thu 9 is Natural Binary Coded Decimal (NBCD or 8-4-2-1 code).

NBCD is a weighted code. If a value of "0" or "1" is assigned to each of the bit positions, where the rightmost position is  $2^0$  and the leftmost is  $2^3$ , and the values are summed for a given code, the result is equal to the decimal digit represented by the code. Thus, 0110 equals  $0\cdot2^3+1\cdot2^2+1\cdot2^1+0\cdot2^0=4+2=6$ . The 1010, 1011, 1100, 1101, 1110, and 1111 binary codes are not used. Because of these illegal states, the addition and subtraction of NBCD numbers is more complex than similar calculations on straight binary numbers.

### ADDITION OF UNSIGNED NBCD NUMBERS

When 2 NBCD digits, A and B, and a possible carry, C, are added, a total of 20 digit sums (A + B + C) are possible as shown in Table 1.

The binary representations for the digit sums 10 thru 19 are offset by 6, the number of unused binary states, and are not correct. An algorithm for obtaining the correct sum is shown in Figure 1. A conventional method of implementing the BCD addition algorithm is shown in Figure 2(a). The NBCD digits, A and B, are summed by a 4 bit binary full adder. The resultant (sum and carry) is input to a binary/BCD code converter which generates the correct BCD code and carry.

An NBCD adder block which performs the above function is available in a single CMOS package (MC14560). Figure 2(b) shows n decades cascaded for addition of n digit unsigned NBCD numbers. Add time is typically 0.1  $\pm$  0.2n  $\mu s$  for n decades. When the carry out of the most significant decade is a logical "1", an overflow is indicated.

### COMPLEMENT ARITHMETIC

Complement arithmetic is used in NBCD subtraction. That is, the "complement" of the subtrahend is added to the minuend. The complementing process amounts to biasing the subtrahend such that all possible sums are positive. Consider the subtraction of the NBCD numbers, A and B:

$$R = A - B$$

where R is the result. Now bias both sides of the equation by  $10^N\,-\,1$  where N is the number of digits in A and B.

$$R + 10^N - 1 = A - B + 10^N - 1$$

Rearranging,

$$R + 10^{N} - 1 = A + (10^{N} - 1 - B)$$

The term  $(10^N-1-B)$ , -B biased by  $10^N-1$ , is known as the 9's complement of B. When A>B, R +  $10^N-1>10^N-1$ ; thus R is a positive number. To obtain R, 1 is added to R +  $10^N-1$ , and the carry term,  $10^N$ , is dropped. The addition of 1 is called End Around Carry (EAC).

When A < B, R + 10<sup>N</sup> - 1 < 10<sup>N</sup> -1, no EAC results and R is a negative number biased by 10<sup>N</sup> - 1; thus R + 10<sup>N</sup> - 1 is the 9's complement of B

### SUBTRACTION OF UNSIGNED NBCD NUMBERS

Nine's complement arithmetic requires an element to perform the complementing function. An NBCD 9's complementer may be implemented using a 4 bit binary adder and 4 inverters, or with combinatorial logic. The Motorola MC14561 9's complementer is available in a single package. It has true and inverted complement disable, which allow straight-through or complement modes of operation. A "zero" line forces the output to "0". Figure 3 shows an NBCD subtracter block using the MC14560 and MC14561. Also shown are n cascaded blocks for subtraction of n digit unsigned numbers. Subtract time is 0.6 + 0.4n µs for n stages. Underflow (borrow) is indicated by a logical '0" on the carry output of the most significant digit. A '0" carry also indicates that the difference is a negative number in 9's complement form. If the result is input to a 9's complementer, as shown, and its mode controlled by the carry out of the most significant digit, the output of the complementer will be the correct negative magnitude. Note that the carry out of the most significant digit (MSD) is the input to carry in of the least significant digit (LSD). This End Around Carry is required because subtraction is done in 9's complement arithmetic.

By controlling the complement and overflow logic with an add/subtract line, both addition and subtraction are performed using the basic subtracter blocks (Figure 4).

TABLE 1 - Sum = A + B + C

Binary Sums	Decimal Number	Corrected Binary Sums
0000 as 008M ni 598	0	0000
		0001
0010	2000	0010
0011010 gnimemslumes	3 480	0011
0100	Andrea Andrea	0100
0101 golfogridus ant to	5	0101
0110	6	0110
0111	7 08 4	0111
1000	8	1000
1001	9	1001
1010	10	0000 + Carry
1011	11	0001 + Carry
1100 Non valid	12	0010 + Carry
1101 BCD	13	0011 + Carry
1110 representation	14	0100 + Carry
1111)	15	0101 + Carry
0000 + Carry	16	0110 + Carry
0001 + Carry	17	0111 + Carry
0010 + Carry	18	1000 + Carry
0011 + Carry	19	1001 + Carry

# ADDITION AND SUBTRACTION OF SIGNED NBCD NUMBERS

Using MC14560 NBCD Adders and MC14561 9's Complementers, a sign and magnitude adder/subtracter can be configured (Figure 5). Inputs A and B are signed positive (As, Bs = "0") or negative (As, Bs = "1"). B is added to or subtracted from A under control of an Add/Sub line (subtraction = "1"). The result, R, of the operation is positive signed, positive signed with overflow, negative signed, or negative signed with overflow. Add/subtract time is typically 0.6  $\pm$  0.4n  $\mu s$  for n decades.

An exclusive-OR of Add/Sub line and BS produces B', which controls the B complementers. If BS, the sign of B, is a logical "1" (B is negative) and the Add/Sub line is a "0" (add B to A), then the output of the exclusive-OR (BS') is a logical "1" and B is complemented. If BS = "1" and Add/Sub = "1", B is not complemented since subtracting a negative number is the same as adding a positive number. When Add/Sub is a "1" and BS = "0", BS' is a "1" and B is complemented. The A complementer is controlled by the A sign bit, AS. When AS = "1", A is complemented.

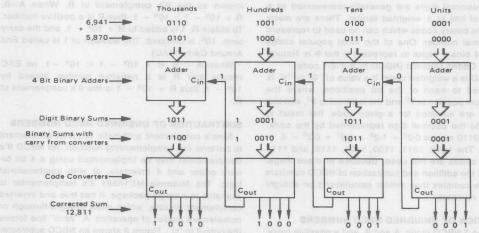


FIGURE 4 — Unsigned NBCD Addition Algorithm

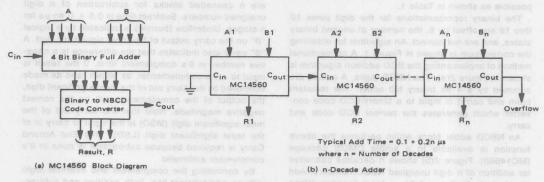


FIGURE 5 — Addition of Unsigned NBCD Numbers

6

The truth table and Karnaugh maps for sign, overflow, and End Around Carry are shown in Figures 6 and 7. Note the use of Bg' from the exclusive-OR of Add/Sub and Bg. Bg' eliminates Add/Sub as a variable in the truth table. As an example of truth table generation, consider an n decade adder/subtracter where Ag = "0", Bg = "1", and Add/Sub = "0". B is in 9's complement form,  $10^N - 1 - B$ . Thus  $A + (10^N - 1 - B) = 10^N - 1 + (A - B)$ . There is no carry when  $A \le B$ , and the sign is negative (sign = "1"). When Ag and Bg are opposite states and Add/Sub is a "0" (add mode), no overflow can occur (overflow = "0"). The other output states are determined in a similar manner (see Figure 6).

From the Karnaugh maps it is apparent that End Around Carry is composed of the two symmetrical functions S2 and S3 of three variables with A5 B5'  $C_{\rm Out}$  as the center of symmetry. This is the definition of the majority logic function  $M_3({\rm ABC})$ . Similarly the Sign is composed of the symmetrical functions S2(3) and S3(3) but with the center of symmetry translated

to AsBs'  $C_{out}$ . This is equivalent to the majority function  $M_3(AsBs'$   $\overline{C}_{out})$ . Further evaluation of the maps and truth table reveal that Overflow can be generated by the exclusive-OR function of End Around Carry and Carry Out. This analysis results in a minimum device count consisting of one exclusive-OR package and one dual Majority Logic package to implement Bs', EAC, Sign and Overflow. The logic connections of these devices are shown in Figure 5.

The output sign, Rs, complements the result of the add/subtract operation when Rs = "1". This is required because the adder performs 9's complement arithmetic. Complementing, when Rs indicates the result is negative, restores sign and magnitude convention.

Several variations of the adder/subtracter are possible. For example, 9's complement is available at the output of the NBCD adders, and output complementers are eliminated if sign and magnitude output is not required.

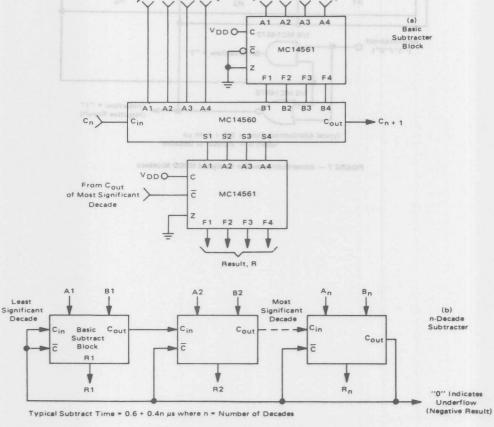


FIGURE 6 — Subtraction of Unsigned NBCD Numbers

# MC14560B

### SUMMARY of the sylupe of and all of

The concepts of binary code representations for decimal numbers, addition, and complement subtraction were discussed in detail. Using the basic Adder and Complementer MSI blocks, adder/subtracters for both signed and unsigned numbers were illustrated with examples.

#### REFERENCES

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- 2. McMOS Handbook, Motorola Inc., 1st Edition.
- Beuscher, H.: Electronic Switching Theory and Circuits, New York, Van Nostrand Reinhold, 1971.
- Garrett, L.: CMOS May Help Majority Logic Win Designer's Vote, Electronics, July 19, 1973.
- 5. Richards, R.: Digital Design, New York, Wiley-Interscience, 1971.

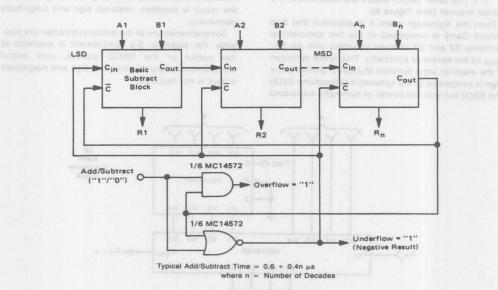
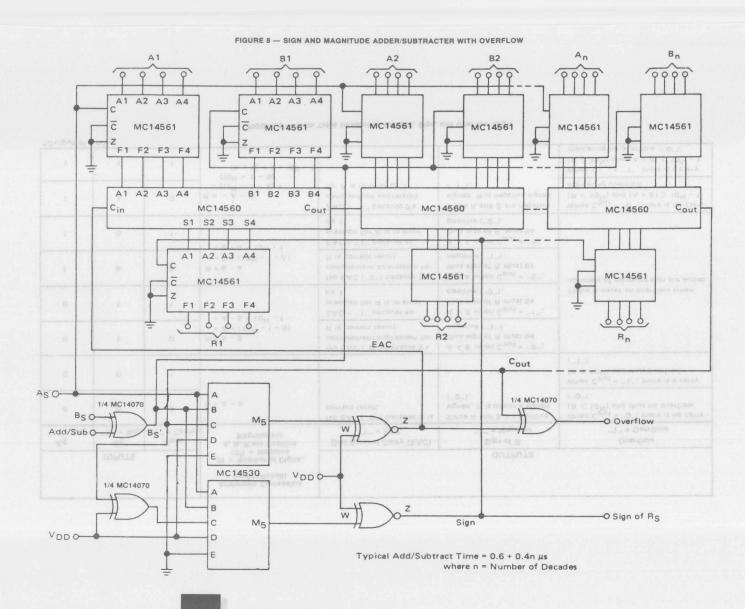


FIGURE 7 — Adder/Subtracter for Unsigned NBCD Numbers





INPUTS		0	Arithmetic Expression for R* (Result)  (N = Number of Digits, 10N = Modulus	OUTPUTS					
As "1" = Neg	BS' "1" = Neg	Cout	A, B, R are Positive Magnitudes)	End Around Carry (EAC) "1" = EAC	Sign of R "1" = Negative	Overflow "1" = Overflow			
0	0	0	R = A + B	No EAC ("0") because R is correct result.	Since A and B are positive signed, R is positive signed ("0").	When $C_{Out} = "0"$ , there is no carry $(R < 10^N)$ and thus no overflow $("0")$ .			
0	0	1			, cos	When $C_{out} = "1"$ , there is a carr $(R \ge 10^N)$ and thus overflow $("1")$			
0	1	0	R = A - B = A + (10 <sup>N</sup> - 1 - B)	No EAC ("0") because 9's complement expression for R is correct result.	$A \leq B$ when $C_{out} = "0"$ ; thus sign of R must be negative ("1").	80			
0	= A - B + 10 <sup>N</sup> - 1	and the same of the same of the same of	EAC = "1" because ex- pression for R is in error by 1.	A > B when C <sub>out</sub> = "1"; thus sign of R must be positive ("0").	There is never an overflow when				
1	0	0	R = B - A = B + (10 <sup>N</sup> - 1 - A)	No EAC ("0") because 9's complement expression for R is correct result.	$B \le A$ when $C_{out} = "0"$ ; thus sign of R must be negative ("1").	numbers of opposite sign are adde			
1	0	1	= B - A + 10 <sup>N</sup> - 1	EAC = "1" because ex- pression for R is in error by 1.	B > A when C <sub>out</sub> = "1"; thus sign of R must be positive ("0").				
1	1, 4	0	R = -A - B = $(10^{N} - 1 - A) +$	EAC = "1" because 9's complement expression for R is in error by 1.	Since A and B are negative signed, R is negative signed ("1").	When $C_{Out}$ = "0", there is no carr (R < 10 <sup>N</sup> ) and (A + B) > 10 <sup>N</sup> - 1 indicating overflow ("1").			
1	1	1	$(10^{N} - 1 - B)$ = - (A + B) + 2 × 10 <sup>N</sup> - 2		÷ - HH- ÷ r	When $C_{out} = "1"$ , there is a carry $(R \ge 10^N)$ and $(A + B) \le 10^N - 1$ indicating no overflow $("0")$ .			

Output of Adders

6-424

FIGURE 9 — Truth Table Generation for EAC, Sign, and Overflow Logic

### TRUTH TABLE

	INPUT	S	0	UTPUT	rs
As	B <sub>S</sub> '	Cout	EAC	SGN	OVF
0	0	0	0	0	0
0	1	0	0	1	0
1	0	0	0	1	0
1	1	0	1	1	39 1
0	0	1	0	0	1
0	Jar	wanta.	91100	0	0
1	0	1	1	0	0
1	1	1	1	1	0

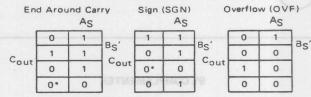
Bs' = (Add/Sub) +Bs

As = Sign of A ("1" = Negative)

Bs = Sign of B ("1" = Negative)

Cout = Adder Carry Out

# KARNAUGH MAPS



\* = Center of Symmetry

EAC = S2 (A<sub>S</sub>B<sub>S</sub>' C<sub>out</sub>) + S3 (A<sub>S</sub>B<sub>S</sub>' C<sub>out</sub>) = M<sub>3</sub> (A<sub>S</sub>B<sub>S</sub>' C<sub>out</sub>)

SGN = S2 (A<sub>S</sub>B<sub>S</sub>' C<sub>out</sub>) + S3 (A<sub>S</sub>B<sub>S</sub>' C<sub>out</sub>) = M<sub>3</sub> (A<sub>S</sub>B<sub>S</sub>' C<sub>out</sub>)

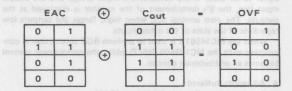


FIGURE 10 — Mapping of EAC, Sign and Overflow Logic

This device contains protection circuity to guard against contage due to high static vortages or stepties contains a function must be taken to avoid applications of the voltage higher than maximum rated voltages to this high-impoduless circuit. For accordance or person operations to the range Vous should be constrained to the range Vous explicit to the value of Vous event of Vous event where the voltage of Vous event of the voltage of Vous event of the voltage of Vous event of the voltage of Vous event of the voltage of voltage of the volta



### 9's COMPLEMENTER

The MC14561B 9's complementer is a companion to the MC14560B NBCD adder to allow BCD subtraction. A BCD number (8-4-2-1 code) is applied to the inputs (A1 =  $2^0$ , A2 =  $2^1$ , A3 =  $2^2$ , A4 =  $2^3$ ). If the complement control (Comp) is low, the BCD number appears at the outputs unmodified. The complement disable (Comp) allows the complement control to be gated, or an inverted control signal to be used. If the complement input is high and the disable input low, the 9's complement of the number is displayed at the outputs. The zero control (Z), when high, forces the outputs low regardless of the state of the other inputs.

When the MC14561B is used to perform BCD subtraction in conjunction with the MC14560B NBCD adder, the complement control becomes an add/subtract control.

- All Inputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

# **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

9's COMPLEMENTER





L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

PIN ASSIGNMENT A1 VDD 14 F1 = 13 A2 2 = 3 = A3 F2 12 4 = A4 F3 11 5 Comp F4 10 z | 9 7 - VSS NC B NC = No Connection

TRUTH TABLE

Z	Comp	Comp	F1	F2	F3	F4	Mode		
0	0	0		100					
0	0	1	A1	A2	A3	A4	Straight-through		
0	1	1							
0	1	0	Ā1	A2	A2A3 + A2A3	Ā2Ā3Ā4	Complement		
1	×	×	0	0	0	0	Zero		

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

	च व्यूप	DHA	VDD	Tic	w*		25°C		Thi	gh*	
Characteristic		Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage '	"O" Level	VOL	5.0	-	0.05	-	0	0.05	ion Et os	0.05	Vdc
$V_{in} = V_{DD}$ or 0	400	0.	10	1	0.05	-	0	0.05		0.05	137
0.8	02-	-	15	+	0.05		0	0.05	non 80.0)	0.05	(F)
200	"1" Level	VOH	5.0	4.95	4747	4.95	5.0	-	4.95	CHEVI THUSE	Vdc
Vin = 0 or VDD	004 2		10	9.95	1491	9.95	10	0.0	9.95	THEFT, H	192
	190		15	14.95	-	14.95	15	" PIT	14.95	THEFT .3	177
nput Voltage	"0" Level	VIL	J						200	APPENT OF	Vdc
$(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$			5.0	-	1.5	it, in which	2.25	1.5	No. and Ten.	1.5	of the same
$(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$			10	-	3.0	-	4.50	3.0	10 TO 0 10 TO	3.0	discis.
$(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$			15		4.0	-	6.75	4.0	to medical	4.0	U-DATE OF
(10 100 0 110 100)	"1" Level	VIH		MWAN	MAR						14 6
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$			5.0	3.5	- 1	3.5	2.75		3.5	-	Vdc
$(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$			10	7.0	-	7.0	5.50	-	7.0	-	
$(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$			15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (AL D	evice)	10Н									mAdd
(VOH = 2.5 Vdc) S	Source	· · ·	5.0	-3.0	-	-2.4	-4.2	-	-1.7	_	
$(V_{OH} = 4.6 \text{ Vdc})$			5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
(VOH = 9.5 Vdc)			10	-1.6	-	-1.3	-2.25	_	-0.9	-	
$(V_{OH} = 13.5 \text{ Vdc})$			15	-4.2	-	-3.4	-8.8	-	-2.4	-	
(VOI = 0.4 Vdc) S	Sink	101	5.0	0.64		0.51	0.88	-	0.36	-	mAd
$(V_{OL} = 0.5 \text{ Vdc})$		0.	10	1.6	- 1	1.3	2.25	-	0.9		1
(VOL = 1.5 Vdc)			15	4.2	_	3.4	8.8	_	2.4	-	
Output Drive Current (CL/C	P Device)	ЮН	10,139A	1 11117 11	-	1	1				mAde
	Source	On	5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	
(V <sub>OH</sub> = 4.6 Vdc)			5.0	-0.52	-	-0.44	-0.88	- 3	-0.36	_	
(VOH = 9.5 Vdc)			10	-1.3	0.27	-1.1	-2.25	-	-0.9	-	
(V <sub>OH</sub> = 13.5 Vdc)			15	-3.6	-	-3.0	-8.8	-	-2.4		Pulas
	Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36		mAdd
$(V_{OL} = 0.5 \text{ Vdc})$		OL	10	1.3	_	1.1	2.25		0.9	_	
(VOL = 1.5 Vdc)			15	3.6	-	3.0	8.8	_	2.4		
Input Current (AL Device)		lin	15	-44 10	±01	-sn s	±0.00001	±0.1	-	± 1.0	μAdo
Input Current (CL/CP Devic	el	lin	15		±03	-	±0.00001	± 0.3	-	± 1.0	μAdo
Input Capacitance				-	-	-	5.0	7.5	1000	-1.0	DF
(V <sub>in</sub> · 0)		Cin		I I		-	5.0	7.5			pr
Quiescent Current (AL Devi	ce)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdd
(Per Package)	20 y 10 7 1		10	-	10	- 1	0.010	10	-	300	1
	85V		15	-	20	1	0.015	20	-	600	
Quiescent Current (CL/CP D	Device)	IDD	5.0	-	20	No	0.005	20	yn=	150	μAde
(Per Package)	1		10	-	40	1/3-801	0.010	40	-	300	
	10 ×		15	-	80		0.015	80	-	600	
Total Supply Current**†		IT	5.0		(m) and (m)	IT = (	1.5 µA/kHz	) f + Ipp			μAdd
(Dynamic plus Quiescent		21	10			IT = (	3.0 µA/kHz	) + + IDD	100		
Per Package)		180.0	15				4.5 µA/kHz				1
(CL - 50 pF on all outpu	its, all							P Harris			1
buffers switching)		H (358) 17									

<sup>\*</sup>T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device. T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C. †To calculate total supply current at loads other than 50 pF:

$$I_{T}(C_{L}) = I_{T}(50 \text{ pF}) + (C_{L} - 50) \text{ Vfk}$$

where:  $I_{T}$  is in  $\mu A$  (per package),  $C_{L}$  in pF, V = (V\_{DD}-V\_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

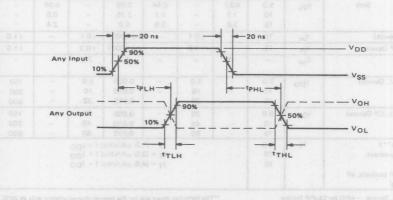
SWITCHING CHARACTERISTICS\* (CL = 50 pF TA = 25°C)

Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH.	18 55V	Leggge E	10 m	Usin ezzgenekti	ns
tTLH, tTHL = (1.5 ns/pF) CL + 25 ns	tTHL	5.0	-	100	200	
tTLH, tTHL = (0.75 ns/pF) CL + 12.5 ns	60/0	10	1 10× 1	50	100	
tTLH, tTHL = (0.55 ns/pF) CL + 9.5 ns	00.0	15	-	40	80	- niv
Propagation Delay Time	tPLH.	1 00	1	Salara de conjunt		ns
tpLH, tpHL = (1.7 ns/pF) CL + 315 ns	TPHL	5.0	40x 1	400	1000	
tpLH, tpHL = (0.66 ns/pF) CL + 127 ns		10	- 1	160	400	
tPLH, tPHL = (0.5 ns/pF) CL + 95 ns		15	-	120	300	

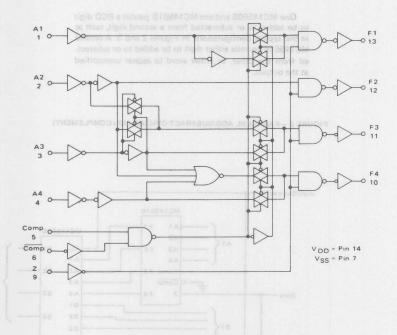
<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### FIGURE 1 - SWITCHING TIME WAVEFORMS



### LOGIC DIAGRAM



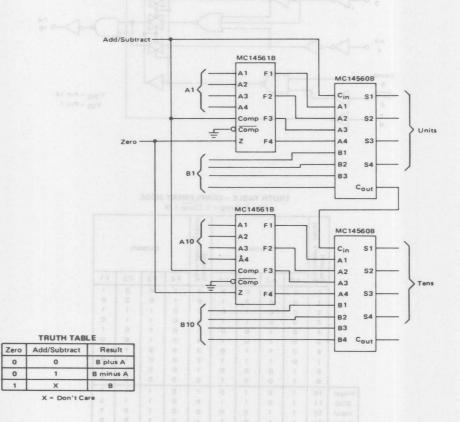
TRUTH TABLE - COMPLEMENT MODE (Z = 0, Comp = 1, Comp = 0)

	Decimal Equivalent Input		Inp	uts 2 A		Decimal Equivalent Output		Outp	uts	
	Eq.	A4	A3	A2	A1	Eq	F4	F3	F2	F1
	0	0	0	0	0	9	1	0	0	1
	1	0	0	0	1	8	1	0	0	0
	2	0	0	1	0	7	0	1	1	1
	3	0	0	1	1	6	0	1	1	0
	4	0	1	0	0	5	0	1	0	1
	5	0	1	0	1	4	0	1	0	0
	6	0	1	1	0	3	0	0	1 35	1
	7	0	1	1	1	2	0	0	11	0
	8	1	0	0	0	1	0	0	0	1
	9	1	0	0	1	0	0	0	0	0
legal	10	1	0	1	0	7	0	1	1	1
BCD	11	1	0	1	1	6	0	1	1	0
nput	12	-1	1	0	0	5	0	- 1	0	1
odes	13	1	1	0	1	4	0	1	0	0
	14	1	1	1	0	3	0	0	1	1
	15	1	1	1	1	2	0	0	1	0

### TYPICAL APPLICATIONS

One MC14560B and one MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in the typical configurations in Figures 2 and 3. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

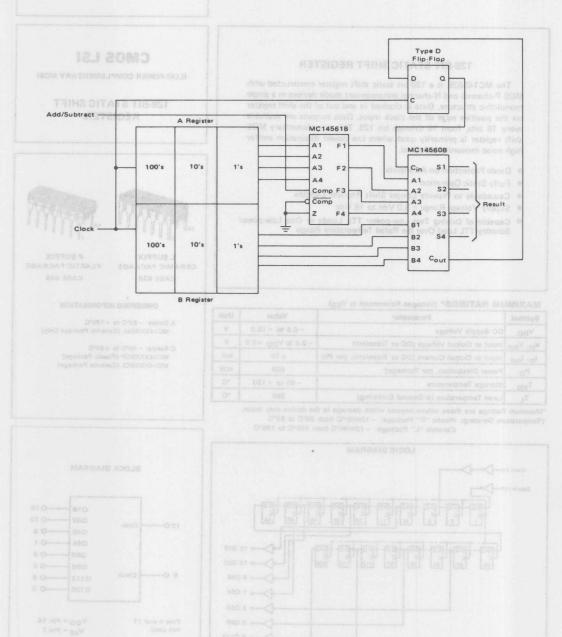
### FIGURE 2 - PARALLEL ADD/SUBTRACT CIRCUIT (10's COMPLEMENT)



MC145828

FIGURE 3 - SERIAL ADD/SUBTRACT CIRCUIT





# MC14562B

### 128-BIT STATIC SHIFT REGISTER

The MC14562B is a 128-bit static shift register constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through bit 128. This complementary MOS shift register is primarily used where low power dissipation and/or high noise immunity is desired.

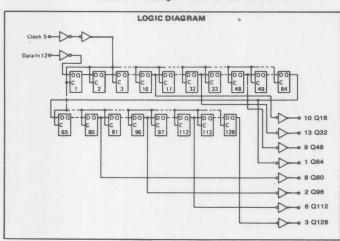
- Diode Protection on All Inputs
- Fully Static Operation
- Cascadable to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin, lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C



## **CMOS LSI**

(LOW-POWER COMPLEMENTARY MOS)

128-BIT STATIC SHIFT REGISTER.





CERAMIC PACKAGE

P SUFFIX
PLASTIC PACKAGE
CASE 646

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

**BLOCK DIAGRAM** -010 016 Q32 -0 13 120-Q48 -09 -01 0.64 080 -08 -02 096 Clock 0112 -0 6 Q128 -0 3 V<sub>DD</sub> = Pin 14 Pins 4 and 11 not used. VSS = Pin 7

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		9.597	6356	VDD	T	ow*		25°C	SHIP THE	Thi	igh °	
	Characteri	stic	Symbol		Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Vol	tage	"0" Level	VOL	5.0	-	0.05		0	0.05	andreit n.	0.05	Vdc
Vin = V	DD or 0	08		10	-	0.05	-	0	0.05	Robert Bald	0.05	MILE
	0.8	40	1. 44	15	-	0.05	-	0	0.05	Politica Don	0.05	RUT
		"1" Level	VOH	5.0	4.95	191	4.95	5.0	-	4.95	ADU AGAIS	Vdc
$v_{in} = 0$	or V <sub>DD</sub>		OH	10	9.95	1497	9.95	10		9.95	D ou do	0
		808		15	14.95	_	14.95	15	13 (30)	14.95	12/11/18	
Input Volta	oe .	"O" Level	VIL					019.43.00	217111	1	W.BUT	Vdc
	1.5 or 0.5 Vo	1 - 128 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -		5.0		1,5	-	2.25	1.5	0.01 = 1	1.5	1
	9.0 or 1.0 Vo		908	10	- 1	3.0	-	4.50	3.0	- 11	3.0	Sport C
	13.5 or 1.5 V		220	15	-	4.0		6.75	4.0	tislos	4.0	(43)
		"1" Level	VIH	80								Vdc
(Va - (	0.5 or 4.5 Vo		-111	5.0	3.5	st 1	3.5	2.75	_	3.5	Puras Fran	the Page 1
	1.0 or 9.0 Vo		-	10	7.0	_	7.0	5.50		7.0		
	1.5 or 13.5 V		1	15	11.0	_	11.0	8.25	_	11.0	-	
Output Drive	e Current (A	I Davisal	Louis	10.0	1	- 1	11.0	0.20		11.0	10 X 20 X 3	mAdo
(VOH		Source	ОН	5.0	-3.0	- 1	-2.4	-4.2	_	-1.7	_	IIIAUC
(VOH =		Source		5.0	-0.64		-0.51	-0.88		-0.36		
(VOH =		10-	00-	10	-1.6	boot-	-1.3	-2.25		-0.9		
	13.5 Vdc)	88-	01-	15	-4.2	PCIS***	-3.4	-8.8		-2.4		
· · · ·					-	-	-	-		-		-
(VOL =		Sink	IOL	5.0	0.64		0.51	0.88	-	0.36	-	mAdd
(VOL =		1000	350	10	1.6	347 -	1.3	2.25	-	0.9	N NEWS IN	SPACE
(VOL =		109	188	15	4.2	-	3.4	8.8	-	2.4	_	
		L/CP Device)	ГОН									mAdo
(VOH =		Source	200	5.0	-2.5	13/12 -	-2.1	-4.2	-	-1.7		
(VOH =	4.6 Vdc)	097	0.000	5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(VOH = !			180	10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(VOH =	13.5 Vdc)			15	-3.6	- la	-3.0	-8.8	Zimi?	-2.4	Louis Pier	6000
(VOL = 0	0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdo
(VOL = (	0.5 Vdc)		-	10	1.3	- 1	1.1	2.25	-	0.9	-	
(VOL =	1.5 Vdc)	and the latest transport	AND DESCRIPTION	15	3.6	-	3.0	8.8	-	2.4		- Contraction
Input Currer	nt (AL Devic	e)	lin	15	ionomi.	± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdc
Input Currer	nt (CL/CP D	evice)	lin	15	-	± 0.3	-	±0.00001	± 0.3		± 1.0	μAdc
Input Capac	itance		Cin	_	1.	-		5.0	7.5	-		pF
(Vin 0)			-111									
Quiescent Ci	urrent (AL C	Device)	IDD	5.0	-	5.0	-	0 010	5.0	-	150	μAdc
(Per Pack	age)		00	10	-	10	-	0.020	10	-	300	
		281803	WAS ON	15	TENT O	20	in stance	0.030	20	-	600	
Quiescent Ci	urrent (CL/C	P Device)	IDD	5.0	-	50	-	0.010	50	-	375	μAdc
(Per Pack			.00	10	_	100		0.010	100		750	I AAGC
	-301			15	_	200	_	0.030	200		1500	
Total Supple	Current**1		IT	5.0			1 - 11					1
	c plus Quieso		"1	10	-		T = (1	94 µA/kHz	T + IDD			μAdc
Per Pack		.ent,					17 = (3	.81 µA/kHz	DD			
	pF on all ou	staute all		15			1T = (5	.52 μA/kHz	ססי ייי			
(CF 20	pr on all or switching)	ithats' 911										

\*T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = + 125°C for AL Device, +85°C for CL/CP Device.

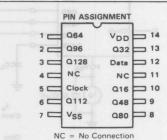
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: I  $_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V  $_{DD}-V_{SS}$ ) in volts, f in kHz is input frequency, and k = 0.004.



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

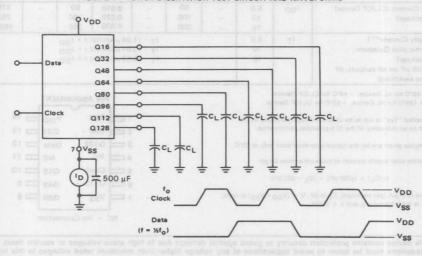
SWITCHING CHARACTERISTICS\* (C1 = 50 pF TA = 25°C)

Char	acteristic			Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	Muni	W-dyT	1970	tTLH.	509	Thirmy3.	500	Charten	ns
tTLH, tTHL = (1.5 ns/pF)				†THL	5.0	167	100	200	V happini Vi
tTLH, tTHL = (0.75 ns/pF) CL + 12.5 ns				80.0 L	10	11/4/1	50	100	
tTLH, tTHL = (0.55 ns/pF	) CL + 9	.5 ns		land I	15	-	40	80	w myV
Propagation Delay Time		10.19	20.5	tPLH.	T 08	HDV	leve I "I"		ns
Clock to Q				TPHL		BUT 1		G/G/F 10 G	= 66V
tPLH tPHL = (1.7 r	s/pF) CL	+ 515 ns		10.1	5.0	-	600	1200	
tpLH, tpHL = (0.66					10		250	500	500
tpLH, tpHL = (0.5 m	s/pF) CL	+ 145 ns			15	214	170	340	ted A chillian
Clock Pulse Width	3.0	02.6		twH	5.0	600	300	V D. Tip D. R.	ns
(50% Duty Cycle)				0.8	10	220	110	FOLE OF LS V	= 0V1
					15	150	75	-	
Clock Pulse Frequency		atic	3.8	fcl	5.0	-	1.9	1.1	MHz
				- 0.9	10	- 1	5.6	3.0	- OV0
			0.01		15	-	8.0	4.0	= ov
Data to Clock Setup Time	1000000			t <sub>su(1)</sub>	5.0	-20	-170	Al commed se	ns
				0.8	10	-10	-64	289001	HOM?
				48.0	15	0	-60	4.6.Vot.)	NOW THE
				t <sub>su</sub> (0)	5.0	-20	-91	0.5 V=1	ns
				4 2 1 2 4	10	-10	-58	(3)4/E 51	HOVI
				1 16	15	0	-48	1.00 V 9.00	e aesko
Data to Clock Hold Time		2:25	6.1	th(1)	5.0	350	263	(±)V, 8.0)	ns
				- 1 54	10	165	109	1.5 V#1	JOVI
					15	155	100	OS introduction	nO marruC
				th(0)	5.0	350	267	A-V d S	ns
				1.52	10	200	140	( +V 8.5	HOV9.
8.0-		88.8 -	1.1-	E.1	15	140	93	9.5 V=)	HOVA.
Clock Input Rise and Fall	Times			tr, tr	5.0		_	15	μs
				52   -	10	377	Sint-	5 / 5 /	LOVE.
				1 2 14	15	- 1	-	4000	5 WWW.

\*The formulas given are for the typical characteristics only at 25°C.

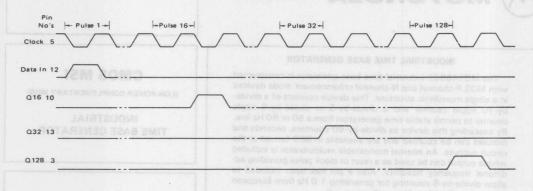
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

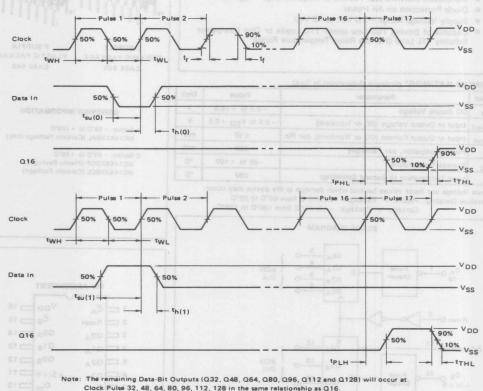


# MC14562B





### AC TEST WAVEFORMS



Clock Pulse 32, 48, 64, 80, 96, 112, 128 in the same relationship as Q16.

#### INDUSTRIAL TIME BASE GENERATOR

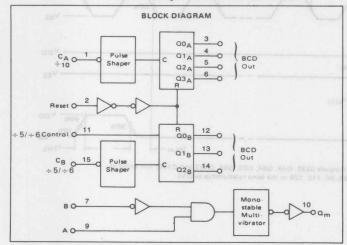
The MC14566B industrial time base generator is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter to permit stable time generation from a 50 or 60 Hz line. By cascading this device as divide-by-60 counters, seconds and minutes can be counted and are available in BCD format at the circuit outputs. An internal monostable multivibrator is included whose output can be used as a reset or clock pulse providing additional frequency flexibility. Also a pin has been included to allow divide-by-5 counting for generating 1.0 Hz from European 50 Hz line. Pin 11 = VDD will cause ÷5.

- Negative Edge Triggered Counters for Ease of Cascading
- Pulse Shapers on Counter Inputs Accept Slow Input Rise Times
- Monostable Multivibrator Positive or Negative Edge Triggered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

#### MAXIMUM RATINGS\* (Voltages Referenced to Voc.)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin, Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin, lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

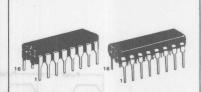
\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C
Ceramic "L" Package: -12mW/°C from 100°C to 125°C



## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL
TIME BASE GENERATOR



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT VDD 16 1 CA CB 15 2 [ Reset Q2B 14 200 4 01A Q18 13 Q0B 12 Q2A 5/÷6 11 6 = Q3A B am **10** □9 VSS

.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to Vec)

	3 40	10/101	VDD	Tic	ow*		25°C		Th	igh *	
Characteristi	с	Symbol	Vdc	Min	Max	Min	Тур #	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	ACTION C. P.	0.05	Vdc
$V_{in} = V_{DD}$ or 0	136		10	_	0.05	-	0	0.05	COLUMN COLUMN CO.	0.05	PLET'
·III ·BB s. s	40	-	15	-	0.05		0	0.05	duna para	0.05	4211
	"1" Level	VOH	5.0	4.95	5.137	4.95	5.0		4.95	minut House	Vdc
$V_{in} = 0$ or $V_{DD}$		.01	10	9.95	Frids.	9.95	10	a + har	9.95	* 31497 .	119
	530	-	15	14.95		14.95	15	PER	14.95	- 18/ds 1	297
Input Voltage	"0" Level	VIL		11.00		14.00	10	20.0	14.55	Supply of	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		1.	5.0	-1	1.5	_	2.25	1.5	R ama T	1.5	1
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	930	M	10		3.0	-	4.50	3.0	Talladi	3.0	HEST.
(V <sub>O</sub> = 13.5 or 1.5 Vdc)	215	-	15		4.0	_	6.75	4.0	No Galan	4.0	448
100 10.5 01 1.5 100	"1" Level	VIH	10		4.0		0.70		20130		100
(VO = 0.5 or 4.5 Vdc)		*IH	5.0	3.5	DHOUGH	3.5	2.75		3.5	लक्षांमा कर्मच	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)	909	1200 -	10	7.0		7.0	5.50	1	7.0		1
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	125	000	15	11.0		11.0	8.25		11.0		
Output Drive Current (AL	The state of the s	lavi	13	11.0		11.0	0.23		11.0		mAdo
(VOH = 2.5 Vdc)	Source	ТОН	5.0	-3.0	Diggs	-2.4	-4.2		-1.7	atio Wy astu	MAGG
(V <sub>OH</sub> = 4.6 Vdc)	Source	1288	5.0	-0.64		-0.51	-0.88	i a 🗍 i a a	-0.36		
(V <sub>OH</sub> = 9.5 Vdc)	125	008	10	-1.6		-1.3	-2.25	1	-0.9		
(V <sub>OH</sub> = 13.5 Vdc)	08	270	15	-4.2		-3.4	-8.8	_	-2.4		
	0				-	-	-		-	19011 BILL	100
(V <sub>OL</sub> = 0.4 Vdc)	Sink	IOL	5.0	0.64	10, - 1	0.51	0.88	-	0.36	-	mAde
(V <sub>OL</sub> = 0.5 Vdc)	20 1		10	1.6	-	1.3	2.25	-	0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)	1-22-1-1		15	4.2	-	3.4	8.8	-	2.4	-	
Output Drive Current (CL/		ОН						9/1	T 062 30	enith arru	mAdd
$(V_{OH} = 2.5 \text{ Vdc})$	Source		5.0	-2.5	POLIT.	-2.1	-4.2	-	-1.7	-	-
$(V_{OH} = 4.6 \text{ Vdc})$	Sinsi, Lessia		5.0	-0.52	BHTE	-0.44		-	-0.36	-	
$(V_{OH} = 9.5 \text{ Vdc})$	21111111111111		10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(V <sub>OH</sub> = 13.5 Vdc)			15	-3.6		-3.0	-8.8	-	-2.4		
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	OL	5.0	0.52	DINE	0.44	0.88	-	0.36	-	mAdd
$(V_{OL} = 0.5 \text{ Vdc})$	006	008	10	1.3	-	1.1	2.25	-	0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)	1000	2008	15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)		l <sub>in</sub>	15		± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdo
nput Current (CL/CP Devi	ice)	lin	15	behinstel.	± 0.3	on my desire	±0.00001	± 0.3	-	± 1.0	μAdd
Input Capacitance (V <sub>in</sub> = 0)		Cin	-		-	-	5.0	7.5		-	pF
Quiescent Current (AL Dev	vice)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdd
(Per Package)			10		10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	
Quiescent Current (CL/CP	Device)	IDD	5.0	_	20	_	0.005	20	_	150	μAdd
(Per Package)	## twitters	WAW USE	10	1831 8	40	ES REPRIC	0.010	40	-	300	
			15	_	80	_	0.015	80	-	600	1
Total Supply Current**†	g	J-IT-00	5.0			r = (1	.0 μA/kHz)	f + los			μAdo
(Dynamic plus Quiescer	nt,		10				.0 μA/kHz)				J
Per Package)	HOR K		15				.0 μA/kHz)				
(C <sub>1</sub> = 50 pF on all outp	outs, all	St. I				1 13	O AMINITZI	00			
buffers switching)	400	Manager !	N								

 $<sup>^*</sup>T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ V1k}$$

where:  $I_{\mbox{\scriptsize T}}$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{\mbox{\scriptsize DD}}-V_{\mbox{\scriptsize SS}})$  in volts, f in kHz is input frequency, and k=0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \in (V_{in} \text{ or } V_{out}) \in V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS\* (C1 = 50 pF. TA = 25°C)

Characteristic	3095		Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time  tTLH: tTHL = (1.5 ns/pF) CL + 25  tTLH: tTHL = (0.75 ns/pF) CL + 1  tTLH: tTHL = (0.55 ns/pF) CL + 9	2.5 ns	mitel	tTLH. tTHL	5.0 10 15	Symbol 1004	100 50 40	200 100 80	ns Hay toaroc QV = mV
Propagation Delay Time, Clock to Q3, tp_H, tpHL = (1.7 ns/pF) C_L + 13 tp_H, tpHL = (0.66 ns/pF) C_L + 4 tp_H, tpHL = (0.5 ns/pF) C_L + 29	tPLH, tPHL	5.0 10 15	HOY	1450 530 320	4500 1500 1000	ns v 0 = mV		
Propagation Delay Time, Reset to Q3, tpHL = (1.7 ns/pF) CL + 845 ns tpHL = (0.66 ns/pF) CL + 282 ns tpHL = (0.5 ns/pF) CL + 185 ns			tPHL	5.0 10 15	=	930 315 210	3000 1000 750	ns 2 - ovi
Clock Pulse Width	2.78 5.50 6.25	8.6 0.5 0.17	<sup>®</sup> WH(cl)	5.0 10 15	1200 400 270	400 125 90	Lanv B & so Lanv B if so abv # 7.1 so	0 = 08) 1 = 0 V1 1 = 10 V2
Reset Pulse Width	-4.2 -0.88 -2,25	4.5- 18:0- 6:1- 4.5-	₹WH(R)	5.0 10 15	1200 400 270	400 125 90	5 Vaci 5 Vaci 5 Vaci	ns HO
Clock Pulse Frequency	0.08 2.25 8.8	12.0 C.1 2.8	fcl	5.0 10 15	101	1.0 2.5 4.2	0.3 1.0 1.5	MHz
Clock Pulse Rise and Fall Time	0.06 - 0.16 - 2.15	1.5- 50.0- 1.7-	tTLH, tTHL	5.0 10 15		No Limit	6 Vec) 8 Vec) 8 Vec)	
Monostable Multivibrator Pulse Width	SR 0 ac.0 8/8	800.0 1.f 0.f	tWH(Q <sub>m</sub> )	5.0 10 15	1200 400 300	2800 900 600	Gay a Gay a	0 - 30 VI

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

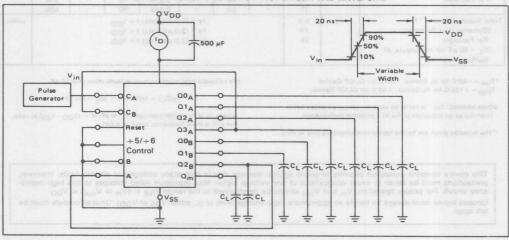
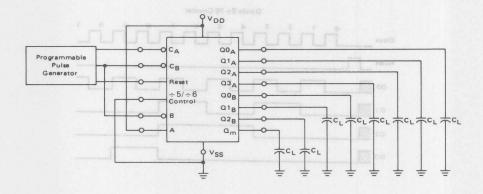
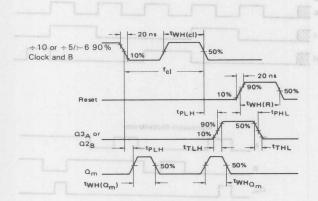


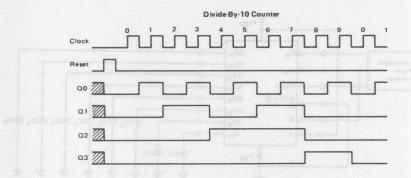
FIGURE 2 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

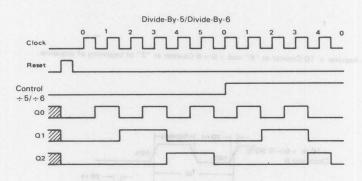


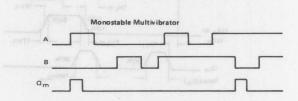
Note: Assume  $\div$  10 Counter at "6" and  $\div$  5/ $\div$  6 Counter at "2" at beginning of sequence.



PARTON AND THE TIMING DIAGRAM

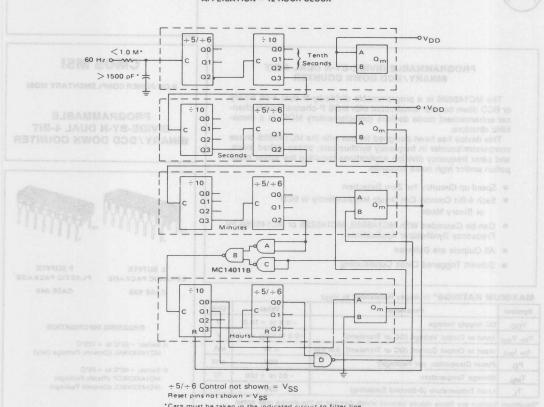






= Don't Care

APPLICATION - 12 HOUR CLOCK



\*Care must be taken in the indicated circuit to filter line transients which may cause "false" counting.

### PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BINARY/BCD DOWN COUNTER

The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14568B, MC14522B or MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning

MAXIMUM RATINGS\* (Voltages Referenced to Vss)

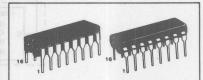
Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin, lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE
DIVIDE-BY-N DUAL 4-BIT
BINARY/BCD DOWN COUNTER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

**BLOCK DIAGRAM** CTL = Low for Binary Count CTL = High for BCD Count P1 P2 P3 CTL<sub>1</sub> CTL<sub>2</sub> P4 P5 P6 P7 V<sub>DD</sub> = Pin 16 10 V<sub>SS</sub> = Pin 8 15 0 Q BINARY/BCD BINARY/BCD Clock O 9 Clock Counter #1 Counter #2 Load Zero Detect Cascade O-7 Zero Detect Encoder

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

	may7 KA		VDD	Tic	w*		25°C		Th	igh °	
Characteristi		Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	L	0.05	-	0	0.05	Section .	0.05	Vdc
$V_{in} = V_{DD}$ or 0	001	00	10	- 3	0.05	_	0	0.05	-	0.05	Outpu
001	190		15	_	0.05	_	0	0.05	-	0.05	
	"1" Level	VOH	5.0	4.95	-	4.95	5.0	_	4.95	_	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	000	OH	10	9.95	N33-	9.95	10		9.95	10517-10 T	1
007	98		15	14.95	-	14.95	15	_	14.95		200000
nput Voltage	"0" Level	VIL	81	11.00		11.00	1.0		1 1.00		Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	O Level	*IL	5.0	-	1.5	-	2.25	1.5	-	1.5	V 00
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$	420		10		3.0	_	4.50	3.0	205	3.0	D-mwT
$(V_0 = 13.5 \text{ or } 1.5 \text{ Vdc})$		TOTAL S	15		4.0	_	6.75	4.0	- Buglist	4.0	10%
(VO = 13.5 01 1.5 VdC	"1" Level	VIH	13	-	4.0	-	0.73	4.0		4.0	-
(VO = 0.5 or 4.5 Vdc)		VIH	5.0	3.5		1 25	2.75		3.5		Vdc
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$	gre	+	10	7.0		3.5	5.50		7.0	haune	00
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	285	0.7	15		I I	7.0		I			
	3.99		15	11.0	-	11.0	8.25		11.0		-
Output Drive Current (AL	TO STATE OF THE ST	10Н			phip		-4.2		1.70	velot d	mAdd
$(V_{OH} = 2.5 \text{ Vdc})$	Source	1000	5.0	-3.0		-2.4		-	-1.7	Detect of	and a
$(V_{OH} = 4.6 \text{ Vdc})$			5.0	-0.64	-	-0.51	-0.88	-	-0.36		
$(V_{OH} = 9.5 \text{ Vdc})$	001		10	-1.6	-	-1.3	-2.25	-	-0.9	-	
(V <sub>OH</sub> = 13.5 Vdc)	200		15	-4.2	-	-3.4	-8.8	-	-2.4	-	
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	Brann	mAd
(VOL = 0.5 Vdc)	285		10	1.6	-	1.3	2.25	-	0.9	-	
(VOL = 1.5 Vdc)			15	4.2	-	3.4	8.8	-	2.4	-	-
Output Drive Current (CL.	(CP Device)	ТОН	10.0	1	927				10000	COPPL SQL	mAde
(VOH = 2.5 Vdc)	Source	4061	5.0	-2.5	-	-2.1	-4.2		-1.7	-	
(V <sub>OH</sub> = 4.6 Vdc)		211	5.0	-0.52	-	-0.44	-0.88		-0.36	-	
(VOH = 9.5 Vdc)	35		10	-1.3	- 1	-1.1	-2.25	_	-0.9	port actual	
(V <sub>OH</sub> = 13.5 Vdc)	a.e. [		15	-3.6	1	-3.0	-8.8	_	-2.4	Section of the section of	Clouled
(V <sub>OL</sub> = 0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	_	0.36	-	mAde
(V <sub>OL</sub> = 0.5 Vdc)	Ollik	,OL	10	1.3	-	1.1	2.25		0.9		-
$(V_{OL} = 1.5 \text{ Vdc})$	T10012 (20)		15	3.6	,H,717	3.0	8.8	BOW	2.4	uelFl out.d	Clock
nput Current (AL Device)		1	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAdo
		lin		-		-	-		_		-
nput Current (CL/CP Dev	ice)	lin	15	-	± 0.3	ud allege	±0.00001	± 0.3	100 TEL 100	± 1.0	μAdd
Input Capacitance (V <sub>in</sub> = 0)		Cin	-	-	-	004000	5.0	7.5	n ncession	if res —a bot	pF
Quiescent Current (AL De	vice)	IDD	5.0	12345W	5.0	M/3-	0.005	5.0	-	150	μAdd
(Per Package)	The state of the s		10		10	-	0.010	10	-	300	F 19 6
			15	1 2800	20	-	0.015	20	-	600	
Quiescent Current (CL/CP	Device)	IDD	5.0	_	50	6, 44	0.005	50	-	150	μAde
(Per Package)			10	_	100	1 -	0.010	100	_	300	p
	Sand Sand	1	15	-	200	130	0.015	200	4-47	600	
Total Supply Current**†	Per contract	IT	5.0			10.50	μA/kHz)f+	las	-	000	μAdo
(Dynamic plus Quiesce	nt	1	10	-			μΑ/KHZ) f +				μΑθί
Per Package)			15				μΑ/kHz) f +				
(C <sub>1</sub> = 50 pF on all out	nuts all	Dige.	13	1 3 3 4		(1.95	HA/KHZ)T	'DD			
buffers switching)	pu.s, an										

 $<sup>^*</sup>T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

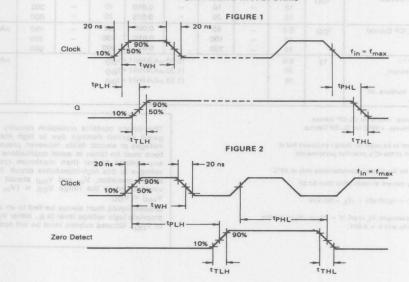
<sup>†</sup>To calculate total supply current at loads other than 50 pF:

SWITCHING CHARACTERISTICS (CL = 50 pF, TA = 25°C)

					veds	VDD		All Types		
	Char	racteristic			Symbol	Vdc	Min	Typ#	Max	Unit
Output Rise Tim	e	80.0	D-		tTLH	5.0	-	100	200	ns
					80.0	10	-	50	100	
						15		40	80	
Output Fall Tim	e 88.8		01	200	tTHL	5.0	_	100	200	ns
					- 1 66	10	-	50	100	
						15	TV.	40	80	
Turn-On Delay 1	ime	84	92.5	F BUY	tPLH	9.8			35 V 2 0 se 2	ns
Zero Detect	Output				0.5	5.0	_	420	700	
					0.8	10	-	175	300	
						15	177V	125	250	
Q Output					- 1 8	5.0	-	675	1200	ns
					1 0	10		285	500	
					- 1 0	15	-	200	400	
Turn-Off Delay	Time .		5.2	5.5-	tPHL	The same	PU	TEDINACI	THE THEORY S	ns
Zero Detect	Output					5.0	-	380	600	
						10	-	150	300	
						15	-	100	200	* KOVI
Q Output						5.0	-	530	1000	ns
						10		225	400	
	1.8		8.8	37		15	-	155	300	"JOV
Clock Pulse Widt	h				twH	5.0	300	100	(3) (5mg) 4	ns
					- 31	10	150	45	Eves	= weW
	38.9-		田良.0-	55.0-	130	15	115	30	75v 9.4	E MON
Clock Pulse Fre	quency		-2.25	1,1-	fcl	5.0	-	3.5	2.1	MHz
					1 30	10	-	9.5	5.7	HOV
b4m -	0.38		88.9	Nik G	1 - 1 58	15	101	13.0	7.8	" HOVE
Clock Pulse Rise	and Fall T	ime	05.5		tTLH, tTHL	5.0			0.5 Vdc)	μς
					1 2	10		NO LIMIT		IVOL =
					1.00	15				multiple

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## SWITCHING WAVEFORMS



### INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, P5, P6, P7 (Pins 11, 12, 13, 14) — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) — Preset data is decremented by one on each positive transition of this signal.

### **OUTPUTS**

Zero Detect (Pin 1) — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

**Q** (Pin 15) — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

#### CONTROLS

Cascade Feedback (PIn 7) — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are "don't cares." Refer to Table 1 for output characteristics.

CTL<sub>1</sub> (PIn 2) — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

CTL<sub>2</sub> (PIn 10) — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

### SUPPLY PINS

Vss (Pin 18) — Negative Supply Voltage. This pin is usually connected to ground.

**Vpp (PIn 16)** — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

#### **OPERATING CHARACTERISTICS**

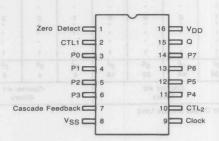
The MC14569B is a programmable divide-by-N dual 4-bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL<sub>1</sub> and CTL<sub>2</sub>.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock

cycles, one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14568B, MC14522B or the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to "0", Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to Vpp.

## PIN ASSIGNMENT



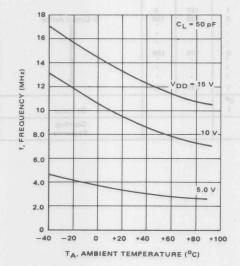


TABLE 1 - MODE CONTROLS (Cascade Feedback = Low)

	Control		Divide Ratio		
CTL <sub>1</sub>	CTL <sub>2</sub>	Zero Detect	Q		
0	0	256	256		
0	1	160	160		
1	0	160	160		
1	1	100	100		

Note: Data Preset Inputs (P0-P7) are "Don't Cares" while Cascade Feedback is Low.

TABLE 2 — MODE CONTROLS (CTL<sub>1</sub> = Low, CTL<sub>2</sub> = Low, Cascade Feedback = High)

nia sidT	egation	/ ylaqui8		eset outs	PI) 25	y	wat y		ride	and goes high an one clock cycle noremented to zero.
P7	P6	P5	P4	Р3	P2	P1	PO	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	256	256	Max Count
0	0	0		0	0	0	- 1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1.	3	Х	
	FILL W						FEMALE		Х	
	La i		100	-	Company City	Supplied in	13/0 -03/	TASTER	X	
				1 100	ALTO-DAY	TOAR	DEA	Latin.	X	
0	0	0	0	1	1	1	1	15	X	The MC145699 is a programme
0	0	0	1	0	0	0	0	16	X	
t to lugi	so with a	deglas I	DIN'S EU	dengava i	phints! a	199	DEXTIG	SETEO-G S	X	all down country. This country
anidat o	p2) ten	tures arres	dividual 16	com son	a aberra	ED .	01.079	Translatin util	X	a., present in BCD or binary out
			( along	Agde Co	ugin S. I	1963	ad As	an eomeu	Step The	A For each counter, the bound
0	4 401 6	ESBEN.	01,00	pribasa	an nod		000	20	X	riche Ad Anticonadapul sesor
edt.	0	B, the f	0	0	0	0	0	32	X	mun) or a low flot binary count
réligadas	0.00 10	en etuah	o spetel	d Toro	us "Q. su	oni -				TL, and CTLs.
iwottel	wit for	iso.i bri	Clock	.00 03	betser	100	red be	rogianna	X	The divide ratio N 69 being the
Casca	endie	least si.	14858B	1784 terri	1 .1010	100	one b	thy toson	X	e present inputs PO to PY) is out
0	1	0	0	0	0	0	0	64	X	supo erit an noce as talauco e
							- Abotto	ANDRIA I	X	re, a division ratio of one is not
									х	
									×	
0	1	1	1	1	1	1	1	127	x	
1	0	0	0	0	0	0	0	128	128	Q Output Active
						1 :		100.10		
								1		01
1	0	0	0	1	0	0	0	136	136	
	av izz	10		Tin loning C	.oroš		. 1			
	0			(3)				1.		
1	1	1	1	1	1	1	1 -	255	255	Color 8
27	26	25	24	23	22	21	20	200		
128	64	32	16	8	4	2	1	1		Bit Value
		ter #2	2	ED 69		ter #1		31		Counting Sequence

X = No Output (Always Low)

~

TABLE 3 — MODE CONTROLS (CTL1 = High, CTL2 = Low, Cascade Feedback = High)

				puts					ride	199		
P7	P6	P5	P4	Р3	P2	P1	PO	Zero Detect	Q	19	Comments	
0	0	0	0	0	0	00	0	160	160	0	Max Count	10
0	0	0	0	0	0	0	0	X 2	X	- 6	Illegal State Min Count	
0	0	0	0	0	0	11	1	3	X	1 12	Will Count	
				8.	1			1. 1	X			
				×.					X	Total By		
				*					×			
0	0	0	0	- × 1	0.0	0	1	9	X	0		
0	0	0	1	7.0	0	0	0	10	X			
			. 1	10.					×			
				1								
				X	100				X			
0	0	0	0	X o	0	0	1 0	19	X	0		
			·	X .					X			
				N . 1					×			
				z.					×			
0	0	1	1	0	0	0	0	30	×			
				1					X			
				1 3 1		10.5	15.	1 9 1	×			
				R.	00.	10.	0 .	9.	×	9		
0	1	0	0	0	0	0	0	40	X	11944		
				10.1	on.	0	1	0.	×			
		1			200	1 .	5 .	2 1	×			
									X			
0	1	0	1	0	0	0	0	50	X			
				1	1	1 .	1	1 . 1	1 P			
									X			
	evitoA jus	mo o		651	128	0.	0	0	X	0		
0	1 1	1	0	0	0	0	0	60	X			
	. 1								X	4 14		
				5.60	287	8.	0 .	9.	X	1		
0	1	1	1	0	0	0	0	70	×			
	1							1	x	- 1		
	. 7			081	807	1		1	×			
	soldald.					79 .	12.	19.	×	18		
1	0	0	0	0	0	0	0	80	80	97	Q Output Active	Э
	- Statement	18 .					1.6 163	6			COUNTY SE	
				•	1			-			and the same of the same of	
1	0	0	1	0	0	0	0	90	90		(sets) appropriate total	
1	1	1	1					450	150			
:	1	:	1	0	0	0	0	150	150	SELECT TO		
:				1	1		1:			I Ingertia		
1	1	1	1	1	0	0	1	159	159	10 F	*	
80	40	20	10	8	4	2	1		, 55		Bit Value	
-		ter #2	10	-		nter #1	1					
		ter #2 nary				iter #1					Counting Sequence	

X = No Output (Always Low)

TABLE 4 — MODE CONTROLS (CTL<sub>1</sub> = Low, CTL<sub>2</sub> = High, Cascade Feedback = High)

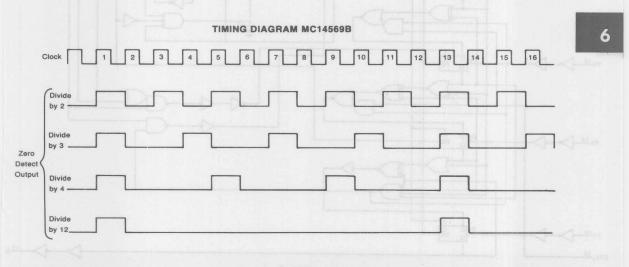
				ues	199				ride itio	17		
P7	P6	P5	P4	Р3	P2	P1	PO	Zero Detect	Q	59	Comments	
0	0	0	0	0	0	0	0	160	160	0	Max Count	0
0	0	0	0	0	0	0	1	X	X	0	Illegal State	
0	0	0	0	0	0	01	0	2	X	0	Min Count	
0	0	0	0	0	0	1	1.	3	X	0		
				Q. 1					×			
				× . 1		· .			X			
0	0	0	0	× 1	1	1	01	15	×	0		
0	0	0	1	0	0	0	0	16	x	1		
	•			2.				1.0	x	3-11		
				- x:		× • /			×			
				× -				1	×	3		
0	0	0	1	- 1	1	. 1	- 1	31	X	1		
0	0	1	0	0	0	0	0	32	X	0		
•				X.	-		2.	1	X	1		
				X.					×	10		
•				18		- 1			×	100		
0	0	1	1	0	0	0	0	48	×	1		
				× . 1						100		
				× •						100		
0	1	0	0	0	0	0	0	64	×	2 1		
	• • •			x ·	05 -	6.	0.	0.	8.	10 1		
				×						1		
0	1	0	1	0	0	0	0	80	×	18 19		
				× .				1		78		
					ns . 1					100		
0	1	1	1	0	0	0	0	112	×	17. 1		
				× .	1			1		12		
,												
1	0	0	0	0	0	0	0	128	128		Q Output Active	
				9:1	08 *	7:1	2 .	9:	9	0		
										1000		
1	0	0	1	0	0	0	0	144	144			
				8.		7.		2.				
1	0	0	-1	1	. 1	1	1	159	159		V	
2 <sup>7</sup> 128	2 <sup>6</sup> 64	2 <sup>5</sup> 32	2 <sup>4</sup> 16	2 <sup>3</sup>	2 <sup>2</sup>	21 2	20	-			Bit Value	
.20	BOAT SALES	ter #2			138	ter #1	9	1	0	-	Counting	-
		CD #2				nary		-			Sequence	

X = No Output (Always Low)

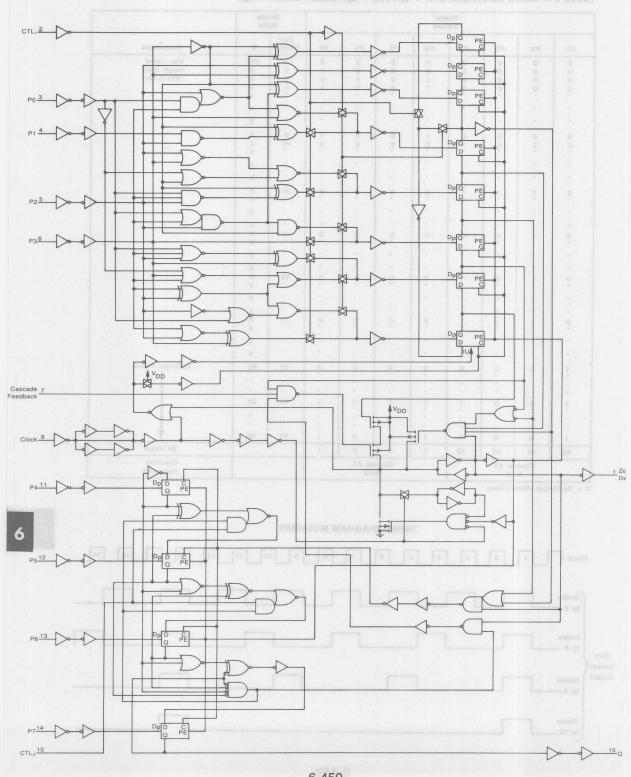
TABLE 5 — MODE CONTROLS (CTL<sub>1</sub> = High, CTL<sub>2</sub> = High, Cascade Feedback = High)

	ide tio					set				
Comments	Q	Zero Detect	PO	P1	P2	Р3	P4	P5	P6	P7
Max Count	100	100	0	0	0	0	0	0	0	0
Illegal State	×	X	1	0	0	0	0	0	0	0
Min Count	X	2	. 0	1	0	0	0	0	0	0
	×	3	1.	1.	0	0	0	0	0	0
										.
	X	+C [		THE STATE OF THE S				1.		
	X	- 14		4			4			
	X	9	1	0	0	1	0	0	0	0
	X	10	0	0	0	0	1	0	0	0
	x				2.		TI	-		
	bendan .	-C.T		-						
	X						the second			
	X	30	0	0	0	0	1 1	1	0	0
	X					.4				
	X						-			
	X	100	-	: 0			1			
	X	40	0	0	0	0	0	0	1 1	0
			. 1				P P			
	×	K.I	7	1.79						
	X	50	0	0	0	0	1009	0		0
	x	30								
	x									
	x	1								
	x	70	0	0	0	0	1	1	1	0
	X		•		•					•
	X		- 55							
	x						T 4.			
Q Output Active	80	80	0	0	0	0	0	0	0	1
G Culput Active										
		-					:			
	90	90	0	0	0	0	1	0	0	1
	90	90	0	0	00					:
THE PARTY		:					1			
	99	99	1	0	0	1	1	0	0	1
	99	99	-							
Bit Value			1	2	4	8	10	20	40	80
Counting Sequence				er #1	Count				Count	

X = No Output (Always Low)



# MC14569B LOGIC DIAGRAM



### TYPICAL APPLICATIONS

### FIGURE 6 — CASCADING MC14568B AND MC14522B OR MC14526B WITH MC14569B

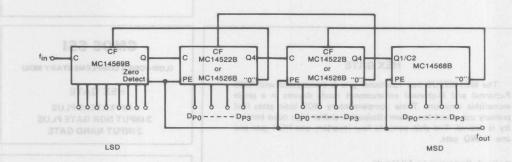
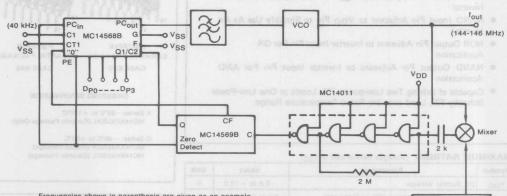


FIGURE 7 — FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER (Channel Spacing 10 kHz)



Frequencies shown in parenthesis are given as an example

Crystal Oscillator (143.5 MHz)



# MC14572UB

### HEX GATE

The MC14572UB hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

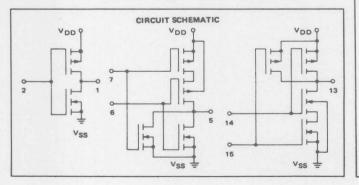
- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- NOR Input Pin Adjacent to V<sub>SS</sub> Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to VDD Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin. Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin-lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

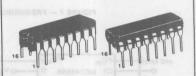


## **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

**HEX GATE** 

4 INVERTERS PLUS 2-INPUT NOR GATE PLUS 2-INPUT NAND GATE



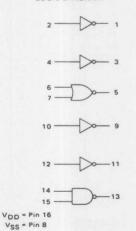
L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXUBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXUBCP (Plastic Package) MC14XXXUBCL (Ceramic Package)

### LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

	779.0	25280	VDD	T	ow*		25°C	9015,050	Thi	igh °	
Character	istic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0		0.05	-	0	0.05	10 Table	0.05	Vdc
$V_{in} = V_{DD}$ or 0	08	0.	10	-	0.05	-	0	0.05	1073401	0.05	N. La
130	58		15	-	0.05	-	0	0.05	72735/	0.05	ITT
	"1" Level	VOH	5.0	4.95	NOT-	4.95	5.0	-	4.95	Sent Times	Vdc
Vin = 0 or VDD		011	10	9.95	-	9.95	10	30 98	9.95	a 8.11 × J	177
			15	14.95	-	14.95	15	112514	14.95	就也"	HTP.
Input Voltage	"0" Level	VIL						10 C.S.	In radio	Service .	Vdc
$(V_O = 4.5 \text{ or } 0.5 \text{ Vo}$	dc)		5.0	-	1.0	-	2.25	1.0	12117	1.0	Proping
$(V_O = 9.0 \text{ or } 1.0 \text{ V})$	dc)		10	-	2.0	-	4.50	2.0	miles z'el	2.0	177
$(V_O = 13.5 \text{ or } 1.5)$	/dc)	-	15	-	2.5	-	6.75	2.5	hen <u>6</u> 8.6)	2.5	520
- 56	"1" Level	VIH					4000 80	Con Trans	den en	- Jielly	101
$(V_O = 0.5 \text{ or } 4.5 \text{ Vol})$	dc)		5.0	4.0	- 0	4.0	2.75	in helpyl i	4.0	avig-autus	Vdc
$(V_O = 1.0 \text{ or } 9.0 \text{ Vol})$	dc)		10	8.0	-	8.0	5.50	-	8.0	-	
$(V_O = 1.5 \text{ or } 13.5)$	/dc)		15	12.5	-	12.5	8.25	of page 194	12.5	II. Thirties	MING N
Output Drive Current (A	AL Device)	ГОН									mAdc
(VOH = 2.5 Vdc)	Source		5.0	-1.2	-	-1.0	-1.7	-	-0.7	-	
(VOH = 4.6 Vdc)		- 18 m	5.0	-0.25	-	-0.2	-0.36	-	-0.14	-	
(VOH = 9.5 Vdc)			10	-0.62	-	-0.5	-0.9	-	-0.35	-	
(VOH = 13.5 Vdc)			15	-1.8	-	-1.5	-3.5	-	-1.1	-	
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
(VOL = 0.5 Vdc)		THE VALUE OF	10	1.6	ST BUILT	1.3	2.25	ONL.	0.9	-	
(V <sub>OL</sub> = 1.5 Vdc)			15	4.2	-	3.4	8.8	-	2.4	-	
Output Drive Current (C	CL/CP Device)	ГОН									mAdc
(VOH = 2.5 Vdc)	Source	0	5.0	-1.0	-	-0.8	-1.7	- 1	-0.6		
(VOH = 4.6 Vdc)			5.0	-0.2	-	-0.16	-0.36	-	-0.12	-	
(VOH = 9.5 Vdc)			10	-0.5	-	-0.4	-0.9	( - )	-0.3	-	
(VOH = 13.5 Vdc)			15	-1.4	-	-1.2	-3.5	-	-1.0	-	
(VOI = 0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdc
(VOL = 0.5 Vdc)		0.	10	1.3	-	1.1	2.25	-	0.9	-	
(VOL = 1.5 Vdc)		Al gineral	15	3.6	-	3.0	8.8	- 100	2.4	-	
Input Current (AL Devi	ce)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Current (CL/CP D	Device)	1 <sub>in</sub>	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdc
Input Capacitance	7-2	Cin	_		+	10-75	5.0	7.5	- 1000		pF
(V <sub>in</sub> = 0)		oin				200					
Quiescent Current (AL	Device)	IDD	5.0	-	0.25		0.0005	0.25	-	7.5	μAdc
(Per Package)	501.007	100	10	-	0.50	100	0.0010	0.50	-	15.0	A. 100
11 61 1 36110361			15	-	1.00	_	0.0015	1.00	-	30.0	
Quiescent Current (CL/	CP Davica)	lon	5.0	-	1.0	+	0.0005	1.0	-	7.5	μAdc
(Per Package)	C. Device)	IDD	10	1	2.0	-	0.0005	2.0	_	15.0	имос
ti et i ackage;			15		4.0		0.0010	4.0	_	30.0	
Total Supply Current**	+	IT	5.0	1	1	1== (	1.89 µA/kHz			00.0	μAdc
(Dynamic plus Quies		10	10				3.80 µA/kHz				MAGC
Per Package)	scent,	The Control of the Co	15				5.68 μA/kH2				
(C <sub>1</sub> = 50 pF on all o	outpute all	man M	15	1		17 = (:	5.00 μΑ/KH8	טטי די ו			
buffers switching)	dipats, an	MOS									1
Duriers switching)		11 M		1							1

\*Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

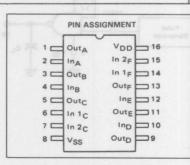
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_{\tau}(C_L) = I_{\tau}(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts, f in kHz is input frequency, and k = 0.006.



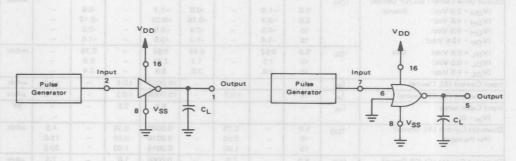
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this highimpedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must

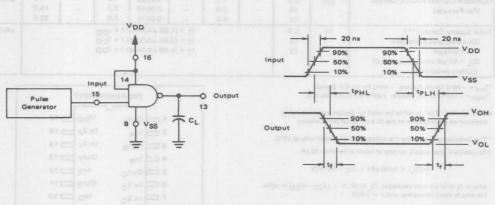
Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise Time	tTLH	Wide B	Tonioy8	21	Charles min	ns
tTLH = (3.0 ns/pF) CL + 30 ns	200	5.0	254	180	360	AND NAMED IN
tTLH = (1.5 ns/pF) CL + 15 ns	1 200	10	72	90	180	The Law
tTLH = (1.1 ns/pF) CL + 10 ns	I min	15	-	65	130	
Output Fall Time	tTHL	0 = 7	1-77	Thought Tree		ns
tTHL = (1.5 ns/pF) CL + 25 ns		5.0	72	100	200	- Lak
tTHL = (0.75 ns/pF) CL + 12.5 ns		10	- 1	50	100	1000
tTHL = (0.55 ns/pF) CL + 9.5 ns		15	7.0	40	80	Total view
Propagation Delay Time	tPLH,	6.0			B or o 5 Vol	ns
tpLH, tpHL = (1.7 ns/pF) CL + 5 ns	TPHL	5.0	-	90	180	1000 00
tpLH, tpHL = (0.66 ns/pF) CL + 17 ns	las II	10	-	50	100	- 201
tpLH, tpHL = (0.5 ns/pF) CL + 15 ns		15		40	80	1

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - SWITCHING TIME TEST CIRCUITS AND WAVEFORMS





# MC14580B

### 4 x 4 MULTIPORT REGISTER

The MC14580B is a 4 by 4 multiport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

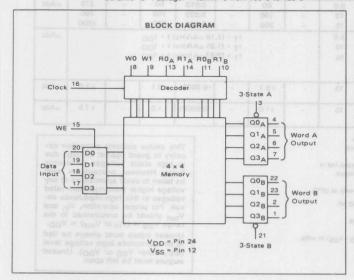
Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or one Lowpower Schottky TTL Load Over the Rated Temperature Bance
- Pin Compatible with CD40108

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
In. lout	Input or Output Current (PC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TI	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/"C from 65°C to 85°C Ceramic "L" Package: -12mW/"C from 100°C to 125°C



## CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

4 x 4 MULTIPORT REGISTER



L SUFFIX CERAMIC PACKAGE CASE 623



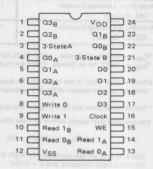
P SUFFIX
PLASTIC PACKAGE
CASE 709

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: - 40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

#### PIN ASSIGNMENT



		V <sub>DD</sub> Vdc	Tio	w	25°C			Thigh*		
Characteristic	Symbol		Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	10 7 415	4.95	-	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	- On	10	9.95	102400	9.95	10	5 wi b	9.95	225.4704	To a contract
		15	14.95	hel-un	14.95	15	ulate-urbai	14.95	norm House	Sections
Input Voltage "0" Level	VIL		resultation ar	alumi ma	Ita et			and a	often bee	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	11.	5.0	et de fi	1.5	To the	2.25	1.5	2000 TO	1.5	1
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		10	A	3.0	-	4.50	3.0	DIOM: UV	3.0	SULFORR
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15		4.0	-	6.75	4.0	10 sna	4.0	SUCTION
ABTAIDEN THE "1" Level	VIH							-	-	-
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	- 111	5.0	3.5	B 10 530	3.5	2.75	dus aigs	3.5	pritt pauly	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	_	7.0	5.50	dierett	7.0	05559330	Id Yan
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	-	15	11.0	- 1	11.0	8.25	_	11.0	_	
Output Drive Current (AL Device)	lau		11.0		11.0	0.20	trially de	11.0		mAdo
(VOH = 2.5 Vdc) Source	ІОН	5.0	-3.0	_	-2.4	-4.2		-1.7	on Oute	MAGG
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88	I I	-0.36	ALCO TO SER	The same of
(V <sub>OH</sub> = 9.5 Vdc)	C. activi	10	-1.6	1	-1.3	-2.25		-0.9	e Pinase	pai2
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2		-3.4	-8.8	VALUE +	-2.4	eriod/ on	
	-		-		-	-		-	711	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	1904 079	0.51	0.88	DOP-WILL	0.36	O to side	mAdo
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	DIVINETE(	1.3	2.25	YO TUBO	0.9	10029 1	wedq .
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	-	2.4	- 8	NES .
Output Drive Current (CL/CP Device)	ІОН					80	magn	efficie intel		mAde
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-2.5		-2.1	-4.2	-	-1.7		
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	1
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	910 <del>-</del> 316	-0.9	RAFING	<b>网络</b> 尼斯塔
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	bey-	-3.0	-8.8	1 There	-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	of For	0.44	0.88	-	0.36	dr allows 2	mAde
(VOL = 0.5 Vdc)		10	1.3	-	1.1	2.25	-	0.9		1
(VOL = 1.5 Vdc)		15	3.6	34 of 4 a	3.0	8.8	TEQU)	2.4	grisQuio, re	test tue
Input Current (AL Device)	lin	15	-	± 0.1	/E9 10	± 0.00001	±0.1	100 m	±1.0	μAdo
Input Current (CL/CP Device)	lin	15	-	± 0.3		±0.00001	±0.3	roid-resid	±1.0	μAdo
Input Capacitance	Cin	-	1000		_	5.0	7.5	matter and		DF
(Vin = 0)	oin					0.0	7.3	mulate	VIVE COR	1
Quiescent Current (AL Device)	E Stee	5.0	-	5.0	-	0.010	5.0		150	μAdd
(Per Package)	IDD	10	trebe to	10	ord of sta	0.020	10	den value	300	And
( cr rackage)		15	- 4	20	0 ment d	0.030	20	9" pour	600	enung
2			-		-	-	50	-		+
Quiescent Current (CL/CP Device)	IDD	5.0	-	50		0.010	100	-	375	μAdd
(Per Package)	in the	10	-	100	-	0.020	200	-	750	
		15	-	200		0.030	-	-	1500	-
Total Supply Current * * †	IT	5.0				.18 μA/kHz				μAdd
(Dynamic plus Quiescent,		10				.91 μA/kHz				
Per Package)		15	1.72		IT = (2	.67 μA/kHz	) f + 1DC	)		-
(CL = 50 pF on all outputs, all										1
buffers switching)										
Three-State Leakage Current	ITL	15	-	± 0.1	-	.0.00001	± 0.1	-	±3.0	μAdd
(AL Device)		MILLER		14, 1000		CHICAGO CO.		-		
Three-State Leakage Current	ITL	15	-	±1.0		•0.00001	± 1.0	11-11	± 7.5	μAdd
(CL/CP Device)				1	1	ALL LAND	Laborate Control			1

 $<sup>^*</sup>T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\rm in}$  and  $V_{\rm out}$  should be constrained to the range  $V_{\rm SS} \leqslant (V_{\rm in} \text{ or } V_{\rm out}) \leqslant V_{\rm DD}.$  Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{\rm SS}$  or  $V_{\rm DD}$ ). Unused outputs must be left open.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

where: IT is in  $\mu$ A (per package), CL in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.004.

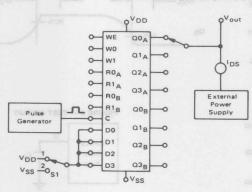
# MC14580B

SWITCHING CHARACTERISTICS\* (CI = 50 pF, TA = 25°C)

Characteristic	Symbol	V <sub>DD</sub>	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH, tTHL	5.0		100	200	ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns	(Figures 3 and 6)	10		50	100	-
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	(Figures 3 and 6)	15	7	40	80	Marin Taranta
Propagation Delay Time	tPLH, tPHL	5.0	200	650	1300	ns
Clock to Output	(Figures 3 and 6)	10		250	500	
	*	15	_	170	340	
Write Enable Setup Time	t <sub>su</sub>	5.0	800	400	_	ns
(Enabling a Write or Read)	(Figure 5)	10	300	150	-	
		15	200	100	-	rectured.
Write Enable Removal Time	trem	5.0	0	- 100	10	ns
(Disabling a Write or Read)	(Figure 5)	10	0	-50		2 1 1
		15	0	-35	-	
Setup Time**	t <sub>su</sub>	5.0	50	20		ns
Address, Data to Clock	(Figure 3)	10	30	0		Centere
		15	25	0		E C
Hold Time**	th	5.0	480	160	_	ns
Clock to Address, Data	(Figure 3)	10	195	65		
		15	150	50		
3-State Enable/Disable Delay Time	tpHZ, tpLZ	5.0		130	260	ns
	tpzH, tpzL	10	-	60	120	
	(Figures 4 and 7)	15	-	45	90	
Clock Pulse Width	t <sub>w</sub>	5.0	820	410	- Improved	ns
	(Figure 3)	10	330	165	of some	1
	B to A	15	220	110	+,,,,,,,,,	-

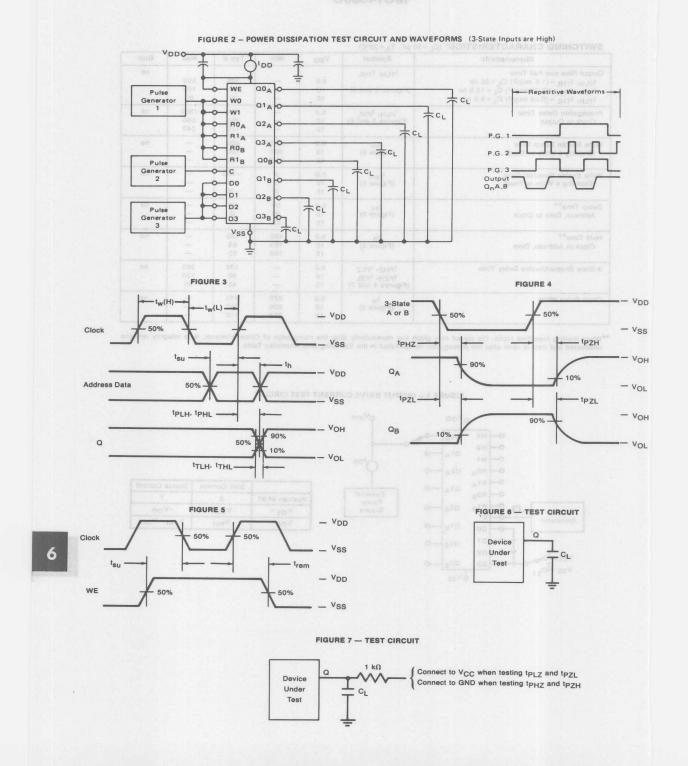
<sup>\*\*</sup>When loading repetitive highs, the output may glitch low momentarily after the rising edge of Clock. However, data integrity remains unaffected and data is valid after the propagation delays listed in the Switching Characteristics Table.

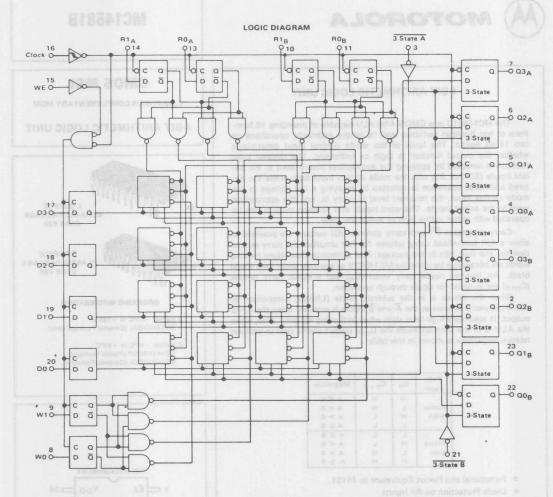
## FIGURE 1 - OUTPUT DRIVE CURRENT TEST CIRCUIT



	Sink Current	Source Current
Position of S1	2	1
V <sub>GS</sub> =	V <sub>DD</sub>	-V <sub>DD</sub>
V <sub>DS</sub> =	Vout	Vout - VDD

# MC14580B





TRUTH TABLE

Clock	WE	Write 1	Write 0	Read 1 <sub>A</sub>	Read 0 <sub>A</sub>	Read 1 <sub>B</sub>	Read 0 <sub>B</sub>	3-State A	3-State B	Dn	QnA	Q <sub>n</sub> B
7	1	0	1	0	1	0	1	1	1	1	1	1
	1	0	1	0	1	0	1	1 1 1	1	0	0	0
	X	X	×	×	×	×	×	1	1	×	No Change	No Change
X	X	X	×	×	×	×	X	0	0	X	Z	Z
0	×	×	×	×	×	×	Х	cont or a	escretefall	X	No Change	No Change
-1	X	X	X	X	X	X	X	1	1 10	×	No	No
_	1	0	0	0	¥ 1	81 1918	0	1	1	D <sub>n</sub> to	Change Contents of word 1	
-					Y I S	TOGYS	10-		arkment en	word	displayed	
	0	0	0	0	1	1	0	1 1 .00	brand i ve	Word 0	Contents of word 1	
- 1			85 - 10		PART L	903		-	750	altered	displayed	

Z = High Impedance X = Don't care

### 4-BIT ARITHMETIC LOGIC UNIT

The MC14581B is a CMOS 4-bit ALU capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 14-bit words. The level of the mode control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate  $\overline{(P)}$  and carry generate  $\overline{(G)}$  outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582B as a second order look ahead block. An inverted ripple carry input  $(C_n)$  and a ripple carry output  $(C_{n+4})$  are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the  $\overline{A}$  and  $\overline{B}$  inputs is provided using the A = B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the  $C_{\Pi+4}$  output can be used to indicate relative magnitude as shown in this table:

Data Level	Cn	Cn + 4	Magnitude
	Н	н	A S B
Active	L	н	A < B
High	н	L	A > B
	L	L	A≥B
1	L	L	A ≤ B
Active	н	L	A < B
Low	L	н	A > B
	н	н	A ≥ B

- Functional and Pinout Equivalent to 74181.
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> . I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

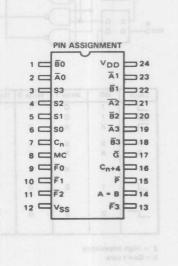
\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C Ceramic "L" Package: -12mW/°C from 100°C to 125°C

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

4-BIT ARITHMETIC LOGIC UNIT





	The court	243.0	VDD	Tic	w *	25°C			Thigh*		1
Characterist	ic	Symbol	Vdc	Min	Max	Min	Тур #	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	10 H =	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	02	.00	10	-	0.05	-	0	0.05		0.05	
00	00		15	1	0.05	-	0	0.05		0.05	
	"1" Level	VOH	5.0	4.95		4.95	5.0	-	4.95		Vdc
$V_{in} = 0$ or $V_{DD}$	Level	*OH	10	9.95	HIJ9F	9.95	10		9.95	AND UND	Action of the same
III O S. FDD			15	14.95	19491	14.95	15		14.95	Miles Co. Feb.	100
U.S.	"O" Level	V	13	14.55		14.55	13	1071710	14.55	Deal De 16	111
Input Voltage		VIL	5.0			_	2.25	1.5	100.00	1.5	Vdc
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$			5.0	T	1.5		2.25	3.0	21 (2.57)	3.0	
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$			15	T.	4.0	_	4.50	4.0	pc_11700 a	4.0	must.
$(V_0 = 13.5 \text{ or } 1.5 \text{ Vdc})$		14	15	1	4.0	-	6.75	-	a C Da	4.0	-
(M OF 4 F M 1)	"1" Level	VIH	19				40 281 A	gD IRela	88.0) =		1
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$			5.0	3.5	-	3.5	2.75	1011301	3.5	M97, HJA	Vdc
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$			10	7.0	4.365	7.0	5.50	_	7.0	# A 07 (0)	Sur
$(V_0 = 1.5 \text{ or } 13.5 \text{ Vdc})$			15	11.0	tent	11.0	8.25	- di Mai	11.0	war in	-
Output Drive Current (AL		ІОН					en 191 e	10 Pleas	80.0 -		mAdd
$(V_{OH} = 2.5 \text{ Vdc})$	Source	-	5.0	-1.2	-	-1.0	-1.7	G7 [9s)	-0.7	MIGHT STATE	
$(V_{OH} = 4.6 \text{ Vdc})$			5.0	-0.64		-0.51	-0.88	-	-0.36	of Floring	100
$(V_{OH} = 9.5 \text{ Vdc})$			10	-1.6	SUCT.	-1.3	-2.25	10 ( Hol)	-0.9		
(V <sub>OH</sub> = 13.5 Vdc)			15	-4.2	-	-3.4	-8.8	-	-2.4	17.7	
(VOI = 0.4 Vdc)	Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdo
$(V_{OL} = 0.5 \text{ Vdc})$			10	1.6	-	1.3	2.25	75	0.9	10 to 10 to	
(VOL = 1.5 Vdc)			15	4.2	1392	3.4	8.8	-	2.4	10 st 01 nt	NESS.
Output Drive Current (CL	(CP Device)	ІОН	20.0			-	1000		1 × × ×	1	mAdo
(V <sub>OH</sub> = 2.5 Vdc)	Source	'OH	5.0	-1.0	_ 1	-0.8	-1.7	In Latin	-0.6	Hali Will	1
$(V_{OH} = 4.6 \text{ Vdc})$	Source	-	5.0	-0.52		-0.44	-0.88	Tel Jadi	-0.36	HSF_KLI	-
$(V_{OH} = 9.5 \text{ Vdc})$			10	-1.3	1791	-1.1	-2.25		-0.9	in sq Sc	113
$(V_{OH} = 13.5 \text{ Vdc})$		3	15	-3.6	14431	-3.0	-8.8	10 1 Set	-2.4	NET BUS	
	Skf	-	_	-		-	-	-	-	197 (Ad	-
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	OL	5.0	0.52	-	0.44	0.88	307 90	0.36	何学「北」	mAdd
$(V_{OL} = 0.5 \text{ Vdc})$			10	1.3	1191	1.1	2.25	-	0.9	Dot no	100
(V <sub>OL</sub> = 1.5 Vdc)	800		15	3.6	Leave -	3.0	8.8	207(Bak	2.4	und Turn	1
Input Current (AL Device	120 (	lin	15	-	± 0.1	-	±0.00001	± 0.1	38.55 P	± 1.0	μAdc
Input Current (CL/CP Dev	vice)	lin	15	-	± 0.3	-	±0.00001	±0.3	14.5 1	±1.0	μAdo
Input Capacitance (Vin = 0)		Cin	-	-	-	olga iši gla	5.0	7.5	side let su	mandy and	pF
Quiescent Current (AL De	vice)	IDD	5.0	-	5.0	in the Change	0.005	5.0	H =0 11	150	μAdo
(Per Package)		100	10	_	10	4008	0.003	10	t to achies	300	Ande
(rerrockage)			15	2	20		0.015	20	_	600	1
2 10 10				-		+	-		-		-
Quiescent Current (CL/CF	Device)	1DD	5.0	1939 SU	20	108	0.005	20	-	150	μAdd
(Per Package)		· · · · · · · · · · · · · · · · · · ·	10	-	40		0.010	40	-	300	
7.31			- 15	747 33	80	EHIT	0.015	80	_	600	-
Total Supply Current ** †		IT	F.0	257 6		IT = (	1.8 µA/kHz	) f + IDE	1837		μAdd
(Dynamic plus Quiesce	ent,		10				3.7 µA/kHz				
Per Package)		1 10	15	a've Swing		IT = (	5.5 μA/kHz	) f + IDC			
(C <sub>L</sub> = 50 pF on all out	puts, all	-		100							1 100
buffers switching)	Ada		100	A NY SHILLIE	ALTERNATION OF		1 0%	40	Termina.		
*T <sub>low</sub> = -55°C for AL Dev T <sub>high</sub> = +125°C for AL D							n are for the t				°C.
#Data labelled "Typ" is n	ot to be used fo	r design pur	poses but	is PAD			$T(C_L) = I_T(5)$				
onded as an indicatio	n of the IC's poi		mance.			I <sub>T</sub> is in μA	(per package	), C <sub>L</sub> in pf	=, V = (V <sub>DC</sub>		volts,
19	aua Ada						(per package equency, and			o-V <sub>SS</sub> ) in	volt

<sup>\*</sup>Tlow = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time	tTLH.	The same	ADMINISTRA			ns
t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTHL	5.0	107	100	200	gisla'V Jugiu
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns	1 000	10	_	50	100	DV = MIY
tTLH, tTHL = (0.55 ns/pF) CL + 9.5 ns	30.0	15	-	40	80	
Propagation Delay Time	tPLH,	1 08	HOV	199/9/2	FIE 12/1/1	ns
Sum in to Sum Out	TPHL	8 01				おりまれば
tpLH, tpHL = (1.7 ns/pF) CL + 620 ns	1 2 2	5.0	-	705	1410	
tpLH, tpHL = (0.66 ns/pF) CL + 217 ns		10	HV.	250	500	egartoV ruo
tpLH, tpHL = (0.5 ns/pF) CL + 155 ns	I st. I	15	-	180	360	NO HALL
Sum in to Sum Out (Logic Mode)	tPLH,	11 48			Jak July W	ns
tpLH tpHL = (1.7 ns/pF) CL + 520 ns	tPHL	5.0	-	605	1210	BET - GVA
tpLH tpHL = (0.66 ns/pF) CL + 182 ns		10		215	430	
tpLH, tpHL = (0.5 ns/pF) CL + 155 ns	1 - 1 3	15	-	180	360	S.O = O.VI
Sum in to A = B	tPLH.				10000 0000	ns
tpLH, tpHL = (1.7 ns/pF) CL + 870 ns	tPHL	5.0	-	955	1910	1 - 0 - 0
tpLH, tpHL = (0.66 ns/pF) CL + 297 ns		10	1401	330	660	Park Driver
tpLH, tpHL = (0.5 ns/pF) CL + 220 ns		15		245	490	INCH- ST
Sum In to P or G	tPLH,				10174	ns
tpLH, tpHL = (1.7 ns/pF) CL + 400 ns	tPHL	5.0	- 1	485	970	HOY
tpLH, tpHL = (0.66 ns/pF) CL + 147 ns		10		180	360	HOY
tpLH, tpHL = (0.5 ns/pF) CL + 105 ns		15	4)	130	260	D = 30VI
Sum In to Cn+4	tPLH	100			1004	ns
tpLH, tpHL = (1.7 ns/pF) CL + 530 ns		5.0	-	615	1230	10 AT
tpLH, tpHL = (0.66 ns/pF) CL + 187 ns		10	1-01	220	440	best Grant
tpLH, tpHL = (0.5 ns/pF) CL + 135 ns		15	-	160	360	- HOM
Carry In to Sum Out	tPLH,			Market Ball	1000	ns
tpLH, tpHL = (1.7 ns/pF) CL + 295 ns	tPHL	5.0		380	760	- HOV
tpLH, tpHL = (0.66 ns/pF) CL + 112 ns		10	-	145	290	HOV
tPLH, tPHL = (0.5 ns/pF) CL + 80 ns		15	(4)	105	210	D= NOV
Carry in to Cn+4	tPLH,	2 97				ns
tpLH, tpHL = (1.7 ns/pF) CL + 220 ns	tPHL	5.0	-	305	610	10 //
tpLH, tpHL = (0.66 ns/pF) CL + 87 ns	1.02	10	-	120	240	THE CHANGE
tpLH, tpHL = (0.5 ns/pF) CL + 60 ns	E DE T	15	T mi	85	170	PURTNER RUP

\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## AC TEST SETUP REFERENCE TABLE

	AC P	ATHS	DC DATA	INPUTS		FIG. 3
TEST	INPUTS	OUTPUTS	TO V <sub>SS</sub>	TO V <sub>DD</sub>	MODE	WAVEFORM
Sum <sub>in</sub> to Sum <sub>out</sub> Delay Time	ĀO	Any F	Remaining A's	All B's	Add	#1
Sum <sub>in</sub> to P Delay Time	Ā0	P	Remaining A's	All B's	Add	#1
Sum <sub>in</sub> to G Delay Time	Вo	G	All Ā's Cn	Remaining B's	Add	#1
Sumin to Cn+4 Delay Time	BO	C <sub>n+y</sub>	All A's Cn	Remaining B's	Add	#2
C <sub>n</sub> to Sum <sub>out</sub> Delay Time	c <sub>n</sub>	Any F	All Ā's	All B's	Add	#1
C <sub>n</sub> to C <sub>n+4</sub> Delay Time	c <sub>n</sub>	C <sub>n+4</sub>	All Ā's	All B's	Add	#1
Sum <sub>in</sub> to A = B Delay Time	ĀO	A = B	All B's Remaining A's	c <sub>n</sub>	Sub	#2
Sum <sub>in</sub> to Sum <sub>out</sub> Delay Time (Logic Mode)	Bo	Any F	All A's	М	Exclusive OR	#2

# MC14581B

FIGURE 1 - TYPICAL SOURCE CURRENT TEST CIRCUIT

FIGURE 2 - TYPICAL SINK CURRENT TEST CIRCUIT

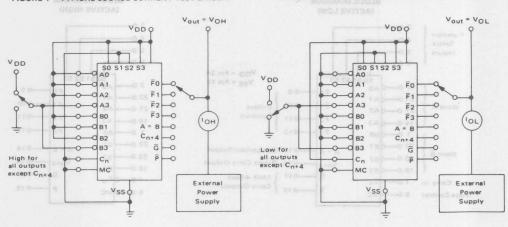


FIGURE 3 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

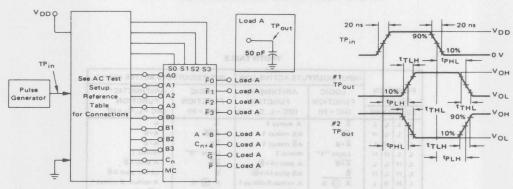
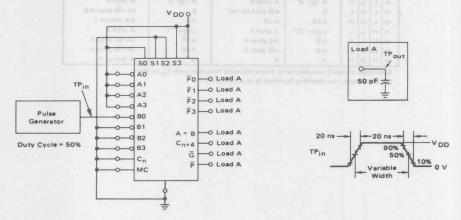
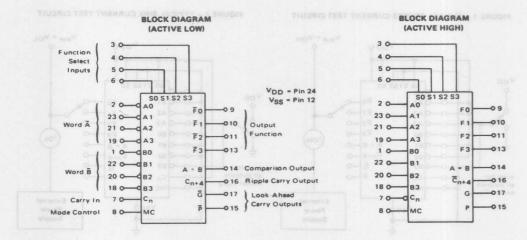


FIGURE 4 - DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



# MC14581B



TRUTH TABLE

				INPUTS/OUTP	UTS ACTIVE LOW	INPUTS/OUTPUTS ACTIVE HIGH			
SELECT S3 S2 S1 S0			Г	LOGIC FUNCTION (MC = H)	ARITHMETIC*	LOGIC	ARITHMETIC* FUNCTION		
53	52	51	50	(MC = H)	$(MC = L, C_n = L)$	(MC = H)	$(MC = L, \overline{C}_n = H)$		
L	L	L	L	Ā	A minus 1	Ā	A		
L	L	L	н	AB	AB minus 1	A+B	A+B		
L	L	н	L	Ā+B	AB minus 1	ĀB	A+B		
L	L	H	н	Logic "1"	minus 1	Logic "O"	minus 1		
L	Н	L	L	A+B	A plus (A+B)	AB	A plus AB		
L	н	L	н	B	AB plus (A+B)	В	(A+B) plus AB		
L	н	н	L	A ⊕ B	A minus B minus 1	A ⊕ B	A minus B minus		
L	н	н	Н	A+B	A+B	AB	AB minus 1		
н	L	L	L	ĀB	A plus (A+B)	Ā+B	A plus AB		
н	L	L	н	A ⊕ B	A plus B	A ⊕ B	A plus B		
н	L	н	L	В	AB plus (A+B)	В	(A+B) plus AB		
н	L	н	н	A+8	A+B	AB	AB minus 1		
н	н	L	L	Logic "O"	A plus A	Logic "1"	A plus A		
н	н	L	н	AB	AB plus A	A+B	(A+B) plus A		
н	н	н	L	AB	AB plus A	A+B	(A+B) plus A		
н	н	н	н	A	A	A	A minus 1		

<sup>\*</sup> Expressed as two's complements. For arithmetic function with  $\mathbf{C}_n$  in the opposite state, the resulting function is as shown plus 1.



# MC14582B

### LOOK-AHEAD CARRY BLOCK

The MC14582B is a CMOS look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The device is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table shown below.

- Expandable to any Number of Bits
- All Buffered Outputs
- Low Power Dissipation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter Bankan	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin, lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

LOGIC EQUATIONS

 $\begin{array}{c} C_{n+x} = \overline{G} + (P0 \circ C_n) \\ C_{n+y} = \overline{G} + (P1 \circ \overline{G}0) + (P1 \circ P0 \circ C_n) \\ C_{n+y} = \overline{G} + (P2 \circ \overline{G}1) + (P2 \circ P1 \circ \overline{G}0) + (P2 \circ P1 \circ P0 \circ C_n) \\ \overline{G} = \overline{G} + (P3 \circ \overline{G}2) + (P3 \circ \overline{G}2) + (P3 \circ \overline{G}1) + (P1 \circ P2 \circ P3 \circ \overline{G}0) \\ \end{array}$ 

P = P3 • P2 • P1 • P0

### PIN DESIGNATIONS

DESIGNATION	PIN NO's	FUNCTION
G0,G1,G2,G3	3,1,14,5	Active-Low Carry-Generate Inputs
P0,P1,P2,P3	4,2,15,6	Active-Low Carry-Propagate Inputs
Cn	13	Carry Input
C <sub>n+x</sub> , C <sub>n+y</sub> C <sub>n+z</sub>	12,11,9	Carry Outputs
G	10	Active-Low Group Carry-Generate Output
P	7	Active-Low Group Carry-Propagate Output

## **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

LOOK-AHEAD CARRY BLOCK





CERAMIC PACKAGE CASE 620

PLASTIC PACKAGE CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS

		VDD	Tio	w*	25°C			Thigh*		M
Characteristic	Symbol	Vdc	lc Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	100-11	0.05	Vdc
V <sub>in</sub> = V <sub>DD</sub> or 0	0.2	10	-	0.05	-	0	0.05	-	0.05	
III OB		15	-	0.05	-	0	0.05	_	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0		4.95	_	Vdd
Vin = 0 or VDD	*OH	10	9.95	740	9.95	10	AREA .	9.95		1
VIN - O OI VDD		15	14.95		14.95	15		14.95	_	
Input Voltage "0" Level	VIL		14.55	1. Str. Str. Str.	14.55	10	of Statut	14.55	SALUM D	Vdc
	VIL	5.0	Laborator Tol	1.5	C. market	2.25	1.5	10 12180	1.5	Vac
(V <sub>O</sub> = 4.5 or 0.5 Vdc)	J - 113	10		3.0	LI CONT	4.50	3.0	daberrar	3.0	The
(V <sub>O</sub> = 9.0 or 1.0 Vdc)		15	No. 1 St. of Line				4.0	100-00	4.0	wendy
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	00 518 B	4.0	V1065-30	6.75	4.0	0187 119	4.0	6300
NOO 18 YE HAD GA "1" Level	VIH		WO		to stable of	purangiast)		to burn to		Bellev
(V <sub>O</sub> = 0.5 or 4.5 Vdc)		5.0	3.5	0 7 3	3.5	2.75	-	3.5	-	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	-	7.0	5.50	- you denut	7.0	idsīmaq	3 #
(V <sub>O</sub> ≈ 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	-	11.0	Sept. The St.	16. 0
Output Drive Current (AL Device)	ІОН							Discions		mAd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	moT It o	-1.7	rede Press	a de
(V <sub>OH</sub> = 4.6 Vdc)	Steel St	5.0	-0.64	-	-0.51	-0.88		-0.36		2. 6
(V <sub>OH</sub> = 9.5 Vdc)	施胜 - 1	10	-1.6	-	-1.3	-2.25	Alexander at	-0.9	in A Timbe	
(V <sub>OH</sub> = 13.5 Vdc)	罪!	15	-4.2	900210	-3.4	-8.8	NO.T.OM	-2.4	to eldisq	10.0
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	graze e	0.51	0.88	BUIL IEW	0.36	+ Yarren	mAd
(VOL = 0.5 Vdc)	OL	10	1.6	_	1.3	2.25	_	0.9		
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	_	3.4	8.8	_	2.4	_	
Output Drive Current (CL/CP Device)	ГОН									mAd
(V <sub>OH</sub> = 2.5 Vdc) Source	TOH	5.0	-2.5		-2.1	-4.2	es maga	-1.7	STTAR I	111111
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	2 _	-0.44	-0.88	SEP-SECTION OF	-0.36		30
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	4.30	-1.1	-2.25	_	-0.9	/ stamus	1
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6		-3.0	-8.8	-	-2.4	And direct	30 0
0		5.0	0.52	J. 12 S. 15	0.44	0.88	75751	0.36		- 0-1
(V <sub>OL</sub> = 0.4 Vdc) Sink	IOL		1000000		The second second	Mark Control of the Control	10 (00) 1	A CONTRACTOR OF THE PARTY OF TH	DO TO INC	mAd
(VOL = 0.5 Vdc)		10	1.3	-	1.1	2.25		0.9	wor Place	
(V <sub>OL</sub> = 1.5 Vdc)		15	3.6	-	3.0	8.8	Pac-ugo	2.4		
Input Current (AL Device)	lin	15	1981 4	± 0.1	-	±0.00001	± 0.1	90ms189	± 1.0	μAd
Input Current (CL/CP Device)	lin	15	- 6	± 0.3	-	±0.00001	± 0.3	en anders	±1.0	μAd
Input Capacitance	Cin	-	rucho year	enivery	elt of age	5.0	7.5	play aupr	ens agai	pF
(V <sub>in</sub> = 0) Quiescent Current (AL Device)	IDD	5.0	(H20)	5.0	ottool 201	0.005	5.0	Collegijo (19)	150	μAd
(Per Package)	טטי	10	- Action	10	-	0.000	10	- Indian	300	1
1. 6. 7 66.10367		15		20	_	0.015	20	- 1	600	-
0 0 101 100 0 1	1		-	-	-	-		-		1
Quiescent Current (CL/CP Device)	l DD	5.0	-	20	-	0.005	20	-	150	μAd
(Per Package)		10	-	40	-	0.010	40	-	300	
		15	-	80		0.015	80		600	-
Total Supply Current**†	IT	5.0	1-7-11			1.4 µA/kHz				μAd
(Dynamic plus Quiescent,	- 1	10				2.8 μA/kHz				
Per Package)	17	15	1			4.3 μA/kHz		)		1
(C <sub>L</sub> = 50 pF on all outputs, all			150.0							
buffers switching)			1 1							1

 $^*T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.
†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: I  $_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.005.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time tTLH, tTHL = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTLH-	5.0	-	100	200	ns
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns		10 15	-	50 40	100 80	
Propagation Delay Time  tp_H, tpHL = (1.7 ns/pF) CL + 260 ns  tp_H, tpHL = (0.66 ns/pF) CL + 107 ns  tp_H, tpHL = (0.5 ns/pF) CL + 85 ns	tPLH, tPHL	5.0 10 15	101-0-0 001-0 161-0	345 140 110	690 280 220	ns

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

#### FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

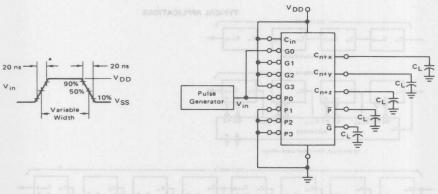
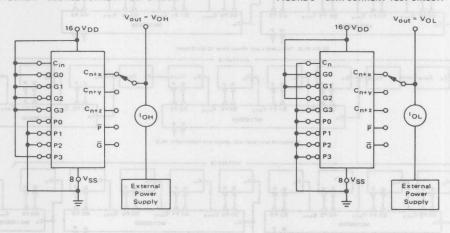


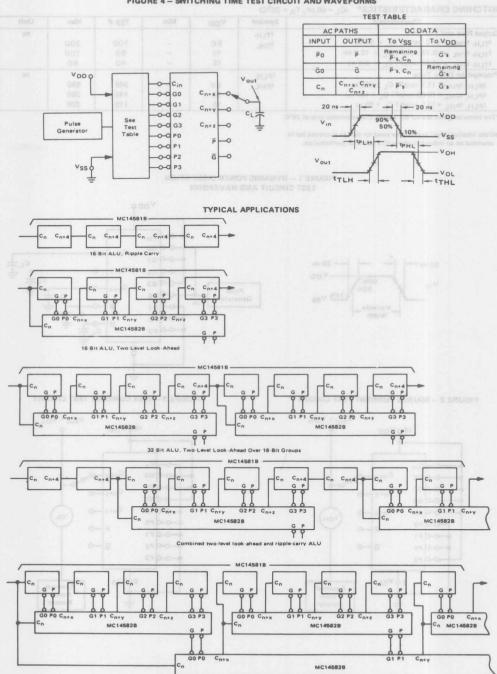
FIGURE 2 - SOURCE CURRENT TEST CIRCUIT

FIGURE 3 - SINK CURRENT TEST CIRCUIT



.

FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



64-Bit ALU, Full-Carry Look-Ahead in Three Levels.

A and B inputs and F outputs are not shown (MC145818).



# MC14583B

### **DUAL SCHMITT TRIGGER**

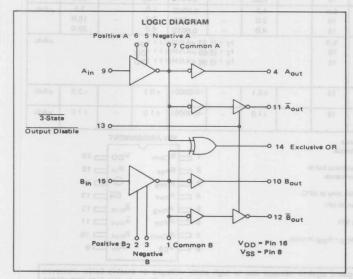
The MC14583B is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Resistor Adjustable Trigger Levels

### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
Vin, Vout	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

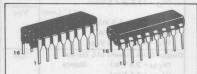
\*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C
Ceramic "L" Package: -12mW/°C from 100°C to 125°C



## **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

DUAL SCHMITT TRIGGER



L SUFFIX

P SUFFIX
PLASTIC PACKAGE

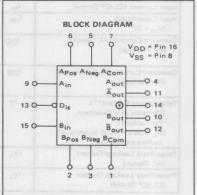
CASE 620

CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



## TRUTH TABLE

- 1	NPUT	S	3005-95	OUTPUTS							
Α	В	Dis	Aout	Aout	Bout.	Bout	•				
0	0	0	0	Z	0	Z	0				
0	0	1	0	1	0	1	0				
0	1	0	0	Z	1	Z	1				
0	1	1	0	1	1	0	1				
1	0	0	1	Z	0	Z	1				
1	0	1	1	0	0	. 1	1				
1	1 .	0	1	Z	1	Z	0				
1	1	1	1	0	1	0	0				

Z = High impedance at output

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

	100	V <sub>DD</sub> Vdc	T <sub>low</sub> *		25°C			Thigh*		-
Characteristic	Symbol		Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V <sub>in</sub> =V <sub>DD</sub> or 0	0.	10	-	0.05	-	0	0.05	-	0.05	
AIU - ADD OLO		15	_	0.05	(Simolar	0	0.05		0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	_	Vdc
Vin=0 or VDD	*OH	. 10	9.95		9.95	10		9.95		Vac
MANUAL MAINS MANUAL MANUAL	(0.35	15	14.95	betterd	14.95	15	S law i	14.95	BAT STVI o	1
4 10 //		15	14.95	La Hole	14.95	15	Hay M. Dinis	14.95	A yman	1
Input Voltage A and B "0" Level	VIL	10. 7	rebasce	mit willeri	istomust.	a reggins	Selemen	100.32 .00	and adult of	Vdc
(V <sub>O</sub> = 4.5 or 0.5 Vdc)		5.0	a trulpe	1.5	riseni n	2.25	1.5	попти	1.5	95 XIII
(V <sub>O</sub> = 9.0 or 1.0 Vdc)	-	10	over year	3.0	eoilāgs	4.50	3.0	tell had	3.0	limits.
(V <sub>O</sub> = 13.5 or 1.5 Vdc)		15	-	4.0	-	6.75	4.0	-	4.0	-
"1" Level	VIH		is Notineen	ob ale fil	ni serenti	illand or				Table 1
(V <sub>O</sub> = 0.5 or 4.5 Vdc)	Marian II	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
(V <sub>O</sub> = 1.0 or 9.0 Vdc)		10	7.0	STANT ING	7.0	5.50	DI THE	7.0	NO. OF TAXABLE	S. Tex
(V <sub>O</sub> = 1.5 or 13.5 Vdc)	温泉 一計	15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (AL Device)	ІОН					arts.	Sent NA	he notes	and Penn	mAdd
(VOH = 2.5 Vdc) Source	0	5.0	-1.2	-	-1.0	-1.7	-	-0.7	-	
(VOH = 4.6 Vdc)	1	5.0	-0.25	_	-0.2	-0.36	0.72 - 49	-0.14	av ylgg	5 4
(VOH = 9.5 Vdc)		10	-0.62	_	-0.5	-0.9	-male	-0.35	-	2 4
(V <sub>OH</sub> = 13.5 Vdc)	ARED	15	-1.8		-1.5	-3.5	-	-1.1	Adres mile	100
(V <sub>OL</sub> = 0.4 Vdc) Sink	1	5.0	0.64	20140 10	0.51	0.88	PACE OWN	0.36	ro stoso	mAdo
	IOL	10	1.6	Range	1.3	2.25	and my	0.9	ET yange	IIIAGO
(V <sub>OL</sub> = 0.5 Vdc)					3.4	8.8		2.4		
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2	-	3.4	8.8	10000	2.4	A 1535181	15. 18
Output Drive Current (CL/CP Device)	ЮН									mAdd
(V <sub>OH</sub> = 2.5 Vdc) Source		5.0	-1.0	-	-0.8	-1.7	-	-0.6	-	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.2	-	-0.16	-0.36	eff eagat	-0.12	MARIE I	M LANGES
(V <sub>OH</sub> = 9.5 Vdc)	6	10	-0.5	W -	-0.4	-0.9	vertices:	-0.3	-	tos
(V <sub>OH</sub> = 13.5 Vdc)		15	-1.4	-	-1.2	-3.5		-1.0	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	Eldane r	mAdd
(VOL = 0.5 Vdc)		10	1.3	(U = 0-	1.1	2.25	p 201 s	0.9	DO to tuo	P LUNY
.(VOL = 1.5 Vdc)		15	3.6	-	3.0	8.8	10 Tell 10	2.4	100 En 100	
Input Current (AL Device)	lin	15		±0.1	-	±0.00001	±0.1	-	± 1.0	μAdo
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdo
Input Capacitance		_	10000		_	5.0	7.5		-	pF
The state of the s	Cin	32	100			3.0	7.5	S Inches	ad Tensel	Pi
(V <sub>in</sub> = 0)										-
Quiescent Current (AL Device)	IDD	5.0	KONG YOU	0.25	01408	0.0005	0.25	100-000	7.5	μAdo
(Per Package)		10	ANTONIA A	0.50	-	0.0010	0.50	9-119	15.0	HUTTEN S
		15	100	1.00	- "	0.0015	1.00	-	30.0	
Quiescent Current (CL/CP Device)	IDD	5.0	-	1.0		0.0005	1.0	-	7.5	μAdo
(Per Package)	18	10	-	2.0		0.0010	2.0	-	15.0	
Ir Oiā		15	-	4.0	-	0.0015	4.0	-	30.0	
Total Supply Current**†	IT.	5.0			I+ = (1	.33 µA/kHz	) f + loo			μAdd
(Dynamic plus Quiescent,		10				2.65 µA/kHz				
Per Package)		15				.98 µA/kHz				
(C <sub>L</sub> = 50 pF on all outputs, all	101		-		1 (0					
buffers switching)			NAME OF TAXABLE PARTY.							
Three-State Leakage Current	le.	15	-	± 0.1		+0.00001	± 0.1	T	1 .20	T A -1-
(AL Device)	ITL	15	-	± 0.1		0.00001	± 0.1		±3.0	μAdo
		-	1	-			-			-
Three-State Leakage Current	ITL	15	-	±1.0	-	+0.00001	± 1.0	-	± 7.5	μAdo
(CL/CP Device)						Maria Salara			1	

PIN ASSIGNMENT \*Tlow = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device. BCom VDD 16 #Data labelled "Typ" is not to be used for design purposes but is 2 BPos Bin \_\_\_\_ 15 intended as an indication of the IC's potential performance. 0 3 = BNeg \_\_\_\_14 \*\*The formulas given are for the typical characteristics only at 25°C. Dis Aout \_\_\_\_ 13 †To calculate total supply current at loads other than 50 pF: 5 \_ ANeg Bout \_\_\_\_ 12 Apos  $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 6 0 Aout 11 where: I\_T is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.005. 7 Acom Bout 10 8 VSS

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

## MC14583B

SWITCHING CHARACTERISTICS\* (C. = 50 pf. T. = 250C)

Characteristic	Symbol	VDD	Min	Тур#	Max	Unit
Output Rise Time	tTLH					ns
tTLH = (3.0 ns/pF) CL + 30 ns		5.0		180	360	
tTI H = (1.5 ns/pF) CI + 15 ns	19	10	_	90	180	ag <sub>A</sub>
tTLH = (1.1 ns/pF) CL + 10 ns		15	_	65	130	7
Output Fall Time	tTHL		100000000000000000000000000000000000000	9		ns
tTHL = (1.5 ns/pF) CL + 25 ns		5.0	- 0.63	100	200	
t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns	1000	10		50	100	-
t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	100	15	0-4 500	40	80	eav
Propagation Delay Time	tpLH,	20			LAME OF	ns
Ain, Bin to Aout, Bout	tPHL				1 7	
tp_H, tpHL = (1.7 ns/pF) CL + 565 ns	THE	5.0	-0-0	650	1300	
tpLH, tpHL = (0.66 ns/pF) CL + 197 ns	ment l	10	0-0-0	230	460	
tp_H, tpHL = (0.5 ns/pF) CL + 125 ns	6	15		150	300	
Ain, Biri to Aout, Bout	tPLH,				GW6 0-	ns
tpLH, tpHL = (1.7 ns/pF) CL + 1015 ns	tPHL	5.0	-	1100	2200	
tpLH, tpHL = (0.66 ns/pF) CL + 347 ns		10	_ 300	380	760	1 11
tpLH, tpHL = (0.5 ns/pF) CL + 235 ns	41	15	_	260	520	
Ain, Bin to Exclusive OR	tPLH,					ns
tpl H, tpHL = (1.7 ns/pF) CL + 665 ns	tPHL	5.0		750	1500	
tpLH, tpHL = (0.66 ns/pF) CL + 257 ns	1112	10	_	280	560	
tpLH, tpHL = (0.5 ns/pF) CL + 145 ns	D TEST HOP	15	HIE 2 - POWE	170	340	
3-State Enable, Disable Delay Time (see figure 5)	t <sub>on</sub> ,					ns
ton, toff = (1.7 ns/pF) CL + 140 ns	toff	5.0		225	450	
t <sub>on</sub> , t <sub>off</sub> = (0.66 ns/pF) C <sub>L</sub> + 57 ns	-011	10		90	180	
t <sub>on</sub> , t <sub>off</sub> = (0.5 ns/pF) C <sub>L</sub> + 30 ns		15	- )	55	110	
Positive Threshold Voltage	V <sub>T+</sub>	5.0	- N	3.30	1 1 1 1 1 1 1 1 1	Vdc
(R1, R2 = 5.0 kΩ)	1.7	10	-	5.70	4 -	
	Dela La La	15	· -	8.20	-	
Negative Threshold Voltage	V <sub>T</sub> _	5.0		1.70	1 1-	Vdc
(R1, R2 = 5.0 kΩ)		10		4.30	4-4-1	and the
the sunt		15	_	6.80	-	
Hysteresis Voltage	VH	5.0	0.85	1.70	3.40	Vdc
$(R1, R2 = 5.0 k\Omega)$		10	0.70	1.40	2.80	
		15	0.70	1.40	2.80	-
Threshold Voltage Variation, A to B	ΔVT	5.0		0.1	- 0	Vdc
$(R1, R2 = 5.0 k\Omega)$		10	-	0.15	- 1 101	14100
	the could a	15	100	0.20	_	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

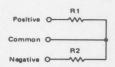
<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### MC14583B

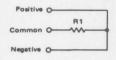
FIGURE 1 - TYPICAL OUTPUT SOURCE AND SINK CHARACTERISTICS TEST CIRCUIT Vout VDD OUTPUT SINK OUTPUT SOURCE CHARACTERISTICS TEST | VGS = - VDD VALUE | VDS = Vout - VDD TEST VGS VDD VDD 0 SWITCH POSITION SWITCH POSITION OUTPUT - 0 UNDER TEST SW2 SW1 SW2 3 SW1 -O SW1 Aout, Bout 2 2 Ā<sub>out</sub>, B̄<sub>out</sub> -d Dis 0 2 Exclusive OR 2 Bout 0 0 9 0 Bin (10 Bout SW2 0 1 000 yss = External Power Supply FIGURE 2 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS PVDD ID 500 µF 7 0.01 µF Ceramic Pulse Generator 1 Ain Aout fout, Ain Aout fout, Bin -d Dis 0 Bout Pulse Bin Bout VSS

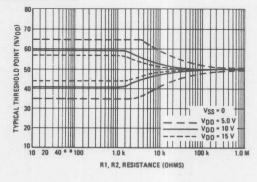
### FIGURE 3 - TYPICAL THRESHOLD POINTS

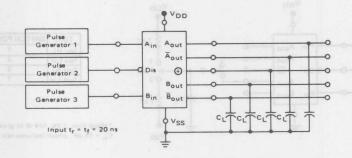


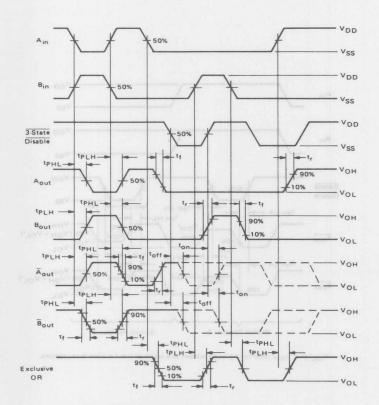


B - Feedback scheme for hysteresis adjustment:



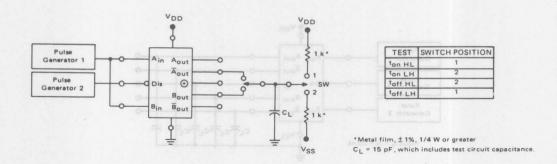


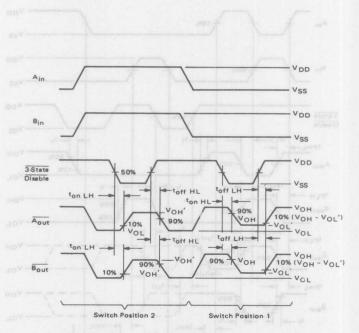




Note: Dashed lines indicate high output resistance.

### FIGURE 5 - 3-STATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





VOL' and VOH' refer to the levels present as a result of the 1 k ohm load resistors.

### MC14584B

### HEX SCHMITT TRIGGER

The MC14584B Hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069UB hex inverter for enhanced noise immunity to "square up" slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace MC14069UB
- For Greater Hysterisis, Use MC14106B which is Pin-for-Pin Replacement for CD40106B and MM74C14

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter all 90.0	00, Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-05 to +180	V
V <sub>in</sub> . V <sub>out</sub>	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
Im. lout	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Packaget	500	mW
1 <sub>stg</sub>	Storage Temperature	-65 to +150	"C
T <sub>1</sub>	Lead Temperature (8-Second Soldering)	260	·C

\*Maximum Ratings are those values beyond which damage to the device may occur †Temperature Derating: Plastic "P" Package: -12mW/"C from 65°C to 85°C Ceramic "L" Package: -12mW/"C from 100°C to 125°C

### EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



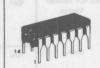
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $v_{SS}$  or  $v_{DD}$ ). Unused outputs must be left open.

### **CMOS SSI**

(LOW-POWER COMPLEMENTARY MOS)

HEX SCHMITT TRIGGER





L SUFFIX
CERAMIC PACKAGE
CASE 632

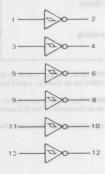
P SUFFIX PLASTIC PACKAGE CASE 646

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### LOGIC DIAGRAM



V<sub>DD</sub> = Pin 14 V<sub>SS</sub> = Pin 7

		VDD	Tic	ow °		25°C		Thi	gh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур #	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	_	0	0.05	-	0.05	Vdc
$V_{in} = V_{DD}$		10	-	0.05	-	0	0.05	-	0.05	-
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
$V_{in} = 0$		10	9.95	-	9.95	10	HOW X	9.95	-	
	131	15	14.95	-	14.95	15	-	14.95	-	
Output Drive Current (AL Device)	ГОН	Post of	POM HI	y behaut	laneo el	TREET !	Schmi	art BAB	MC140	mAdo
(VOH = 2.5 Vdc) Source		5.0	-3.0	of geolys	-2.4	-4.2	rin <del>o</del> len	-1.7	ns teans	No.5
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.64	w ceu y	-0.51	-0.88	b Stad	-0.36	da <del>o</del> vidio	nem.
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.6	lesit el	-1.3	-2.25	pid tolk	-0.9	dissib n	mon-
(V <sub>OH</sub> = 13.5 Vdc)		15	-4.2	and Three	-3.4	-8.8	In Til Iss	-2.4	00 JZT-02 h	1000
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	vistola	0.51	0.88	the state of the s	0.36	peomedo	mAdo
(V <sub>OL</sub> = 0.5 Vdc)		10	1.6	-	1.3	2.25	-	0.9	.emoż	PURSU
(V <sub>OL</sub> = 1.5 Vdc)		15	4.2		3.4	8.8	-	2.4	-	
Output Drive Current (CL/CP Device)	ІОН				V 81 0	a O Vdc	≈ 90/F	F sosti	V vicau	mAdo
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	
(V <sub>OH</sub> = 4.6 Vdc)		5.0	-0.52	QC 30 5	-0.44	-0.88	Day I	-0.36	a eigada	0.0
(V <sub>OH</sub> = 9.5 Vdc)		10	-1.3	HORE BROWN	-1.1	-2.25	KIT TRAC	-0.9	ya <u>tt</u> korto	
(V <sub>OH</sub> = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	i nāitak	-2.4	in allelium	10
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdo
(VOL = 0.5 Vdc)		10	1.3	-	1.1	2.25	1 12000	0.9	an Be U	1 8
(VOL = 1.5 Vdc)		15	3.6	9 andai	3.0	8.8	di-sier	2.4	or C <del>r</del> oss	8 0
Input Current (AL Device)	lin	15	-	± 0.1	DALM	±0.00001	±0.1	10-110	± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	Cin	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (AL Device)	IDD	5.0	-	0.25	-	0.0005	0.25	-	7.5	μAdc
(Per Package)	00	10	-	0.50	Last V	0.0010	0.50	W-350	15	CHOIN
	A	15	- 610	1.00		0.0015	1.00	4 -	30	ton
Quiescent Current (CL/CP Device)	IDD	5.0	-	1.0	-	0.0005	1.0	-	7.5	μAdo
(Per Package)	100	10	-	2.0	-	0.0010	2.0	-	15	pride
their was Carl to the C	13	15	40 1 66	4.0	-	0.0015	4.0	HITOV JUST	34	1 Dus
Total Supply Current**†	IT	5.0			1-=(	1.8 µA/kHz)	f + Inn	1871U-2 1UG	WE TO THE	μAdo
(Dynamic plus Quiescent,		10				3.6 µA/kHz)				4
Per Package)		15				5.4 µA/kHz)				
(CL = 50 pF on all outputs, all			1167.1				- 00			12
buffers switching)										
Hysteresis Voltage	VH*	5.0	0.27	1.0	0.25	0.6	1.0	0.21	1.0	Vdc
	VH.	10	0.36	1.3	0.30	0.70	1.2	0.25	1.2	paters
	-	15	0.77	1.7	0.60	1.1	1.5	0.50	1.4	
Threshold Voltage		F								
Positive-Going	V <sub>T+</sub>	5.0	1.9	3.5	1.8	2.7	3.4	1.7	3.4	Vdc
		10	3.4	7.0	3.3	5.3	6.9	3.2	6.9	
		15	5.2	10.6	5.2	8.0	10.5	5.2	10.5	
Negative-Going	VT-	5.0	1.6	3.3	1.6	2.1	3.2	1,5	3.2	Vdc
1 2 00		10	3.0	6.7	3.0	4.6	6.7	3.0	6.7	1
		15	4.5	9.7	4.6	6.9	9.8	4.7	9.9	

 $<sup>^*</sup>T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: I  $_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = (V\_DD-V\_SS) in volts, f in kHz is input frequency, and k = 0.001.

PV<sub>H</sub> = V<sub>T+</sub> - V<sub>T-</sub> (But maximum variation of V<sub>H</sub> is specified as less than V<sub>T+</sub> max - V<sub>T-</sub> min).

A substitute of the second of the

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

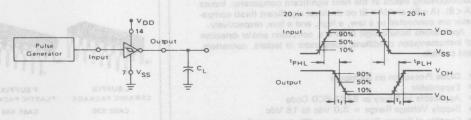
<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25°C.

### SWITCHING CHARACTERISTICS (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ#	Max	Unit
Output Rise Time	tTLH	5.0		100	200	ns
		10	_	50	100	
		15		40	80	
Output Fall Time	tTHL	5.0	8403 3G	100	200	ns
		10	-	50	100	
	cometracted	15	mod dom	40	80	arti
Propagation Delay Time	tPLH, tPHL	5.0	narunit_lessor	125	250	ns
	118 TA 156	10	Al sugar	50	100	DE DA
	bris .(8 <a1< td=""><td>15</td><td>用&gt;型 部</td><td>40</td><td>80</td><td>are turn</td></a1<>	15	用>型 部	40	80	are turn

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### FIGURE 1 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

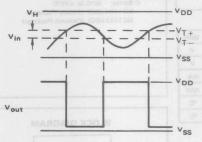


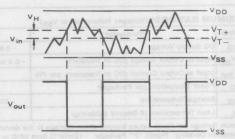
### FIGURE 2 - TYPICAL SCHMITT TRIGGER APPLICATIONS



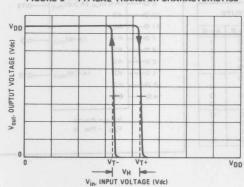
(a) Schmitt Triggers will square up inputs with slow rise and fall times.

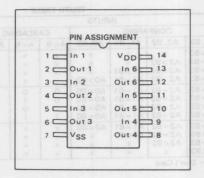
(b) A Schmitt trigger offers maximum noise immunity in gate applications.





### FIGURE 3 - TYPICAL TRANSFER CHARACTERISTICS





### **4-BIT MAGNITUDE COMPARATOR**

The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A<B, A=B, and A>B), and three outputs (A<B, A=B, and A>B). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A>B), (A<B), and (A=B) to the corresponding inputs of the next significant comparator. Inputs (A<B), (A=B), and (A>B) on the least significant (first) comparator are connected to a low, a high, and a low, respectively.

Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

- Diode Protection on All Inputs
- Expandable
- Applicable to Binary or 8421-BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range
- Can be Cascaded See Fig. 3

### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
lin, lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

#### TRUTH TABLE

			Inu	IN IAD	LE					
9,011		11	IPUTS					LITPLIT	0	
	COMP	AFIING	inda a was	CA	SCADIN	IG	OUTPUTS			
A3, B3	A2, B2	A1, B1	A0, B0	A <b< th=""><th>A = B</th><th>A&gt;B</th><th>A<b< th=""><th>A = B</th><th>A&gt;B</th></b<></th></b<>	A = B	A>B	A <b< th=""><th>A = B</th><th>A&gt;B</th></b<>	A = B	A>B	
A3>B3	×	×	×	×	×	×	0	0	1	
A3 = B3	A2>B2	×	×	×	×	×	0	0	1	
A3 = B3	A2 = B2	A1>B1	×	×	×	×	0	0	1	
A3 = B3	A2 = B2	A1 = B1	A0>B0	×	×	×	0	0	1	
A3 = B3	A2 = B2	A1=B1	A0 = B0	0	0	×	0	0	1	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	×	0	1	0	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1 8	0	×	1	0	0	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	1	×	1	1	0	
A3 = B3	A2 = B2	A1 = B1	A0 <b0< td=""><td>×</td><td>×</td><td>×</td><td>1</td><td>0</td><td>0</td></b0<>	×	×	×	1	0	0	
A3 = B3	A2=B2	A1 <b1< td=""><td>×</td><td>×</td><td>×</td><td>×</td><td>1</td><td>0</td><td>0</td></b1<>	×	×	×	×	1	0	0	
A3 = B3	A2 <b2< td=""><td>×</td><td>×</td><td>×</td><td>×</td><td>×</td><td>1</td><td>0</td><td>0</td></b2<>	×	×	×	×	×	1	0	0	
A3 <b3< td=""><td>×</td><td>×</td><td>×</td><td>×</td><td>×</td><td>×</td><td>1</td><td>0</td><td>0</td></b3<>	×	×	×	×	×	×	1	0	0	

× = Don't Care

### **CMOS MSI**

(LOW POWER COMPLEMENTARY MOS)

4-BIT MAGNITUDE COMPARATOR



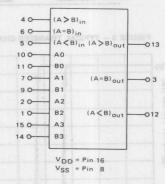
L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

### **BLOCK DIAGRAM**



### MC14585B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

	4.46	espets .	VDD	Tic	w*		25°C		Thi	gh	Tolking Co.
Characteristi	С	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	7.75-sup	0.05	Vdc
$V_{in} = V_{DD}$ or 0	08	02	10	-	0.05	-	0	0.05	0.00-00.0	0.05	12 517
-111 -100 -108			15	-	0.05	-	0	0.05	-	0.05	-
	"1" Level	VOH	5.0	4.95	14/07	4.95	5.0	5.20 L PA .	4.95	N LEWIS	Vdc
$V_{in} = 0 \text{ or } V_{DD}$	Cell	- OH	10	9.95	THAL	9.95	10	1 + 73 1	9.95	- 120GT	1
	991		15	14.95		14.95	15	20 - 20	14.95	200	1000
Input Voltage	"0" Level	VIL						7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7			Vdc
(Vo - 4.5 or 0.5 Vdc)	0 2010.	-15	5.0	-	1.5	Ves in se	2.25	1.5	und tell ion	1.5	1
(VO = 9.0 or 1.0 Vdc)			10		3.0	pi tuo ess	4.50	3.0	or or there as	3.0	shuidis
(V <sub>O</sub> = 13.5 or 1.5 Vdc)			15	_	4.0	inflored in	6.75	4.0		4.0	1
,,,	"1" Level	VIH									Vdc
(Vo = 0.5 or 4.5 Vdc)		111	5.0	3.5		3.5	2.75	_	3.5	_	V GC
(VO = 1.0 or 9.0 Vdc)			10	7.0	_	7.0	5.50	_	7.0	-	
(VO = 1.5 or 13.5 Vdc)			15	11.0	-	11.0	8.25	_	11.0	-	
Output Drive Current (AL	Devicel	ГОН		11.0		11.0	0.20	-	11.0		mAdo
(V <sub>OH</sub> = 2.5 Vdc)	Source	HO	5.0	-3.0	200	-2.4	-4.2	_	-1.7	_	1
(V <sub>OH</sub> = 4.6 Vdc)	Courte		5.0	-0.64		-0.51	-0.88	_	-0.36	_	1
(VOH = 9.5 Vdc)			10	-1.6		-1.3	-2.25		-0.9		
(V <sub>OH</sub> = 13.5 Vdc)		Ser II	15	-4.2		-3.4	-8.8	1804 DIS	-2.4	r struct	
(V <sub>OL</sub> = 0.4 Vdc)	Sink	101	5.0	0.64	-	0.51	0.88	TRUAW	0.36	-	mAde
(V <sub>OL</sub> = 0.5 Vdc)	SIFIK	IOL	10	1.6		1.3	2.25		0.9		111301
(VOL = 1.5 Vdc)			15	4.2		3.4	8.8	-27	2.4		101
	00.0		13	7.2		3.4	0.0		2.7	- In C	- 0.4
Output Drive Current (CL/		ЮН									mAdo
(V <sub>OH</sub> = 2.5 Vdc)	Source	Complete	5.0	-2.5	- 0	-2.1	-4.2		-1.7	- da	100
(V <sub>OH</sub> = 4.6 Vdc)			5.0	-0.52	_	0.44	-0.88 -2.25	- 1/1	-0.36 -0.9		100
(V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	100		15	-4.2	1	-3.0	-8.8		-2.4		1
0		UE (E		-	-		-				mAdd
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.52	0	0.44	0.88	-	0.36	26	mAdd
(Vol = 0.5 Vdc)		201	15	1.3	-	3.0	8.8		2.4		
(V <sub>OL</sub> = 1.5 Vdc)			la l	-	- 1	-		-	-		-
Input Current (AL Device)		lin	15	-	± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdc
Input Current (CL/CP Dev	ice)	lin	15	177	± 0.3	-	±0.00001	± 0.3	1 - 1	± 1.0	μAdd
Input Capacitance (V <sub>in</sub> = 0)	2000	Cin	3 my (8.)	A)	- ,	7	5.0	7.5	-	C-	pF
Quiescent Current (AL Des	vice)	IDD	5.0	-	5.0	V =	0.005	5.0	-	150	μAdo
(Per Package)		4-471	10	-	10	-	0.010	10	-	300	18+14
			15	-	20	-	0.015	20	- 1	600	
Quiescent Current (CL/CP	Device)	Ipp	5.0	-	20	-	0.005	20	_	150	μAdd
(Per Package)			10	-	40	_	0.010	40	-	300	
PHOTO 23, A3, E3, A2, E5,	er boy Apin Si	=Alims 18	15	-	80	-	0.015	80	-	600	BAL
Total Supply Current**†		IT	5.0			17=1	0.6 μA/kHz	) f + 1pp			μAdd
(Dynamic plus Quiescer	nt,		10				1.2 µA/kHz				1
Per Package)		H-1	15				1.8 µA/kHz				
(C <sub>1</sub> = 50 pF on all outp	outs, all					14 18	24,500,000	M. Pare . A.			Inpucts II
buffers switching)		M = (41)									- COL 100

 $^{\circ}T_{low} = -55^{\circ}C$  for AL Device,  $-40^{\circ}C$  for CL/CP Device.  $T_{high} = +125^{\circ}C$  for AL Device,  $+85^{\circ}C$  for CL/CP Device.

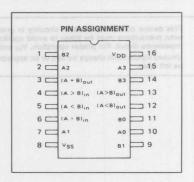
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V=(V_{DD}-V_{SS})$  in volts, f in kHz is input frequency, and k=0.001.



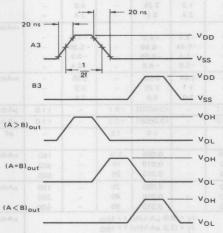
SWITCHING CHARACTERISTICS\* (C1 = 50 pF. TA = 25°C)

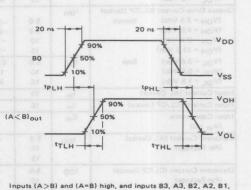
Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns	tTLH-	5.0	Summer!	100	200	ns
t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	THL	10	TO.	50 40	100	
Turn-On, Turn-Off Delay Time	tPLH,	15		40	80	ns
tpLH, tpHL = (1.7 ns/pF) C <sub>L</sub> + 345 ns tpLH, tpHL = (0.66 ns/pF) C <sub>L</sub> + 147 ns		5.0 10	- 201	430 180	860 360	
tpLH, tpHL = (0.5 ns/pF) CL + 105 ns	N. C.	15		130	260	

\*The formulas given are for the typical characteristics only at 25°C. #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

FIGURE 2 - DYNAMIC SIGNAL WAVEFORMS





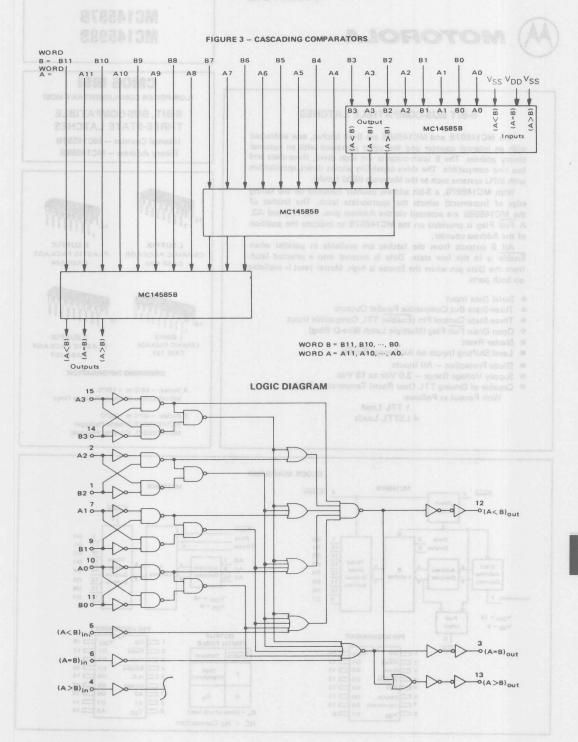
Inputs (A > B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A < B) low

f in respect to a system clock.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this highimpedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must

A1, A0, and (A < B) low.





The MC14597B and MC14598B are 8-bit latches, one addressed with an internal counter and the other addressed with an external binary address. The 8 latch-outputs are high drive, three-state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

With MC14597B, a 3-bit address counter (clocked on the falling edge of Increment) selects the appropriate latch. The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2. A Full Flag is provided on the MC14597B to indicate the position of the Address counter.

All 8 outputs from the latches are available in parallel when Enable is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

- Serial Data Input
- Three-State Bus Compatible Parallel Outputs
- Three-State Control Pin (Enable) TTL Compatible Input
- Open Drain Full Flag (Multiple Latch Wire-O Ring)
- Master Reset
- Level Shifting Inputs on All Except Enable
- Diode Protection All Inputs
- Supply Voltage Range 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range With Fanout as Follows:

1 TTL Load 4 LSTTL Loads

### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

8-BIT, BUS-COMPATIBLE THREE-STATE LATCHES

Internal Counter - MC14597B Binary Address - MC14598B



L SUFFIX CERAMIC PACKAGE CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX CERAMIC PACKAGE CASE 726

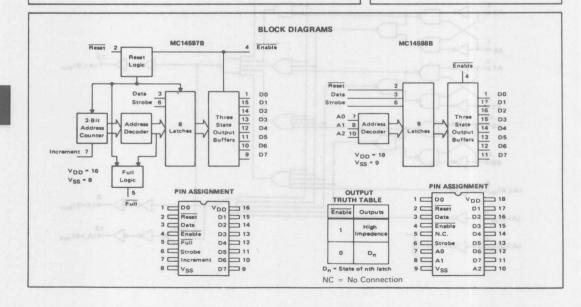


P SUFFIX PLASTIC PACKAGE CASE 707

#### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)



.

### MC14597B • MC14598B

MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	٧
Vin	Input Voltage, Enable (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
Vin	Input Voltage, All other Inputs (DC or Transient)	-0.5 to V <sub>DD</sub> +12	٧
Vout	Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	٧
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C

Ceramic "L" Package: -12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in})$  or  $V_{out} \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

### ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

			Vpp	Tio	w*		25°C		Thi	gh*	
Charac	teristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	. Unit
Output Voltage	"0" Level	VOL	5.0	1-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or	0	0.2	10	-	0.05	-	0	0.05	-	0.05	A SHARE
		00	15	-	0.05	-	0	0.05	-	0.05	
	"1" Level	VOH	5.0	4.95	81 - 1	4.95	5.0	-	4.95	-	Vdc
Vin = 0 or VD	D		10	9.95	_	9.95	10	-	9.95	_	abored as
		m.	15	14.95	50 - 1	14.95	15	_	14.95	-	257 117 80
Input Voltage** -	Enable "0" Level	VIL	Cont.	14.11	or 1	11/12/					Vdc
(VO = 4.5 or 0		100	5.0	-	0.8	-	1.1	0.8	-	0.8	
(VO = 9.0 or 1		ne F	10	-	1.6	-	2.2	1.6	-	1.6	ecionità
(VO = 13.5 or			15	-	2.4	-	3.4	2.4	-	2.4	000000
	"1" Level	VIH	439		22.						Vdc
(VO = 0.5 or 4		·In	5.0	2.0	-	2.0	1.9		2.0		
(VO = 1.0 or 9			10	6.0	20	6.0	3.1		6.0	a property the	merani
(V <sub>O</sub> = 1.5 or 13.5 Vdc)			15	10	- I	10	4.3	_	10	-	
Input Voltage	"0" Level	VIL	568	1	The state of						Vdc
Other Inpu	its	ng .	MAX		De 1						302920
(Vo = 4.5 or 0		na l	5.0	-	1.5	-	2.25	1.5	-	1.5	
(VO = 9.0 or 1	.0 Vdc)	and the same of	10	-	3.0	-	4.50	3.0	-	3.0	
(V <sub>O</sub> = 13.5 or		in I	15	-	4.0	100	6.75	4.0	-	4.0	1013 00
	"1" Level	VIH	457		Ass.		1				Vdc
(VO = 0.5 or 4.5 Vdc)		100	5.0	3.5	0 - 1	3.5	2.75		3.5	-	
(VO = 1.0 or 9			10	7.0	-	7.0	5.50	-	7.0	-	
(V <sub>O</sub> = 1.5 or 13.5 Vdc)		COLUMN TO THE	15	11	-	11	8.25	-	11	MN10381	gent-trik
Output Drive Cur		ГОН	373		37						mAde
(Full-Sink			_055			1				11:5/60 En	reservoid
(V <sub>OH</sub> = 4.6 V		51 1	5.0	-1.0	07 -	-1.0	-2.0	-	-1.0	-	
(V <sub>OH</sub> = 9.5 V		100	10	-	-	-	-6.0	-	1.7	-	120
(V <sub>OH</sub> = 13.5 \			15	-	-	-	-12		-	-	
(VOL = 0.4 Vo		IOL	5.0	1.6	5 m = 1	1.6	3.2	-	1.6	-	mAde
(VOL = 0.5 Vo			10	-	- 1	-	6.0	-	-	-	1
(VOL = 1.5 Vo		100	15	-	- T	-	12	-	-	-	
Input Current	(AL Device)	lin	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdd
Input Current	(CL/CP Device)	lin	15	-	±0.3	-	±0.00001	±0.3	-	±1.0	μAdd
Three-State Leaks	age Current	ITL	85		E 1						μAdo
	(AL Device)		15	-	±0.1	-	±0.00001	±0.1	-	±3.0	
90	(CL/CP Device)		15	-	±1.0	i <del>m</del> art!	±0.00001	±1.0	-	±7.5	noFi Har
Input Capacitance (Vin = 0)	-	Cin	Tis	-	6 - 1	-	5.0	7.5	-	-	pF
Quiescent Current	(AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdd
(Per Package)			10	-	10	2783	0.010	10	210 Fg Ab	300	Name of
			15	-	20	20 100	0.015	20	10 1815 No. 1010	600	Davisi n
Quiescent Current	(CL/CP Device)	IDD	5.0	-	20	-	0.005	20	-	150	μAdo
(Per Package)		00	10	-	40	-	0.010	40	-	300	
			15	-	80	-	0.015	80	-	600	
**Total Supply Cu	urrent at an	İT	5.0			T = (	2.0 μA/kHz)f	+ lon			μAde
External Load C			10				4.0 μA/kHz)f				1
of 130 pF			15				6.0 µA/kHz)f				

<sup>\*</sup>Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

<sup>\*\*</sup> The formulas given are for the typical characteristics only at 25°C.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS\* (TA = 25°C, CL = 130 pF + 1 TTL Load)

				e-Stein 1		VDD	Time to be a first	All Types	and the second	Indeed av
	Char	acteristic		gorg.	Symbol	Vdc	Min	Typ #	Max	Unit
Output Rise			Dogueus	1100	TLH.	-				ns
tTLH, tT	HL = (0.	5 ns/pF) C	L +35 ns	100V	THL	5.0	a turn (mes	100	200	Light   Lool
		2 ns/pF)C		Unu		10	-	50	100	pine4 c
TLH. TT	HL = (0.	16 ns/pF) (	CL +20 n	8	6-1-0	15	-	40	80	numeral
Propagation	Delay Tir	ne	1000		tPLH,	1000				ns
Enable to	Output			Lucian	TPHL	5.0	100	160	320	MELL L
					Table 1	10	u) nggapap at at	125	250	injust Ratios
						15	Hall Sulkhalt	100	200	eQ enumeran
Strobe to	Output					5.0	2 - 150F	200	400	
				V 1913		10	onsass <del>m</del> ed se	100	200	JADIRTO
				19000		15	-	80	160	
Strobe to	Full (N	IC14597B	only)	3.4		5.0	J agv	200	400	1
Otrobe to	Rept -	19154	MAN	91.000		10	E 26%	100	200	SHITT
						15	-08	80	160	equiloV sus
Reset to	Output					5.0	_111	175	350	ragV tml
Leser 10	output					10	_RI	90	180	300
				1 00		15	1 20	70	140	
	-	207.07			200	13	4 67	10	140	Maria Day
Pulse Width Enable				1 81	tWH.	5.0	320	160	0.0	ns
Enable				The same	tWL	10	240	120		State College
				1. 4.0		8.0 15	160	80	- van	to 8.5 a nV
				22				-	1-V 0.1	0 0 0 0 1 DV
Strobe				4.8		5.0	200	100		4 9 21 + UA
						10	100	50	102-110-1	ares a Div
				0.7		15	80	40	-	
Incremen	t (MC14	597B only)			0.8	5.0	200	100	171A 918	10 8 0 × 0 V
				2.5	07	10	100	50	(7. A. 0.6	
				-		15	80	40	(54/ 8.51	0 9 1 5 0 0
Reset						5.0	300	150	.0	egallov n
				30.0		10	160	80	- 100	of setto
			16-1	F 524.5		15	100	50	(-1 V 8 0	VOPASO
Setup Time				21.3	t <sub>BU</sub>		0.		C-SV DIE	ns
Data				-		5.0	100	50	(85-Y 81.7-Y	S.CF # QV
				25.0	0.0	10	50	25	-	
				08.8	0.5	15	35	20	(2 V 8.4	4 9 0 - OA
Address (	MC1459	BB only).		80.0	1 1	5.0	200	100	1.5V 0.9	ou ov
						10	100	50	tary ser	0 6 1 - OA
						15	70	35	2 _ mem	D senD tun
Incremen	t (MC14	597B only)		-2.0	The second	5.0	400	200	7,000 %	R-IIUT)
				9.0	-1.0	10	200	100	- 650	BY . NOA
		3				15	170	85	- 4380	ga . HOA
Hold Time		Tar I		100	th			4	The second	ns
Data				3.2	·n	5.0	100	50	- 3003	A SHOW A PROPERTY.
				0.0		10	50	25	- (003	150 - 10A
					and the second	15	35	20	(cla)	18.T # 10V
Address	(MC1459	8B only)		16000		5.0	100	50	RE JAI	Inginu3 /s
20241	0.74			100004	2 -	10	50	25	E 40/101	Inente 3 /
						15	35	20	rest 40 spec	ed J stard-or
	0.0		3300	TUTTE		1,000	0.0		G.JAI	
Reset Remov	val Time			100003	trem	5.0	20	-25	10 TO TO	ns
				5.0		10	20	-15	-	or Capacitan
						15	20	-10	_	

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C. #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

To Other Latches

To Other Latches

3 Stage Counter

and Decoder

Seven Select

MC14597B FUNCTION DIAGRAM

VDD

VDD 1

Vss

CIk

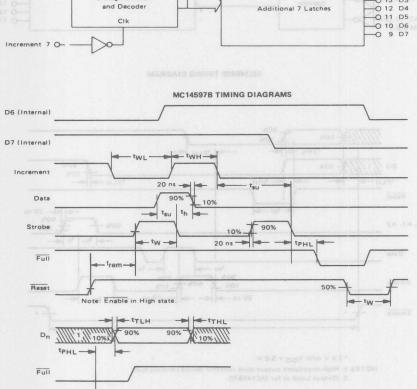
Additional 7 Latches

O 5 Full

-O 1 Do

-O 15 D1 -O 14 D2

-O 13 D3

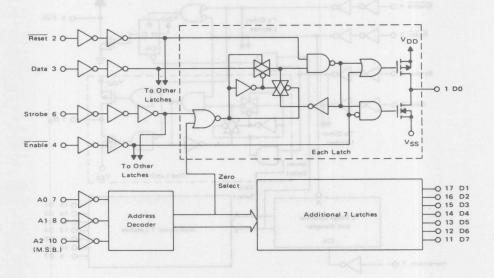


Zero

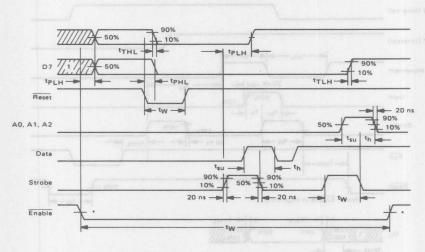
\* 1.4 V with V<sub>DD</sub> = 5.0 V NOTES: 1. High-impedance output state (another device controls bus). 2. Reset in High state.

- twL

Enable



### MC14598B TIMING DIAGRAM



\* 1.4 V with V<sub>DD</sub> = 5.0 V.

NOTES 1. High-impedance output state (another device controls bus).

2. Output Load as for MC14597B.

### MC14597B•MC14598B

LATCH TRUTH TABLE

Strobe	Reset	Addressed Latch	Other
0	1	•	
1	1	Data	
X	0	0	0

= No change in state of latch

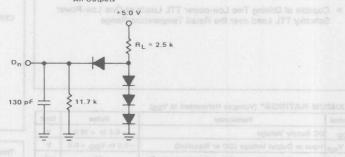
X = Don't care

### TRUTH TABLE FOR MC14597B

Increment	Enable	Reset	Address Counter	Full
7_	×	1	Count Up	-
	×	1	No Change	
X	1	0	Reset to Zero	Set to One
X	0	JUA SER	No Change	Set to One
×	Digse of extens	atri etdaeses secondos si 80 etass sec	If at ADDRESS 7	To Zero on Falling Edge of STROBE

X = Don't care

Test Load
All Outputs



Circuit diagrams external to or containing Motorola products are included as a means of illustration only. Complete information sufficient for construction purposes may not be fully illustrated. Although the information herein has been carefully checked and is believed to be reliable. Motorola assumes no responsibility for inaccuracies. Information herein does not convey to the purchaser

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controlled by the Write/Read line.

 Serial Data Input Parallel Output Master Reset

### MC14599B

FOR COMPLETE DATA **SEE MC14099B** 

### **CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

8-BIT ADDRESSABLE LATCH WITH BIDIRECTIONAL PORT



SUFFIX CERAMIC PACKAGE **CASE 726** 



PSUFFIX PLASTIC PACKAGE **CASE 707** 

### ORDERING INFORMATION

A Series: -55°C to +125°C MC14XXXBAL (Ceramit Package Only)

C Series: -40°C to +85°C MC14XXXBCP (Plastic Package) MC14XXXBCL (Ceramic Package)

## MAXIMUM RATINGS\* (Voltages Referenced to Vos)

Supply Voltage Range = 3.0 Vdc to 18 Vdc

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> +0.5	V
lin, lout	Input or Output Current (DC or Transient), per Pin	±10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

8-BIT ADDRESSABLE LATCH

The MC14599B is an 8-bit addressable latch. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for

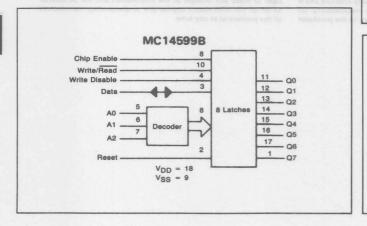
writing into MC14599B. The data pin is a bidirectional data port, which is

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.

Capable of Driving Two Low-power TTL Loads or One Low-Power

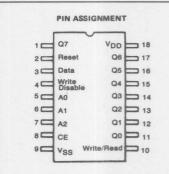
Schottky TTL Load over the Rated Temperature Range

\*Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C Ceramic "L" Package: - 12mW/°C from 100°C to 125°C



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leqslant (V_{in})$  or Vout) ≤ VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.



CMOS Reliability 7

CMOS Reliability



### Introduction

This chapter is intended to demonstrate the quality and reliability aspects of the semiconductor products supplied by Motorola.

### Quality in Manufacturing

### **QUALITY IN DESIGN**

Motorola's quality activity starts at the product design stage. It is its philosophy to "design in" reliability. At all development points of any new design, reliability orientated guidelines are continuously used to ensure that a thoroughly reliable part is ultimately produced. This is demonstrated by the excellent in-house reliability testing results obtained for all Motorola's semiconductor products and, more importantly, by our numerous customers.

#### MATERIAL INCOMING CONTROLS

Each vendor is supplied with a copy of the Motorola Procurement Specification which must be agreed in detail between both parties before any purchasing agreement is made. This is followed by a vendor appraisal report whereby each vendor's manufacturing facility is visited by Motorola's Quality Engineers responsible for ensuring that the vendor has a well organized and adequately controlled manufacturing process capable of supplying the high quality material required to meet the Motorola incoming inspection specification. Large investments have and are continuously being made and Quality Improvement programs developed with our main suppliers concerning:

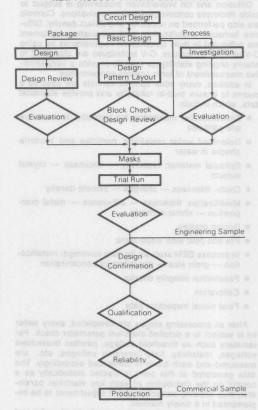
Masks — Silicon — Piece-parts — Chemical products — Industrial gas, etc.

Each batch of material delivered to Motorola is quarantined at Goods-in until the Incoming Quality Organization has subjected adequate samples to the incoming detailed inspection specification. In the case of masks, this will include mask inspection for:

- 1. Defect Density
- 2. Intermask Alignment
- 3. Mask Revision
- 4. Device to Device Alignment
- 5. Mask Type
- Silicon will undergo the following inspections:
- 1. Type "N" or "P"
- 2. Resistivity
- 3. Resistivity Gradient
- 4. Defects
- 5. Physical Dimensions
- 6. Dislocation Density

Incoming chemicals are also controlled to very rigorous standards. Many are submitted to in-house chemical analysis where the supplier's conformance to specification is meticulously checked. In many cases, line tests are performed before final acceptance. A major issue and responsibility for the Incoming Quality Department is to ensure that the most disciplined safety factors have been

### NEW PRODUCT TYPICAL DESIGN FLOW



This basic design flow-chart omits some feedback loops for simplicity

employed with regard to chemicals. Chemicals can and are often rejected because safety standards have not been deemed acceptable.



All processing stages of Motorola products are subjected to demanding manufacturing and quality control standards. A philosophy of "Do it Right the First Time" is instrumental in assuring that Motorola has a reliability record second to none.

The Bipolar and MOS Wafer Fabrication flow charts are examples which highlight the various in-process control points audited by both Manufacturing and Quality people. The majority of these inspections are control audit points with inspection gates at critical points of the process. This is in line with Motorola policy of all personnel being responsible for quality at each manufacturing stage.

Diffusion and ion implantation processing is subject to oxide thickness controls penetration evaluations. Controls are also performed on resistivity and defect density. Diffusion furnaces, metallization, and passivation equipment, are subjected to daily qualification requirements by using C-V plotting techniques. C-V techniques are also used to ensure ongoing stability as they do provide a very sensitive measurement of ionic species concentration.

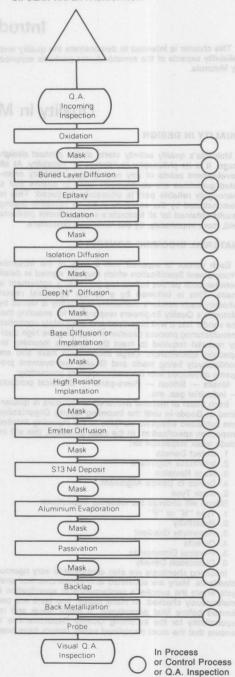
In addition, many other specific controls are used as a means to ensure built-in reliability and provide statistical data, which include:

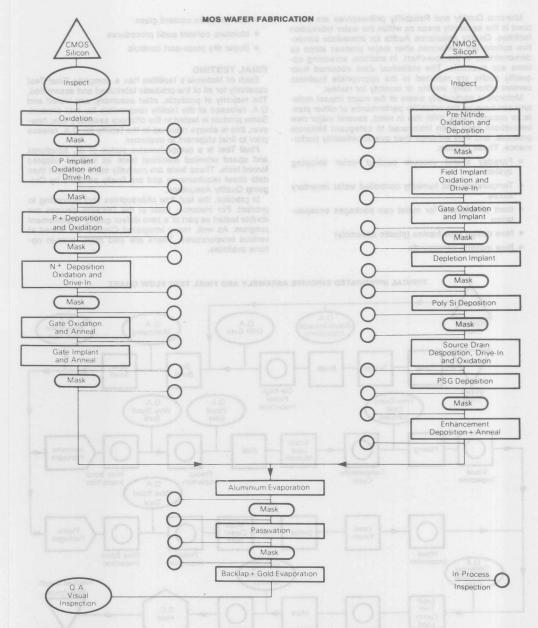
- Environmental monitoring for humidity, temperature and particles
- Deionized water resistivity, particles and bacteria checks in water
- Epitaxial material: resistivity thickness crystal defects
- Oxide: thickness charges pinhole density
- Métallization: thickness adherence metal composition ohmic contacts
- Doping profiles
- · Pre and post etch inspections
- In process SEM analysis for step coverage: metallization grain size phosphorous concentration
- Passivation integrity checks
- Calibration
- · Final visual inspection gate

After all processing stages are completed, every wafer lot is subject to a detailed electrical parameter check. Parameters such as threshold voltage, junction breakdown voltages, resistivity, field inversion voltages, etc., are measured and each batch is sentenced accordingly. The data generated at this point is treated statistically as a control on the distribution of each key electrical parameter, thus allowing corrective action adjustments to be implemented in a timely manner.

Every wafer lot is submitted to an electrical probe test during which every individual die is tested to its electrical specification. Chips which fail are individually inked.

#### **BIPOLAR WAFER FABRICATION**





### **ASSEMBLY**

The assembly operation is of equal importance to the wafer fabrication process as a manufacturing activity which will affect the reliability of the finished product. Motorola continuously makes major investments in specialized assembly areas located in Malaysia, the Philippines and Korea. These assembly plants employ the latest

technologies available to ensure that all Motorola semiconductors are produced to the highest standards of Quality and Reliability. In addition, each wafer fabrication facility has in-house assembly capability which allows some production, specific engineering activity, and qualification of piece-parts suppliers. The major production volumes of Motorola's Integrated Circuits are assembled offshore in the Far East.

Identical Quality and Reliability philosophies are practiced in the assembly areas as within the wafer fabrication facilities. Quality Assurance Audits for immediate corrective actions are performed after major process steps as demonstrated in the flow-chart. In addition, screening options are available. The statistical data obtained from quality audits are reported to the appropriate business centers either daily, weekly, or monthly for review.

Motorola is particularly aware of the major impact moisture can have on the reliability performance of either plastic or ceramic parts. With this in mind, several major new innovations have been introduced to safeguard Motorola products, and thus enhance their overall reliability performance. These include:

- Faraday shield vacuum packed wafer shipping system
- Temperature and humidity controlled wafer inventory stores
- Inert atmosphere for metal can packages encapsulation
- · New design lead frames (plastic assembly)
- New molding compounds

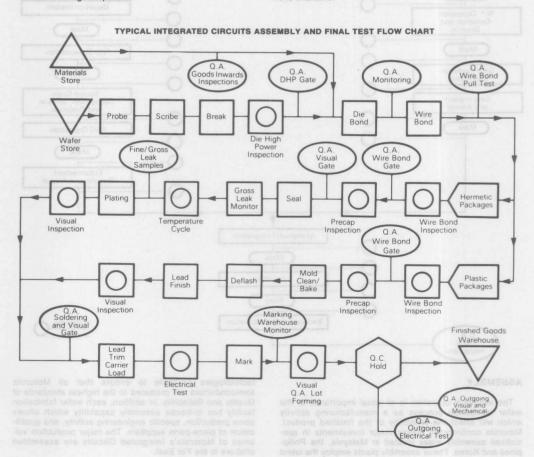
- Low moisture content glass
- Moisture content audit procedures
- Super dry piece-part controls

### **FINAL TESTING**

Each of Motorola's facilities has a complete Final Test capability for all of the products fabricated and assembled. The majority of products, after assembly, are tested and Q.A. released at the facility responsible for that product. Some product is tested in the offshore assembly site; however, this is always returned to the facility for Q.A. release prior to final shipment to customer.

Final Test is a comprehensive series of dc, functional and speed oriented electrical tests as well as adapted forced tests. These tests are normally more stringent than data sheet requirements and are finally sampled by Outgoing Quality Assurance.

In practice, the test flow philosophies vary according to product. For instance, most of the Discrete devices are double tested as part of a zero defect quality improvement program. As well, many integrated Circuits are tested at various temperatures. There are also many burn-in options available.



#### **OUTGOING QUALITY SAMPLING PLAN**

		A.Q.L. 1979	1980	1981	1982	1983	1984	1985
CMOS	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10	0.065	0.065
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15	0.10	0.10
MOS Microprocessors	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10	0.10	0.10
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15	0.10	0.10
NMOS Memories	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10	0.065	0.065
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15	0.065	0.065

### **OUTGOING QUALITY**

Although test procedures may vary from product to product within Motorola, the same philosophy applies when considering quality objectives. Motorola's mission is to be a Quality and Reliability leader worldwide.

#### HIGHLIGHTS:

Motorola recognizes that you, our customers, are truly concerned about improving your own quality image. You are, therefore, concerned about the quality of the product Motorola supplies you.

Our customers measure us by the level of defects in the products we supply at incoming inspection, assembly, and, most important, field reliability.

During the past years, Motorola has achieved impressive reductions in defect rates known as A.O.Q. or Average Outgoing Quality. Instrumental in this success has been the planned continuous reduction in outgoing A.Q.L. to a point where Motorola believes that over all products it can demonstrate the most aggressive A.Q.L.'s in the industry.

This aggressive program has been designed to help eliminate expensive incoming inspection at our customers.

All the facilities also practice an extremely demanding

parts per million program (PPM).

The PPM performance of all Motorola products is calculated in each location using the same method. They are, therefore, directly comparable. Motorola is well aware that when discussing PPM with existing potential customers, it is of paramount importance to explain exactly which failure categories are included in the stated PPM figures. Motorola's PPM figures will include:

- Electrical Inoperative Failure
- Electrical Parametric Failures (dc and ac)
- Visual and Mechanical criteria

In many published cases, stated PPM values refer to Electrical Inoperative failures only.

At Motorola, the Electrical Inoperative, the Electrical Parametric, and the Visual/Mechanical failure rates are calculated separately and then combined to reach an overall total. In this way Motorola believes that it is giving its customers a true and accurate assessment of the quality of the product. Unqualified PPM statements can be misleading and cause the customer to expect quality levels which cannot be achieved. For example, Motorola MOS Logic and Analog IC A.O.Q. is separated into Electrical Inoperative/Electrical Parametric (259 PPM) and Visual/Mechanical (419 PPM). Other product families such as Small Signal Plastic Transistors are already reaching 50 PPM in Electrical Inoperative failure rate.

The Motorola PPM graphs are excellent examples of what has been achieved over the last years with regard to quality improvements.

Improvements between 50% and 300% in average outgoing quality are typical across the broad range of Motorola products.

Throughout the semiconductor industry there have been, and there still are, examples of manufacturers offering higher quality standards at a premium. This is **not** a Motorola strategy, we believe that our customers should expect high quality products at no extra cost. This is Motorola's aim and we will continue to aggressively pursue Quality and Reliability improvements which will be passed on to our customers as an obligation on our part.

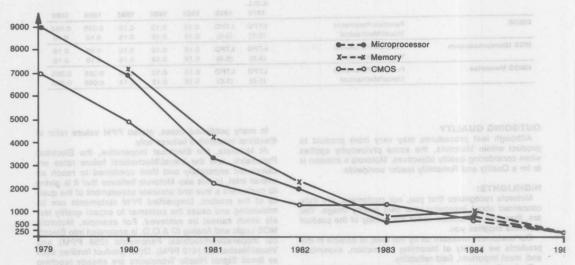
Also, we actively encourage our customers to provide their quality results at their incoming inspection, during their manufacturing process, and from the field in order to better correlate and further improve our quality performance.

### MOTOROLA A.O.Q. PLAN

1980	Hietory					
	Average 1981	1982	Dec 1982	1983	1984	Goal 1985
5000	2370	1380	1150	1399	701	100
7000	4360	2400	2900	918	899	100
7000	3860	2450	2900	763	825	100
	5000 7000	1980 1981 5000 2370 7000 4360	Average         1980         1981         1982           5000         2370         1380           7000         4360         2400	Average         Dec           1980         1981         1982         1982           5000         2370         1380         1150           7000         4360         2400         2900	Average         Dec           1980         1981         1982         1982         1983           5000         2370         1380         1150         1399           7000         4360         2400         2900         918	Average         Dec         1980         1981         1982         1982         1982         1983         1984           5000         2370         1380         1150         1399         701           7000         4360         2400         2900         918         899

A.O.Q. Includes all Defects: Visual, Mechanical, Electrical Inoperative, and Parametric.

### AVERAGE A.O.Q. IN P.P.M. FOR MOS PRODUCTS FIGURES INCLUDE FUNCTIONAL/PARAMETRIC/VISUAL/MECHANICAL



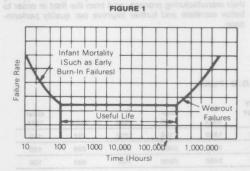
#### RELIABILITY

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of troublefree service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. The following discussion will attempt to present an overview of Motorola's reliability efforts.

BASIC CONCEPTS

It is essential to begin with an explanation of the various parameters of Reliability. These are probably summarized best in the Bathtub Curve (Figure 1). The reliability performance of a device is characterized by three phases: infant

mortality, useful life, and wearout. When a device is produced, there is often a small distribution of failure mechanisms which will exhibit themselves under relatively moderate stress levels and therefore appear early. This period of early failures, termed infant mortality is reduced significantly through proper manufacturing controls and screening techniques. The most effective period is that in which only occasional random failure mechanisms appear. The useful life typically spans a long period of time with a very low failure rate. The final period is that in which the devices literally wear out due to continuous phenomena which existed at the time of manufacture. Using strictly controlled design techniques and selectivity in applications, this period is shifted well beyond the lifetime required by the user.



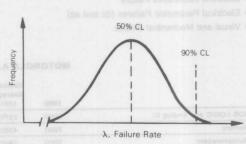


FIGURE 2

Both the infant mortality and random failure rate regions can be described through the same types of calculations. During this time the probability of having no failures to a specific point in time can be expressed by the equation:

$$P_0 = e^{-\lambda t}$$

where  $\lambda$  is the failure rate and t is time. Since  $\lambda$  is changing rapidly during infant mortality, the expression does not become useful until the random period, where  $\lambda$  is relatively constant. In this equation  $\lambda$  is failures per unit of time. It is usually expressed in percent failures per thousand hours. Other forms include FIT (Failures in Time =  $(\%/10^3 \text{ hrs}) \times 10^{-4} = 10^{-9}$  failures per hour) and MTTF (Mean Time To Failure) or MTBF (Mean Time Between Failures), both being equal to  $1/\lambda$  and having units of hours.

Since reliability evaluations usually involve only samples of an entire population of devices, the concepts of the Central Limit Theorem apply and  $\lambda$  is calculated using  $x^2$  distribution through the equation:

$$\lambda \leqslant \frac{x^2 (x, 2r + 2)}{2nt}$$
where  $x = \frac{100 - CL}{100}$ 

CL = Confidence Limit in percent

r = Number of rejectsn = Number of devices

t = Duration of test

The confidence limit is the degree of conservatism desired in the calculation. The Central Limit Theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher  $\lambda$  which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 2). The term (2r+2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to  $\chi^2$  tables.

The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. While Motorola uses data sheet limits to determine failures, sometimes rejects are counted only if they are catastrophic. Due to the increasing chance of a test not being representative of the entire population, as sample size and test time are decreased, the  $x^2$  calculation produces surprisingly high values of  $\lambda$  for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate.

Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_0(t)e - \Theta/kT$$

where R(t) = Reaction rate as a function of time and temperature

 $R_0 = A constant$ 

= Time

θ = Activation energy in electron volts

k = Boltzman's constant

T = Temperature in degrees Kelvin

To provide time-temperature equivalents this equation is applied to failure rate calculations in the form:

$$t = t_0 e \Theta/kT$$

where t = time

to = A constant

The Arrhenius equation essentially states that reaction rate increases exponentially with temperature. This produces a straight line when plotted in log-linear paper with a slope expressed by Θ. Θ may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The activation energy exhibited by semiconductors varies from about 0.3 eV. Although the relationships do not prohibit devices from having poor failure rates and high activation energies, good performance usually does not imply a high  $\Theta$ . Studies by Bell Telephone Laboratories have indicated that an overall ⊕ for semiconductors is 1.0 eV. This value has been accepted by the Rome Air Development Command for time-temperature acceleration in powered burn-in. Data taken by Motorola on Integrated Circuits have verified this number and it is therefore applied as our standard time-temperature regression for extrapolation of high temperature failure rates to temperatures at which the devices will be used (Figure 3). For Discrete products, 0.7 eV is generally

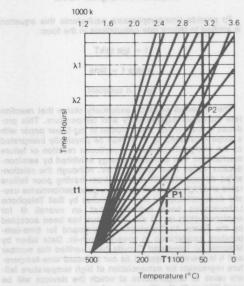
To accomplish this, the time in device hours (t1) and temperature (T1) of the test are plotted as point P1. A vertical line is drawn at the temperature of interest (T2) and a line with a 1.0 eV slope is drawn through point P1.

Its intersection with the vertical line defines point P2, and determines the number of equivalent device hours (t2). This number may then be used with the x² formula to determine the failure rate at the temperature of interest. Assuming T1 of 125°C at t1 of 10,000 hours, a t2 of 7.8 million hours results at a T2 of 50°C. If one reject results in the 10,000 device hours of testing at 125°C, the failure rate at that temperature will be 20%/1,000 hours using a 60% confidence level. One reject at the equivalent 7.8 million device hours at 50°C will result in a 0.026%/1,000 hour failure rate, as illustrated in Figure 4.

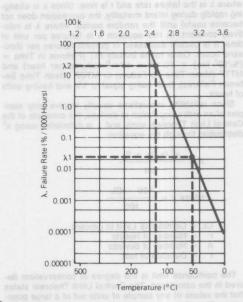
Three parameters determine the failure rate quoted by the manufacturer: the failure rate at the test temperature, the activation energy employed, and the difference between the test temperature and the temperature of the quoted  $\lambda$ . A term often used in this manipulation is the "acceleration factor" which is simply the equivalent device hours at the lower temperature divided by the actual test device hours.

Every device will eventually fail, but with the present techniques in Semiconductor design and applications, the wearout phase is extended far beyond the lifetime required. During wearout, as in infant mortality, the failure rate is changing rapidly and therefore loses its value. The

# FIGURE 3 NORMALIZED TIME-TEMPERATURE REGRESSIONS FOR VARIOUS ACTIVATION ENERGY VALUES



### FIGURE 4 FAILURE RATE



For increased flexibility in working with a broad range of device hours, the time-tem-perature regression lines have been normalized to 500°C and the time scale omitted, permitting the user to define the scale based on his own requirements.

### Reliability

### RELIABILITY TESTS:

### DEFINITION, PURPOSE AND PROCEDURES

These definitions are intended to give the reader a brief understanding of the tests currently used at Motorola for reliability checking. They also state which main failure mechanisms are accelerated by the test.

### HIGH TEMPERATURE STORAGE LIFE

An environmental test where only temperature is the stress. Temperature and test duration must be specified. Usually temperature is the maximum storage temperature of the devices under test. Main failure mechanisms are metallization, bulk silicon, corrosion.

### HIGH TEMPERATURE REVERSE BIAS (HTRB)

An environmental stress combined with an electrical stress whereby devices are subjected to an elevated temperature and simultaneously reverse biased. To be effec-

tive, voltage must be applied to the devices until they reach room temperature at the completion of the test. Temperature, time and voltage levels must be specified. Accelerated failure mechanisms are inversion, channeling, surface contamination.

### HIGH HUMIDITY, HIGH TEMPERATURE REVERSE BIAS (H3TRB)

A combined environmental/electrical stress whereby devices are subjected to an elevated ambient temperature and high humidity, simultaneously reverse biased for a period of time. Normally performed on a sample basis (qualification) on non-hermetic devices. The most common condition is 85°C and 85% relative humidity. More extreme conditions generally are very destructive to the chambers used. Time, temperature, humidity and voltage must be specified. This accelerated test mainly detects corrosion risks.

### STEADY STATE OPERATING LIFE

An electrical stress whereby devices are forward (reverse for zeners) biased at full rated power for prolonged duration. Test is normally 25°C ambient and power is 100% of full rated. (For power devices the I/C's maximum operating Ti is used.) Duration, power and ambient, if other than 25°C, must be specified. Accelerated failure mechanisms mainly are metallization, bulk silicon, oxide, inversion, and channeling.

### DYNAMIC OPERATING LIFE

An electrical stress whereby devices are alternately subjected to forward bias at full rated power or current and reverse bias.

Duration, power, duty cycle, reverse voltage ambient and frequency must be specified. Used normally for rectifiers and silicon controlled rectifiers. Failure mechanisms are essentially the same as steady state operating life.

### INTERMITTENT OPERATING LIFE (POWER CYCLING)

An electrical stress whereby devices are turned on and off for a period of time. During the "on" time the devices

are turned on at a power such that the junction temperature reaches its maximum rating. During "off" cycle the devices return to 25°C ambient. Duration, power, or duty cycle must be individually specified. Accelerated failure mechanisms are mainly die bonds, wire bond, metallization, bulk silicon, and oxide.

### THERMAL SHOCK (TEMPERATURE CYCLING)

An environmental stress whereby devices are alternately subjected to a low and high temperature with or without a dwell time in between to stabilize the devices to 25°C ambient — the medium is usually air. Temperatures, dwell times and cycles must be specified. Failure mechanisms are essentially die bonds, wire bonds, and package.

### THERMAL SHOCK (GLASS STRAIN)

An environmental stress whereby the devices are subjected to a low temperature, stabilized and immediately transferred to a high temperature. The medium is usually liquid. Failure mechanisms essentially are the same as temperature cycling.

### **EXAMPLE OF NEW PROCESS QUALIFICATION TESTS**

Test	01081	Condition	Duration
Operating Life	down	125°C, 5 V or 15 V	1,000 Hours
Temperature Humidity Bias	Dies Ace Dies Ace Dies ZO c	85°C, 85% R.H. 5 V or 15 V	1,000 Hours
Autoclave	8-0	121°C, 100% R.H. 15P.S.I.G.	144 Hours
High Temperature Storage		150° C	1,000 Hours
Thermal Cycle (Air to Air)	29/0	- 65°C to 150°C 5 Min Dwell	1,000 Cycles
Thermal Shock (Liquid to Liquid)	30	- 65°C to 150°C 5 Min Dwell	1,000 Cycles
Shock, Vibration, and Constant Acceleration	ma	1,500G, 3 per Axis 150-2,000 Hz, 20 g 30 kg	0.5 MS 2 Hours
Data Retention Bake (Non-Volatile Memories)		200/250°C	1,000 Hours

### MECHANICAL SHOCK

A mechanical stress whereby the devices are subjected to high impact forces normally in two or more of the six orientations: X1, Y1, Z1, X2, Y2, Z2. Tests are to verify the physical integrity of the devices. G forces, pulse duration, and number of shocks and axes must be specified.

### VIBRATION VARIABLE FREQUENCY

Same as Vibration Fatigue except that frequency is logarithmically varied form 100 Hz to 1 kHz and back. Number of cycles is normally four. Cycle time, amplitude and total duration must be specified. Failure mechanisms are mainly package, wire bond — this test is not applicable to molded devices.

(POWER CYCLING

### **EXAMPLE OF NEW PACKAGE QUALIFICATION TESTS**

Test	Condition	Duration
Operating Life	125°C, 5 V or 15 V	1,000 Hours
Temperature Humidity Bias	85°C, 85% R.H. 5 V or 15 V	1,000 Hours
Autoclave	121°C, 100% R.H. 15 P.S.I.G.	
High Temperature Storage	150°C	1,000 Hours
Thermal Cycle (Air to Air)	- 65°C to 150°C 5 Min Dwell	1,000 Cycles
Thermal Shock (Liquid to Liquid)	-65°C to 150°C 5 Min Dwell	1,000 Cycles
Shock, Vibration, and Constant Acceleration	1,500 G, 3 per Axis 150 – 2,000 Hz, 20 g 30 kg	0.5 ms 2 Hours
Hermeticity	1.85, 10 - 8 atm cc/sec	gualpotus
Visual Inspection		lugh Temperature. Forage
	Outline Dwg.	hampar Cycle
Marking Permanency		fijA 5t tiA
Solderability	230°C	3 Seconds
	1.5 Gram	tria nominditi pipari umagni Appelatbiri
Die Shear		

### **EXAMPLE OF STANDARD RELIABILITY PROGRAM**

Reliability Engineering Department	Motorola Reliability Pr	rogram	For:		Ceranic (25°C 6.5×19/ State Blas
Test Group	Test	Tio .	SS	Frequency	Test Methods/Conditions
Reliability Audit	Thermal Shock		25	1 Product Line Per Week	- 25°C, + 125°C. Dwell Time 5 mn, 100 Cycles
	High Temperature Reverse Bias		40		TA = 150°C, VCB = .8 VCB max. 168 hours
Life Tests	High Temperature Reverse Bias High Temperature Storage	Vas	25 (+2) 25 (+2)	3 Product Lines Per Month	TA = 150 °C, VCB = .8 VCB max. 1,000 hours  TA = 150 °C, 1,000 hours
	Steady State	V31	25		TA = 125°C, 1,000 hours
	Life High Humidity High Temperature Reverse Bias	VSTr	(+2) 25 (+2)		TA = 85°C, 85% Humidity VCB = .8 VCB max. 1,000 hours
(+2) devices for correl		va L	1 + 21		TO SEE THE PROPERTY AND ADMINISTRAL

Product Family	Test Conditions	Device Hours	No. Of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
Non Hermetic Interface I/C's	Operating T <sub>j</sub> = 155°C	591,552	64	1 eV	70°C	0.014
Consumer I/C's	Operating T <sub>j</sub> = 125°C	13,082,000	39	1 eV	70°C	0.0029
DO4/DO5 Rectifier	T <sub>j</sub> = 150°C VR = .8 BVR	798,000	5	.7 eV	70°C	0.009
Plastic Axial Diodes	T <sub>j</sub> = 100°C VR = .8 BVR	295,000	3	.7 eV	70°C	0.21
Button Diodes	T <sub>j</sub> = 150°C VR = .8 BVR	520,000	5	.7 eV	70°C	0.014
Small Signal Plastic Transistor	T <sub>j</sub> = 150°C VCB = .8 BVCO	579,000	6	.7 eV	70°C	0.014 White-2 source
Small Signal Metal Transistor	T <sub>j</sub> = 150°C VCB = .8 BVCBO	3,944,000	12	.7 eV	70°C	0.0039
Case 77 Power Plastic Transistor	$T_j = 150$ °C VBC = .8 BVCBO	364,416	2	.7 eV	70°C	0.0097
TO220 Power Plastic Transistor	$T_j = 150$ °C VCB = .8 BVCBO	366,080	0 8A	.7 eV	70°C	0.0028
TO3P Power Plastic Transistor	$T_j = 150$ °C VCB = .8  BVCBO	297,024	no n3 plana	.7 eV	70°C	0.016
TO3 Power Metal Transistor	$T_j = 150$ °C VCB = .8 BVCBO	247,104	tore 3 to Fi edouals	notion.7 eV	70°C	0.019

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
CMOS Ceramic	125°C Static Bias	6.5×10 <sup>7</sup>	11	1 EV	50°C 85°C	0.00074 0.025
CMOS Plastic	125°C Static Bias	2.1 × 10 <sup>8</sup>	17	1 EV	85°C	0.0088
6800 Series Plastic	125°C Dynamic Bias 5 V	2.88 × 10 <sup>6</sup>	47	1 EV	70°C	0.039
U.V. EPROM Life Test	125°C Dynamic Bias 5 V	434,456	3	1 EV	70°C	0.009
Data Retention	250°C Bake	519,120	3	0.7 EV	70°C	0.0075
EEPROM Life Test	125°C Dynamic Bias 5 V	917,280	25	1 EV	70°C	0.027
Data Retention	250°C	966,672	19	0.7 EV	70°C	0.020
64K DRAM	125°C Dynamic Bias 5.5 V	1.05 × 10 <sup>6</sup>	6	0.7 EV	70°C	0.028

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 90% Confidence
LS-TTL	125°C Static Basis - 5.2 V	VeV.	-	1.0 eV	70°C	0.0029
ECL	125°C Static Bias 5 V	61.74×10 <sup>6</sup>	7	1.0 eV	85°C	0.0189

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
Operational Amplifier	Operating T <sub>j</sub> = 135°C	437,472	2	1 eV	70°C	0.0026
Hermetic Interface I/C's	Operating T <sub>j</sub> = 135°C	718,848	4	1 eV	70°C	0.0033

The reliability approach at Motorola Semiconductors is based on designing-in reliability rather than testing for reliability only. This concept is reflected by Motorola's mandatory procedures which require product, process, and packaging qualification on three independently produced lots before any product is released to volume production. Reliability engineering approval, supported by an officially documented report, is required before any product is released to manufacturing. Tests at both maximum rated and accelerated stress levels are performed. Acceleration is important to determine how and at what stress level a new design, product process, or package would fail. This information provides an indication of which design changes can be implemented to ensure a wider and safer margin between the maximum rated stress condition and the devices stress limitation.

As well as qualifying all new products, processes, and piece-parts, each Motorola manufacturing facility operates an ongoing reliability monitor which covers all process and packaging options. This program provides a continuous up-to-date data base which is summarized in periodical reports.

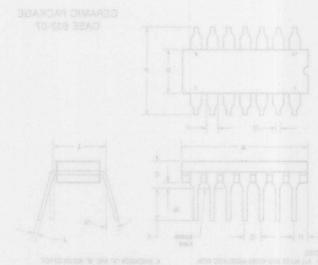
Reliability statistics supporting all Motorola's Semiconductor devices can be obtained from any of the Motorola Sales Offices upon request. The present operating life test results demonstrate Motorola's reputation for producing semiconductors with reliability second to none.

The Quality organization in each facility is responsible for preparing and maintaining a Quality Manual which describes in detail the quality systems and associated Reliability and Quality Assurance organization, policies, and procedures. This manual must be appraised and ultimately approved by the appropriate approval authority.

### PACKAGE DIMENSIONS

The standard package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter. Surface mount packages may be special ordered by specifying the following suffixes: "D" (narrow SOIC), "DW" (wide SOIC), or "FN" (PLCC). For example, to order a quad NOR gate, use MC14001BCD. For package availability, refer to prochure BR274.

### 14-PIN PACKAGE



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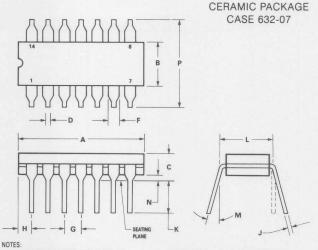
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**Package Dimensions** 

data sheets. Dimensions for the packages are given in this chapter. Surface mount packages may be special ordered by specifying the following suffixes: "D" (narrow SOIC), "DW" (wide SOIC), or "FN" (PLCC). For example, to order a quad NOR gate, use MC14001BCD. For package availability, refer to brochure BR274.

### 14-PIN PACKAGE =



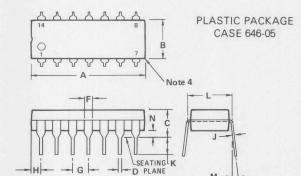
- 1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
- 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL
- 3. 632-01 OBSOLETE, NEW STD. 632-03. SEE ISSUE "C" FOR REFERENCE.
- 4. DIMENSION "A" AND "B" (632-07) DO NOT INCLUDE GLASS RUN-OUT.
- 5. 632-06 OBSOLETE, NEW STD 632-07 6. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM

MATERIAL CONDITION.



	MILLIN	IETERS	INCHES	
DIM	MIN	MAX	MIN	MAX
Α	19.05	19.94	0.750	0.785
В	6.10	7.49	0.240	0.295
C	_	5.08	-	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54	BSC *	0.100	BSC 4
Н	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	4.32	0.125	0.170
L	7.62 BSC *		0.300	BSC *
M	-	15°	-	15°
N	0.51	1.02	0.020	0.040

\*BSC = Basic Spacing Between Centerlines



### NOTES:

- 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE **POSITION AT SEATING** PLANE AT MAXIMUM MATERIAL CONDITION.
- 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



	MILLIN	METERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	18.16	19.56	0.715	0.770	
В	6.10	6.60	0.240	0.260	
C	4.06	5.08	0.160	0.200	
D	0.38	0.53	0.015	0.021	
F	1.02	1.78	0.040	0.070	
G	2.54	BSC*	0.100 BSC*		
Н	1.32	2.41	0.052	0.095	
J	0.20	0.38	0.008	0.015	
K	2.92	3.43	0.115	0.135	
L	7.62 BSC*		0.300	BSC*	
M	00	100	00	100	
N	0.51	1.02	0.020	0.040	

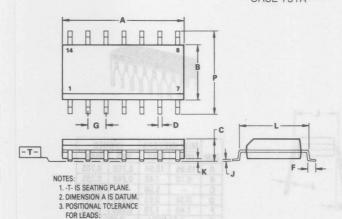
\*BSC = Basic Spacing Between Centerlines

3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH. 4. ROUNDED CORNERS OPTIONAL.

# PACKAGE DIMENSIONS (Continued)

### 14-PIN PACKAGE

SOIC PACKAGE CASE 751A



♦ 0.25 (0.010) M A S

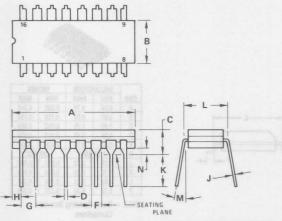


	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	8.54	8.74	0.336	0.344
В	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1,27	BSC *	0.050	BSC *
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

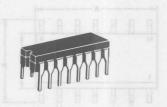
\*BSC = Basic Spacing Between Centerlines

### 16-PIN PACKAGE

CERAMIC PACKAGE CASE 620-08

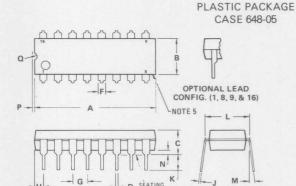


- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- 2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
- 3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
  5. DIM "F" MAY NARROW TO 0.76 mm
- DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.



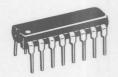
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
В	6.10	7.49	0.240	0.295
C	-	5.08	3047	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54	BSC*	0.100 BSC*	
Н	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC *		0.300	BSC *
M	-	150	-	15 <sup>0</sup>
N	0.51	1.02	0.020	0.040

\*BSC = Basic Spacing Between Centerlines



#### NOTES

- LEADS WITHIN 0.13 mm
   (0.005) RADIUS OF TRUE
   POSITION AT SEATING
   PLANE AT MAXIMUM
   MATERIAL CONDITION.
- 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- 4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
- 5. ROUNDED CORNERS OPTIONAL.



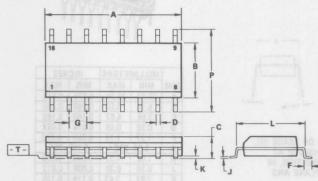
	MILLIN	ETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
A	18.80	21.34	0.740	0.840	
В	6.10	6.60	0.240	0.260	
C	4.06	5.08	0.160	0.200	
D	0.38	0.53	0.015	0.021	
F	1.02	1.78	0.040	0.070	
G	2.54	BSC *	0.100 BSC*		
Н	0.38	2.41	0.015	0.095	
J	0.20	0.38	0.008	0.015	
K	2.92	3.43	0.115	0.135	
L	7.62 BSC *		0.300	BSC*	
M	00	100	00	100	
N	0.51	1,02	0.020	0.040	

\*BSC = Basic Spacing Between Centerlines

# PACKAGE DIMENSIONS (Continued)

### **16-PIN PACKAGE**





्र<sub>िक्</sub>रिक्षेत्र के विकास

	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	9.78	10.01	0.385	0.394
В	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27	BSC *	0.050 BSC 1	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

\*BSC = Basic Spacing Between Centerlines

NOTES:

- 1. -T- IS SEATING PLANE.
- 2. DIMENSION A IS DATUM. 3. POSITIONAL TOLERANCE
- FOR LEADS:

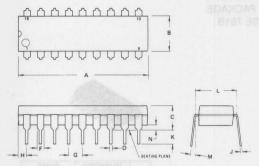
  | 0.25 (0.010) | A | S |

| Medicine | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | M

NO PLANE NO

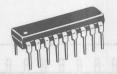
LEADE, TRUE PORTIONED
WITHRE 0.35 am (0.010 BilAT SEATING PLANE, AV
MAXIMUM MATERIAL
CONNECTION
CONNECTION

### PLASTIC PACKAGE CASE 707-02



### NOTES:

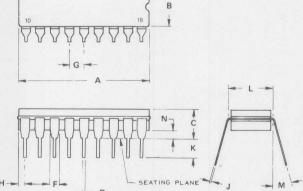
- 1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
- 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



	MILLIN	METERS	INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
В	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54	BSC *	0.100 BSC*	
Н	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62	BSC*	0.300	
M	00	150	00	150
N	0.51	1.02	0.020	0.040

\*BSC = Basic Spacing Between Centerlines

### CERAMIC PACKAGE CASE 726-04



- AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION:
- 1. LEADS, TRUE POSITIONED 2. DIM "L" TO CENTER OF WITHIN 0.25 mm (0.010) DIA. LEADS WHEN FORMED PARALLEL.
  - 3. DIM "A" & "B" INCLUDES MENISCUS.



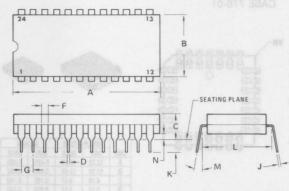
	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	22.35	23.11	0.880	0.910
В	6.10	7.49	0.240	0.295
С	-	5.08	-	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54	BSC*	0.100 BSC*	
Н	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC *		0.300	BSC*
M	00	15 <sup>0</sup>	00	15 <sup>0</sup>
N	0.51	1.02	0.020	0.040

\*BSC = Basic Spacing Between Centerlines

### PACKAGE DIMENSIONS (Continued)

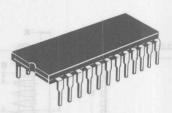
### 24-PIN PACKAGE

### CERAMIC PACKAGE CASE 623-05



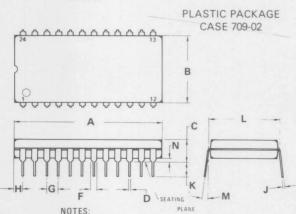
### NOTES:

- 1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

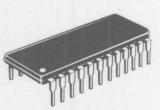


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
В	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54	BSC *	0.100	BSC *
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
į	15.24	BSC	0.600	BSC *
M	00	150	00	150
N	0.51	1.27	0.020	0.050

\*BSC = Basic Spacing Between Centerlines



- POSITIONAL TOLERANCE OF LEADS (D),
   SHALL BE WITHIN 0.25 mm (0.010) AT
   MAXIMUM MATERIAL CONDITION, IN
   RELATION TO SEATING PLANE AND
   EACH OTHER.
- 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



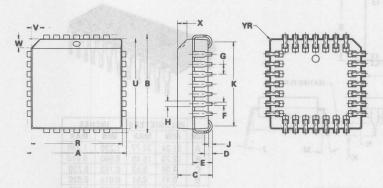
	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	31.37	32.13	1.235	1.265
В	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54	BSC *	0.100	BSC*
Н	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC*		0.600	BSC*
M	00	150	00	150
N	0.51	1.02	0.020	0.040

\*BSC = Basic Spacing Between Centerlines

### PACKAGE DIMENSIONS (Continued)

### 28-PIN PACKAGE

PLCC PACKAGE CASE 776-01





### NOTES:

- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
- 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 3. CONTROLLING DIMENSION: INCH

	MILLIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
В	12.32	12.57	0.485	0.495
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27	BSC*	0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.38	0.63	0.015	0.025
K	9.91	10.92	0.390	0.430
R	11.43	12.57	0.450	0.456
U	11.43	12.57	0.450	0.456
٧	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
γ	0.00	0.50	0.000	0.020

\*BSC = Basic Spacing Between Centerlines